Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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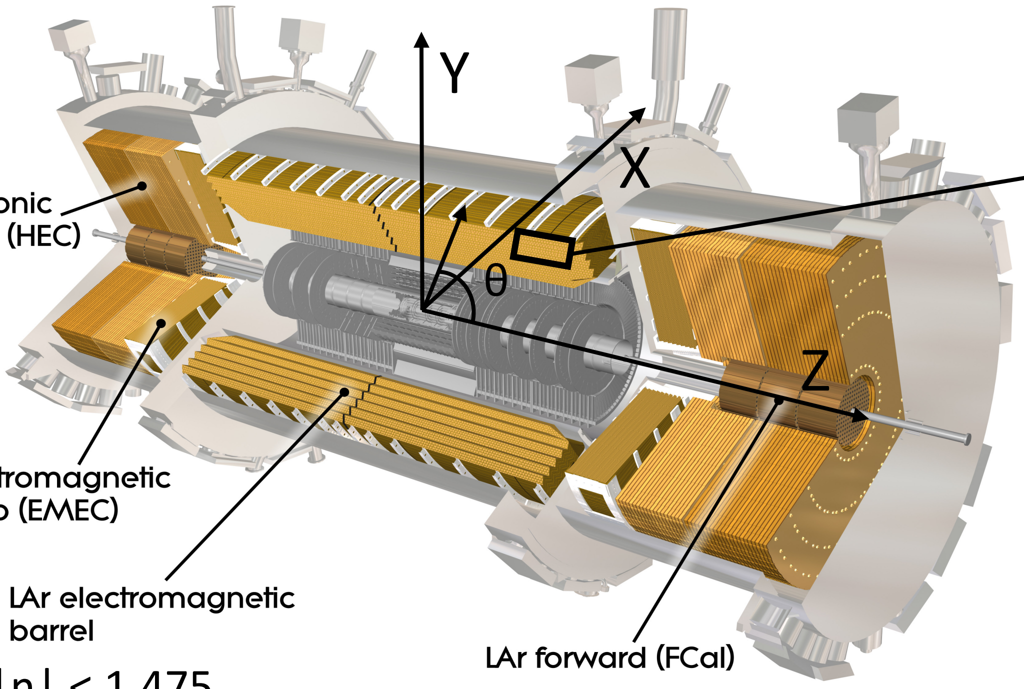
ATLAS EXPERIMENT

TEXAS
The University of Texas at Austin

Liquid Argon (LAr) Calorimeter

1.5 < |η| < 3.2
Copper absorber,
parallel plate geometry

LAr hadronic end-cap (HEC)



LAr electromagnetic end-cap (EMEC)

1.375 < |η| < 3.2

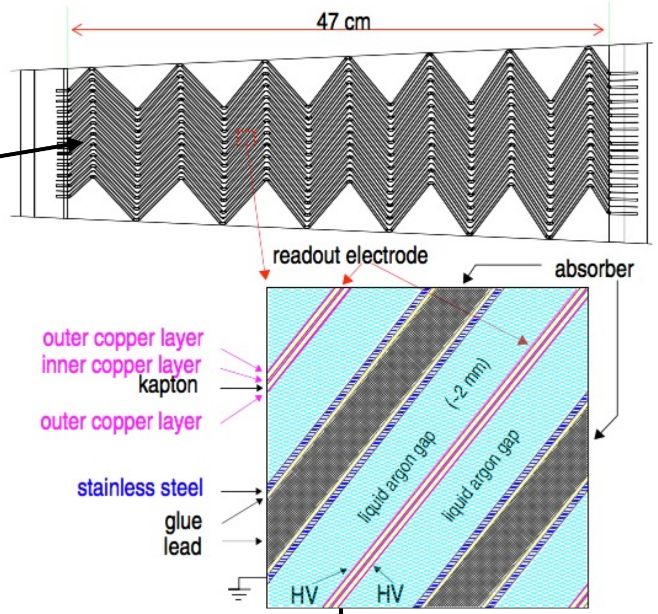
Lead absorber,
accordion geometry

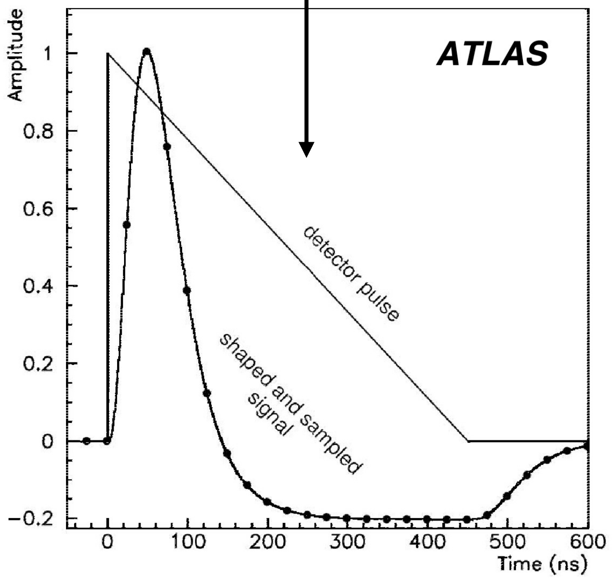
LAr electromagnetic barrel

|η| < 1.475

LAr forward (FCal)

1.5 < |η| < 3.2
Copper and Tungsten absorber,
cylindrical electrodes parallel to the beam

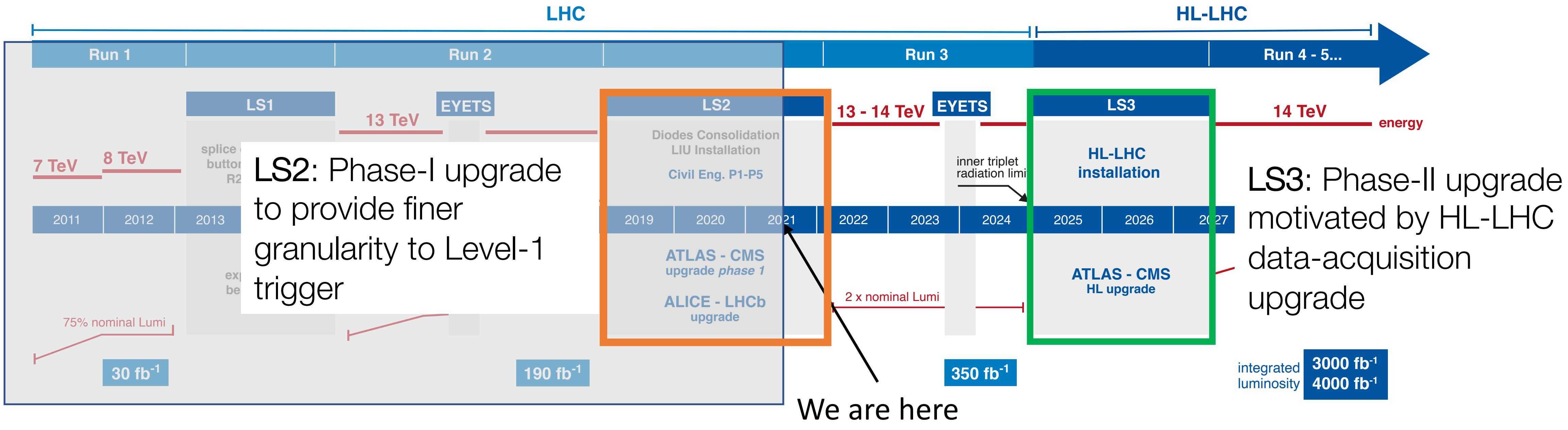




~182,00 readout channels

$$\eta \equiv -\ln[\tan(\theta/2)]$$

High Luminosity LHC (HL-LHC)



- ATLAS detector undergoes several upgrades during Long Shutdown 2 (LS2) and Long Shutdown 3 (LS3)
- For Run 3, LHC will operate at 2x nominal luminosity and 2x average number of interactions
- Phase-I upgrade will provide higher-granularity and higher-resolution from the LAr calorimeter to Level-1 trigger processors
- In HL-LHC period, LHC will operate at 5–7.5x nominal luminosity and 10x average number of interactions

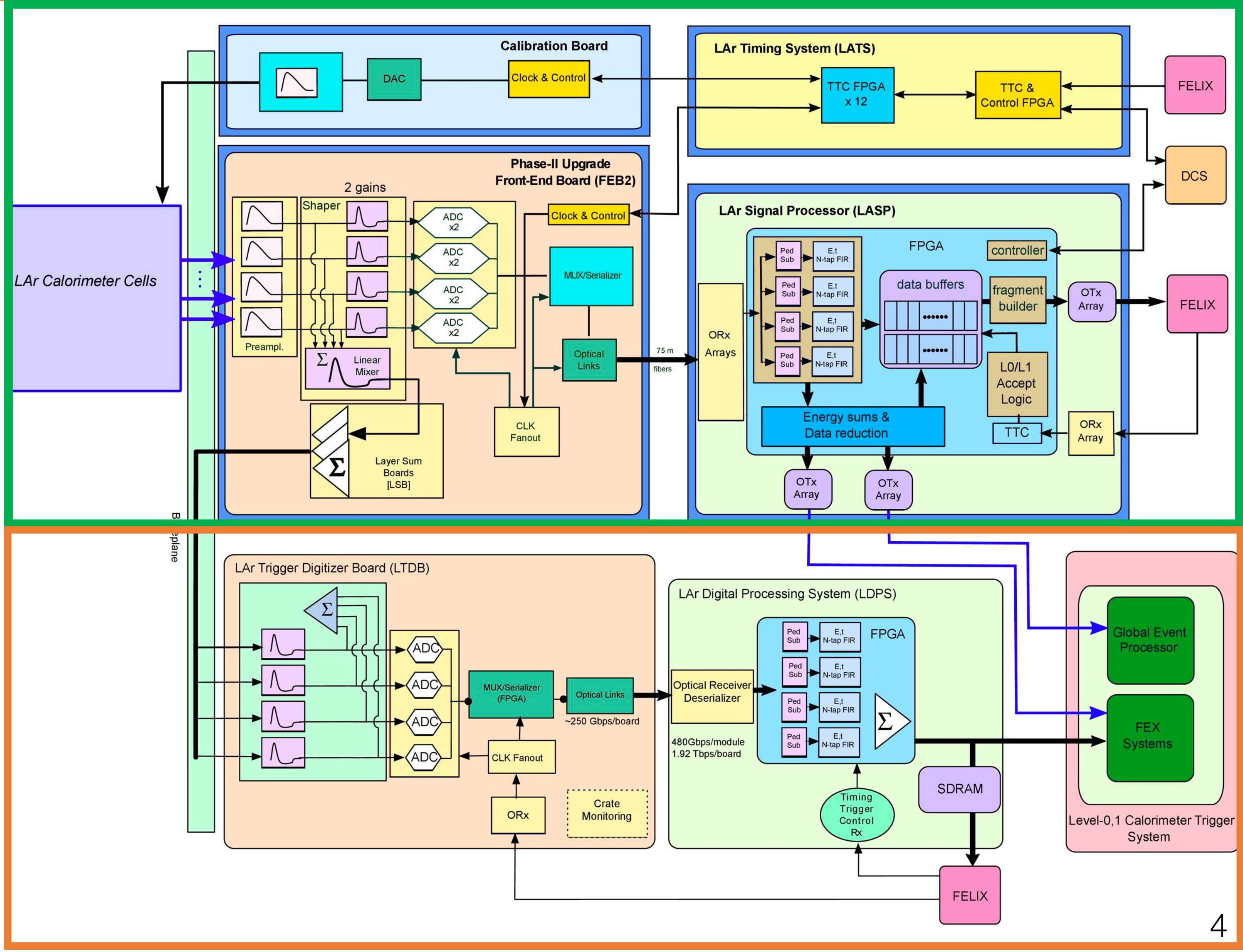
LAr Calorimeter Upgrade Roadmap

Phase-II

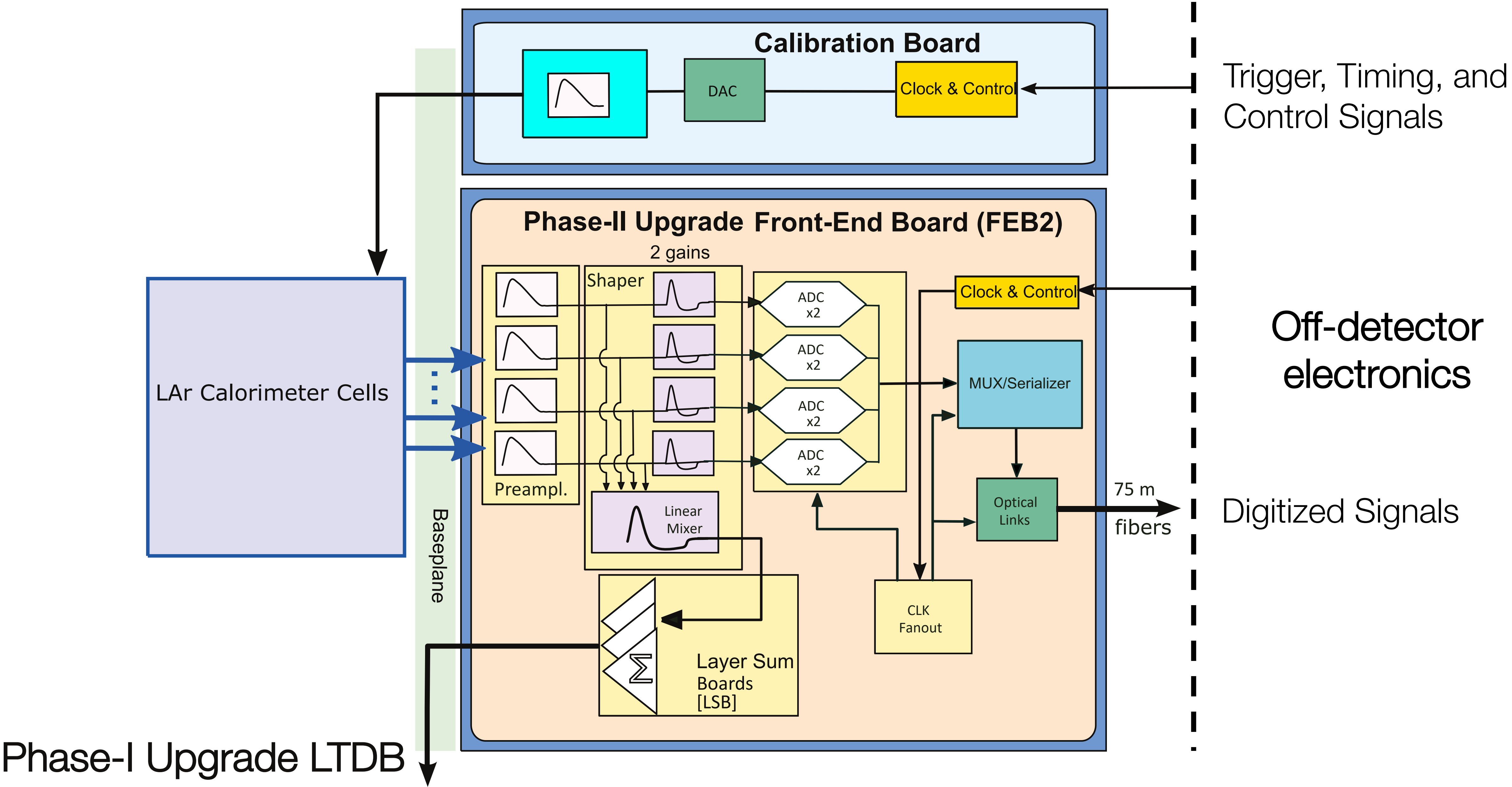
Motivated by HL-LHC data-acquisition upgrade. Digitize analog signals @ 40 MHz, send digitized signals off-detector

Phase-I

Staged approach to provide finer granularity to the Level-1 trigger processors

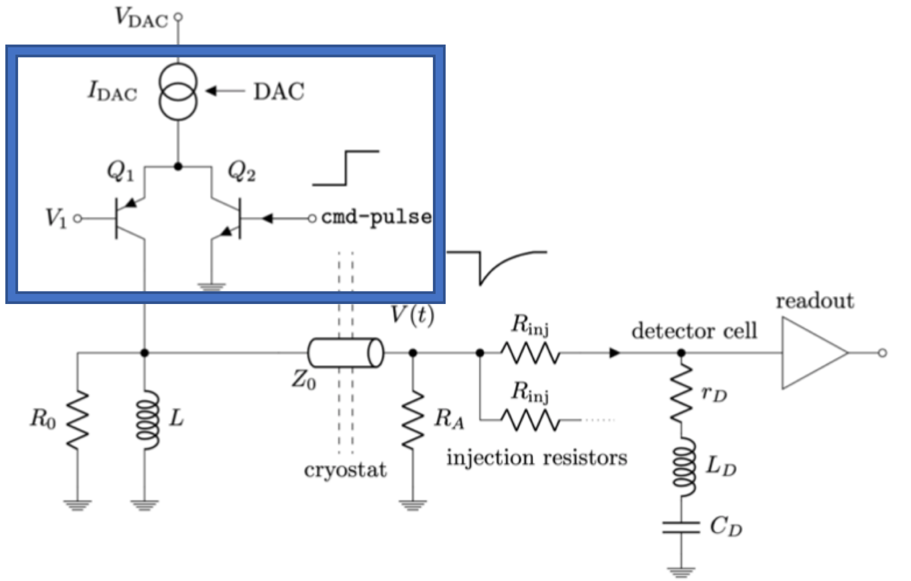


On-detector electronics



Calibration System

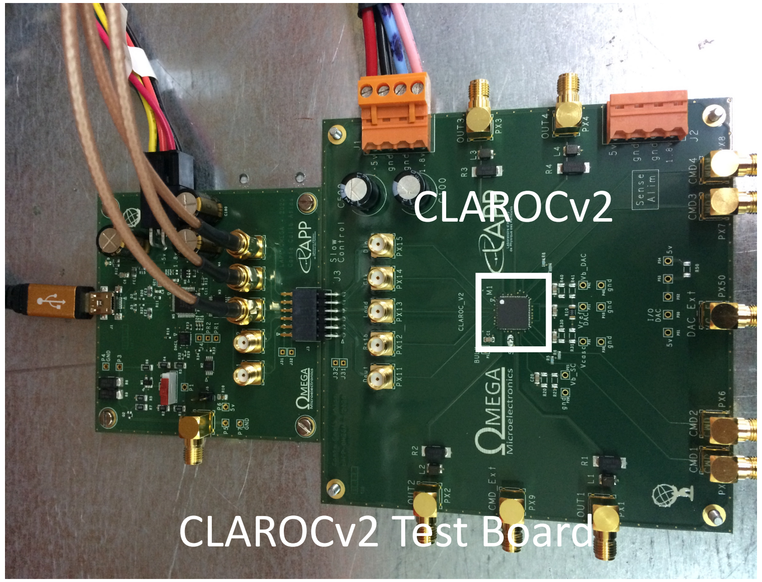
Deliver a calorimeter pulse with precisely known amplitude and shape close to calorimeter ionization to calibrate the readout electronics



- Requirements:

  16-bit dynamic range; integral non-linearity (INL) < 0.1%;

  pulse rise time < 1ns
- Calibration of Liquid Argon Output Chip (CLAROC)
  - Custom high-frequency (HF) switch + 16-bit digital-to-analog converter (DAC) designed in XFAB, HV CMOS 180 nm technology
  - HF switch is radiation hard, however the DAC does not meet the radiation tolerance requirements
    - **CLAROCv3**: HF switch + current mirrors in XFAB 180nm
    - **Link and DAC for CLAROC (LADOC)**: 13-bit DAC designed in TSMC 130nm CMOS technology to command the HF switch
- 32-channel calibration prototype board (CABANON) fabricated



Pre-amplifier+Shaper (PA/S)

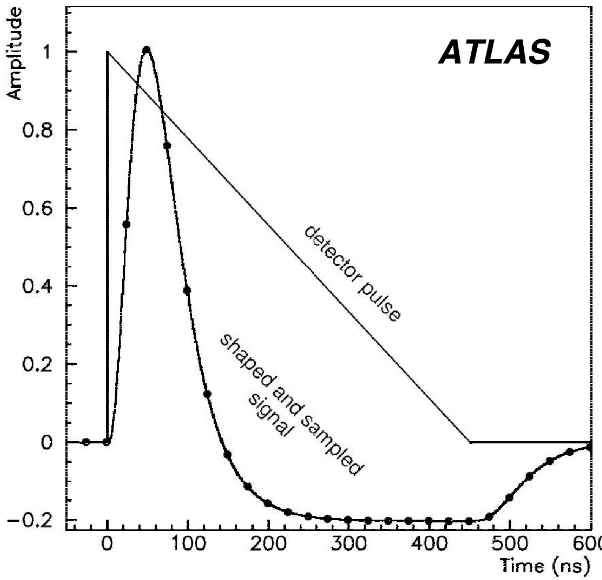
Amplification and bipolar CR-(RC)^2 shaping of signal from calorimeter cell

- Requirements:

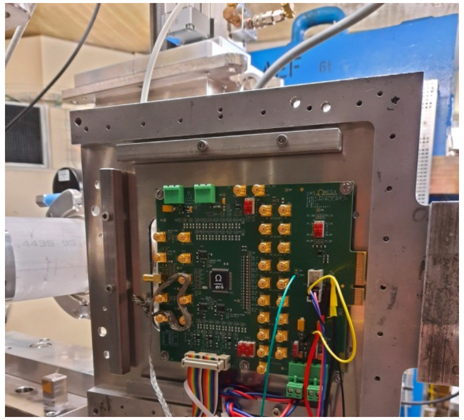
  Dynamic range: 10 mA for 25 Ω channels,
  2 mA for 50 Ω channels

  Preamplifier noise: 350 nA for 10 mA channels,
  120 nA for 2 mA channels

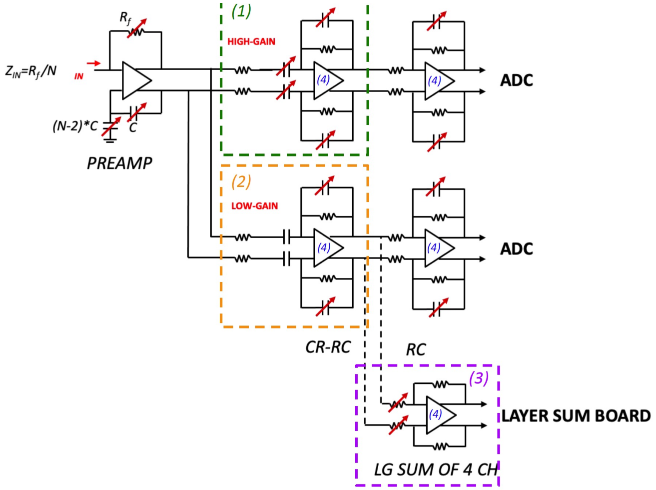
  INL < 0.2%; sum of four channels sent to Level-0 Trigger



- Liquid Argon Upgrade Read Out Chip (LAUROC)
  - Single-ended pre-amplifier with two-gain shaper with differential outputs to the analog-to-digital converter (ADC)
  - LAUROC2 meets all specifications
- ATLAS Liquid Argon Front End (ALFE)
  - Fully-differential pre-amplifier with two-gain shaper with differential outputs to the ADC
  - ENI <147 nA@46 ns (25 Ω)/ <47.5 nA@38 ns (50 Ω)



LAUROC Test Board



ALFE2 channel architecture

Analog-to-digital converter (ADC)

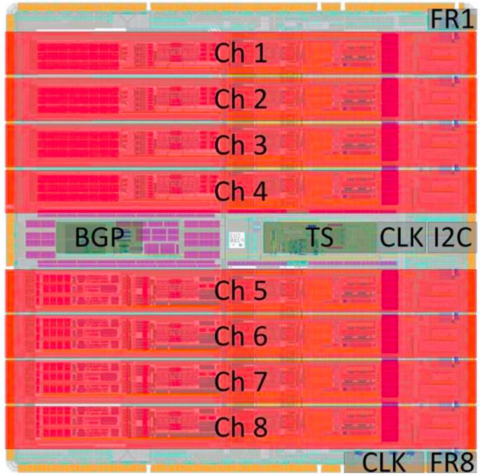
Digitize the analog signal on two gains to cover the full dynamic range

- Requirements:

  Digitize both gains of four calorimeter channel signals @ 40 MHz

  14-bit dynamic range, >11-bit precision

- COLUTA
  - Eight channel, 15-bit ADC
  - Multiplying DAC (MDAC) block determines the most significant three bits of the 15-bit code
  - 12-bit pipeline Successive Approximation Register (SAR) digitizes the analog signal
  - Digital Data Processing Unit (DDPU) block computes ADC codes and outputs data to optical links @ 640 MHz
  - Meets design specifications, including radiation hardness



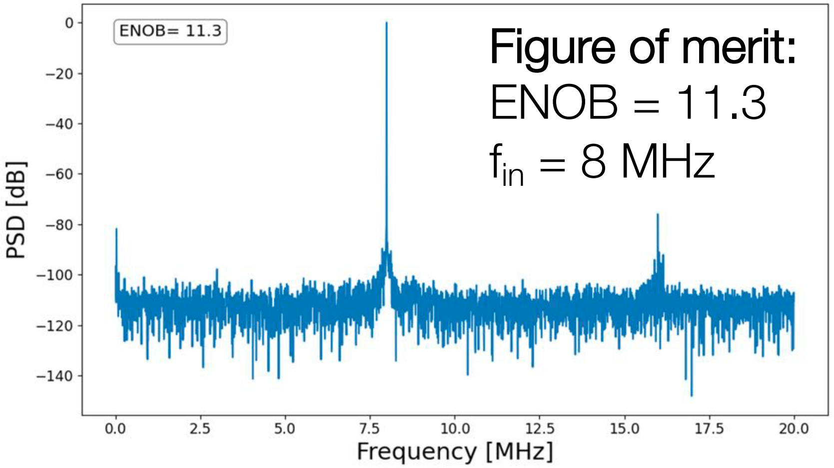
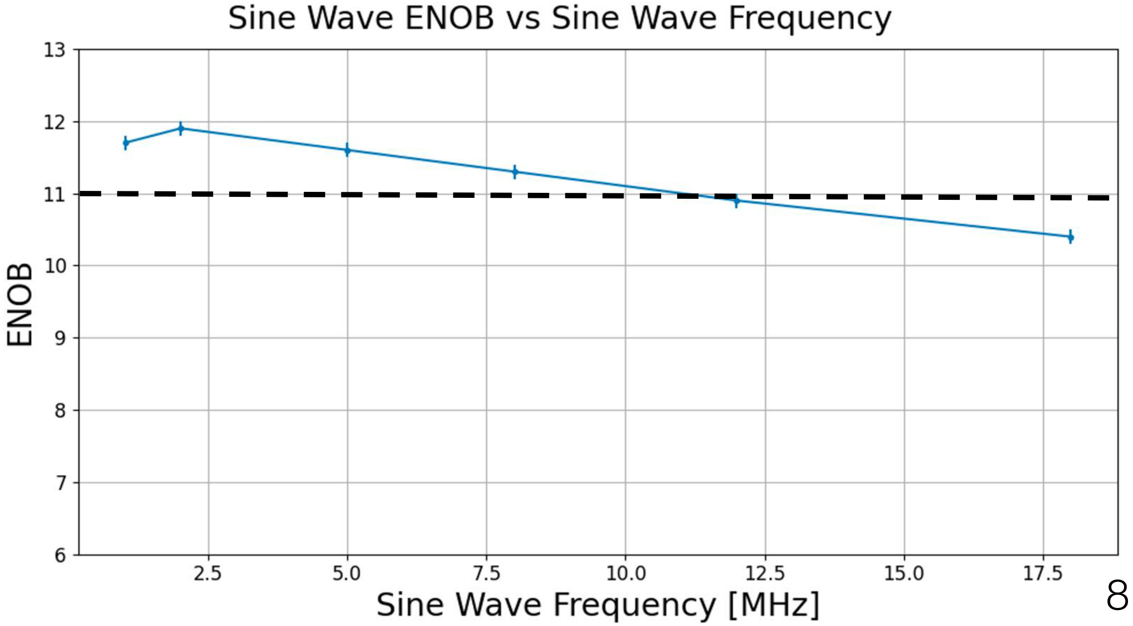
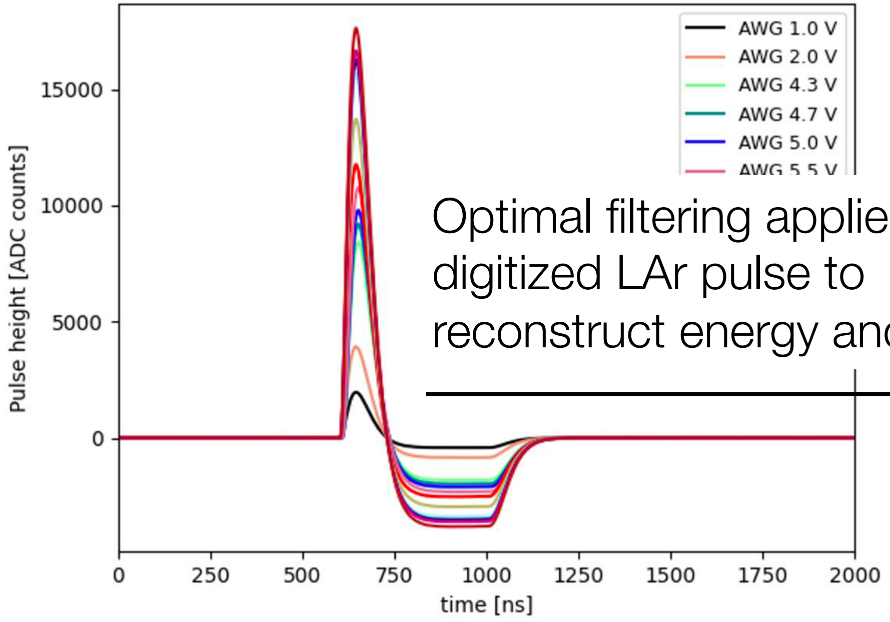


Figure of merit:
ENOB = 11.3
f_{in} = 8 MHz

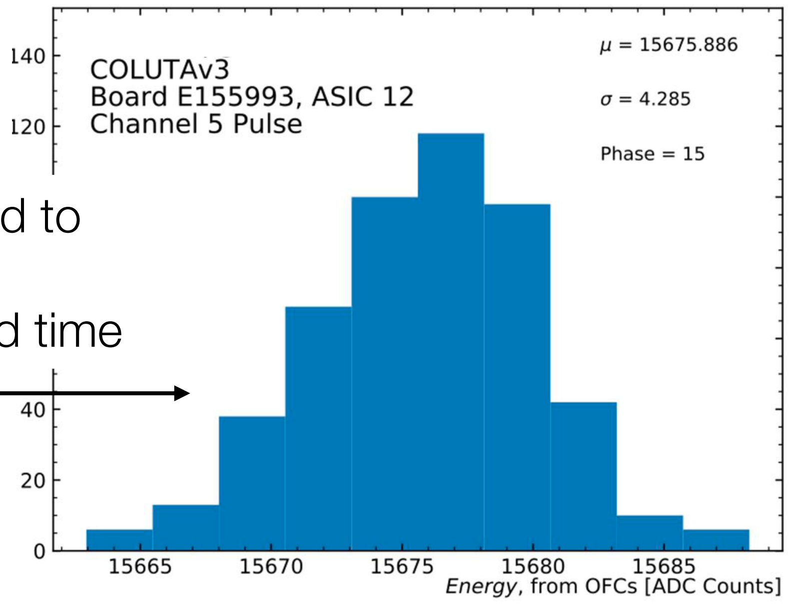


Analog-to-digital converter (ADC)

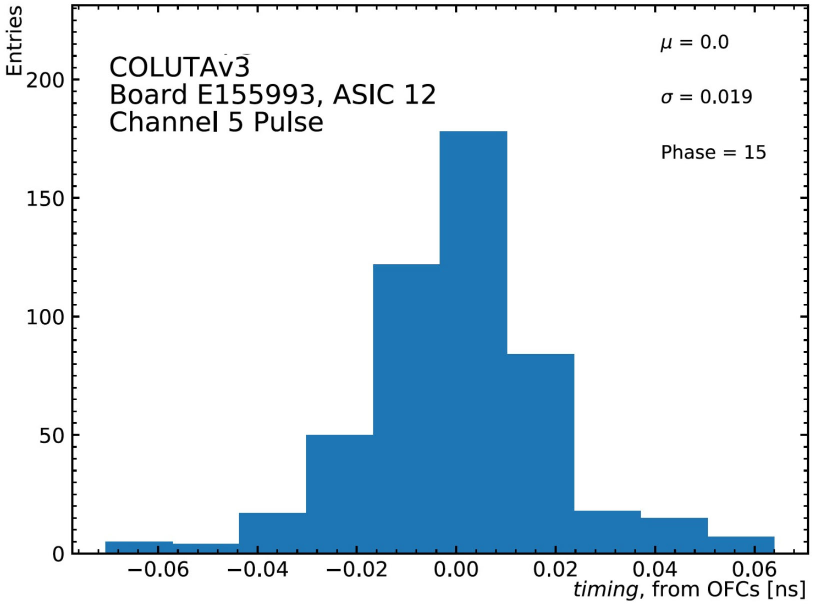


Optimal filtering applied to digitized LAr pulse to reconstruct energy and time

Energy Resolution



Timing Resolution



- Performance measured by injecting a sine wave at different carrier frequencies

Achieve precision of 11.7 and 11.3 bits at 1 & 8 MHz

- 200 kHz sine data and DAC scan used to calculate non-linearity

DNL < ±1.0 15-bit LSB, no missing codes

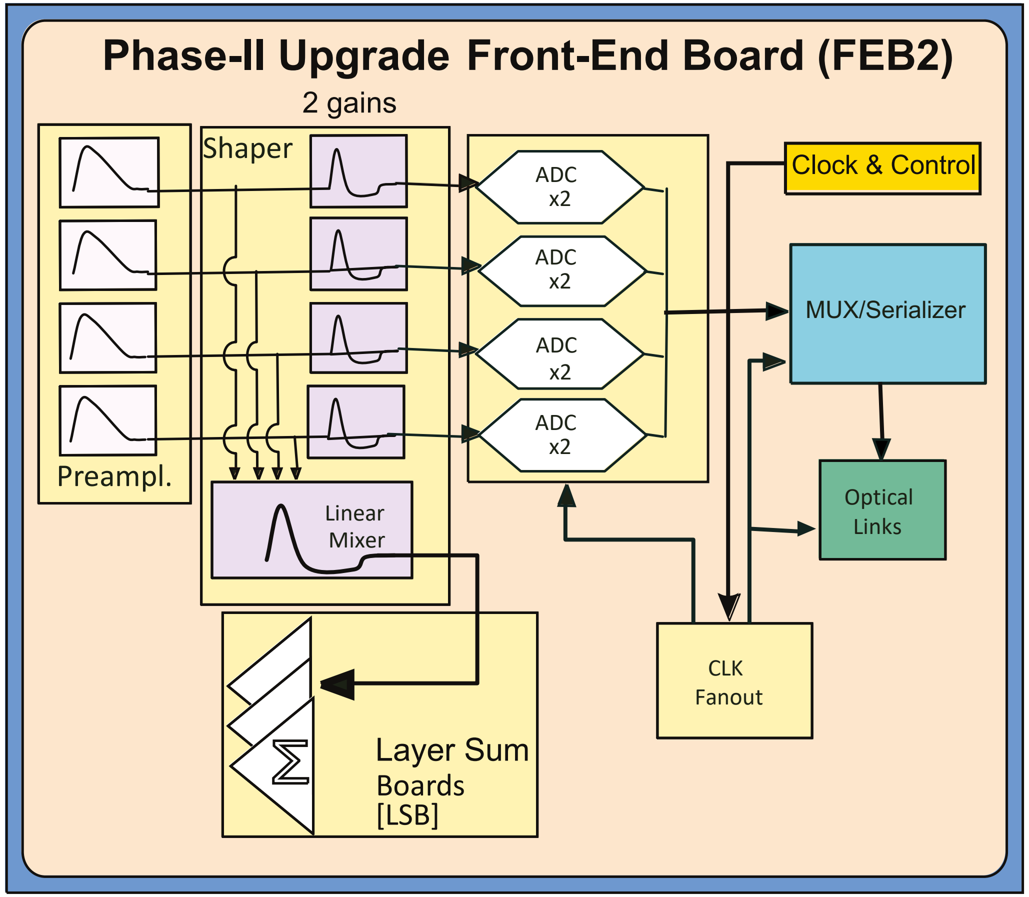
INL < 0.03%

- 30 pulses interleaved to make fine resolution pulse for energy and timing analysis

$\sigma(E)/E = 0.03$ %

$\sigma(t) = 19$ ps

Front-end board (FEB2)



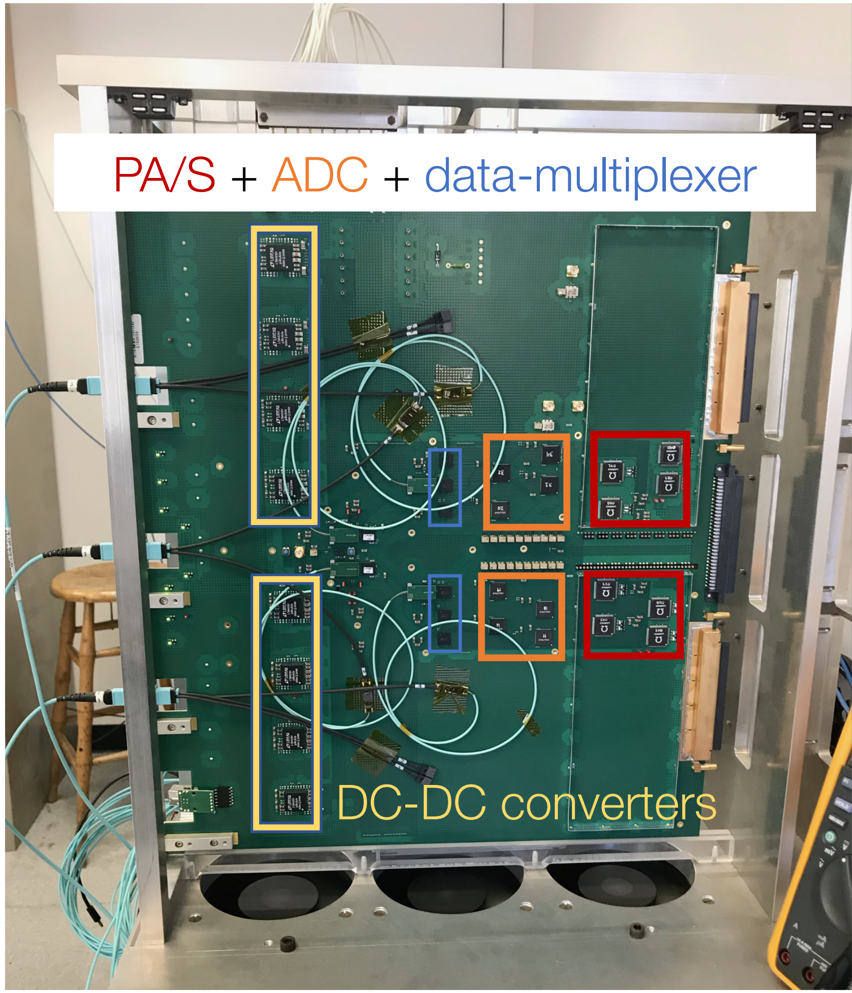
Read out 128 channels per board
Digitize and transmit analog signals over two gains
Provide low-jitter clock distribution, and integrate required control, configuration and monitoring functions
Provide trigger sums through crate baseplane to Phase-I LTDB
Radiation-tolerant to HL-LHC specifications

FEB2 “Slice” Testboard

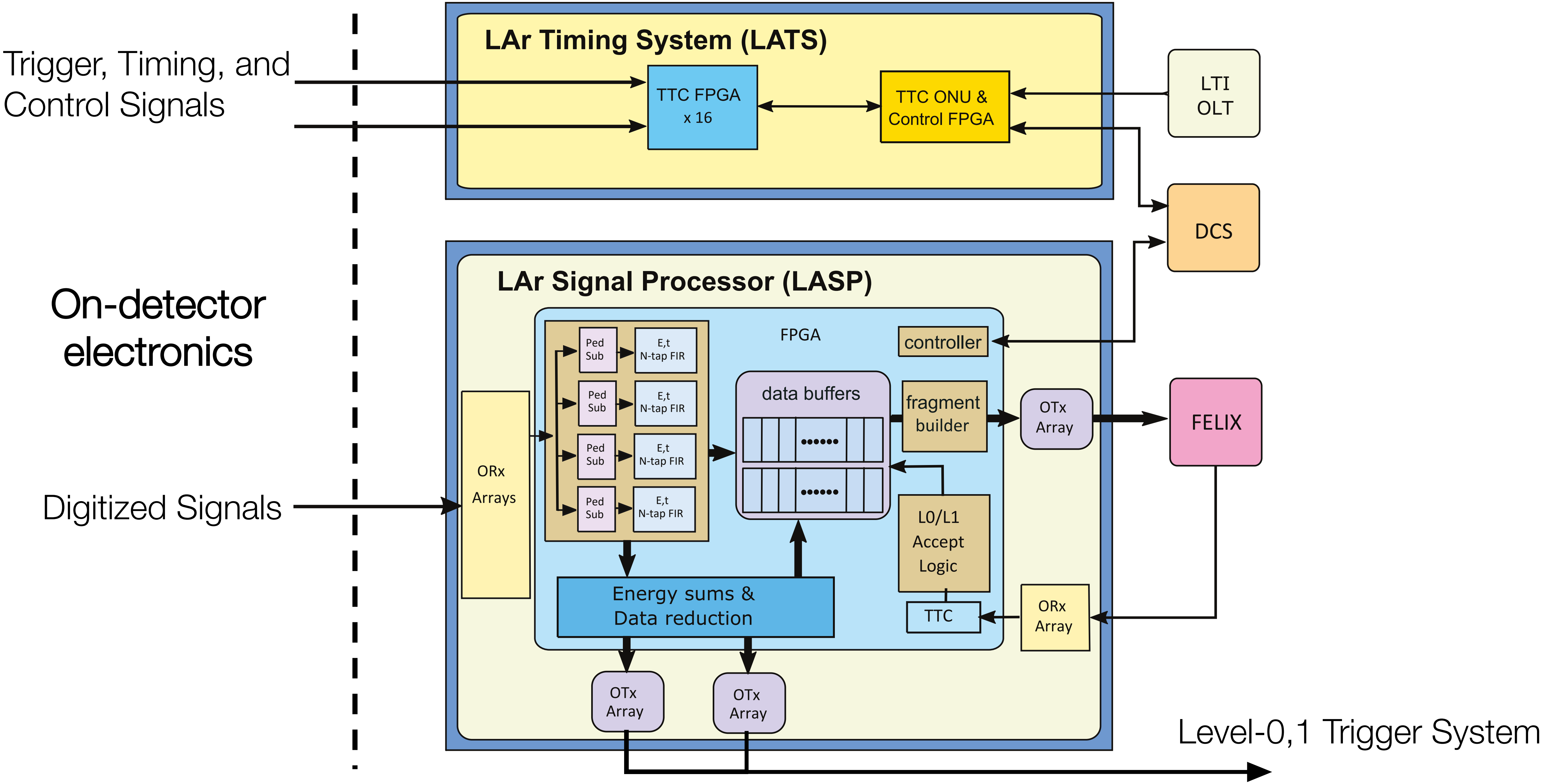
Integration of the on-detector electronics representing ¼ slice of the FEB2

- Full-sized PCB, with layout and density planned for final FEB2
- 32-channel readout and integrating pre-prototype versions of the preamplifier-shaper and ADC, layer sum boards, radiation-tolerant power distribution, optical links for data and control
- Test and evaluate the analog performance achieved with 3 different power options
- Successfully demonstrated full digital functionality, slow control and monitoring, and full redundancy of bi-directional clock and control links
- Full readout chain working:

  Input → PA/S → ADC → data-multiplexer → off-detector electronics



Off-detector electronics



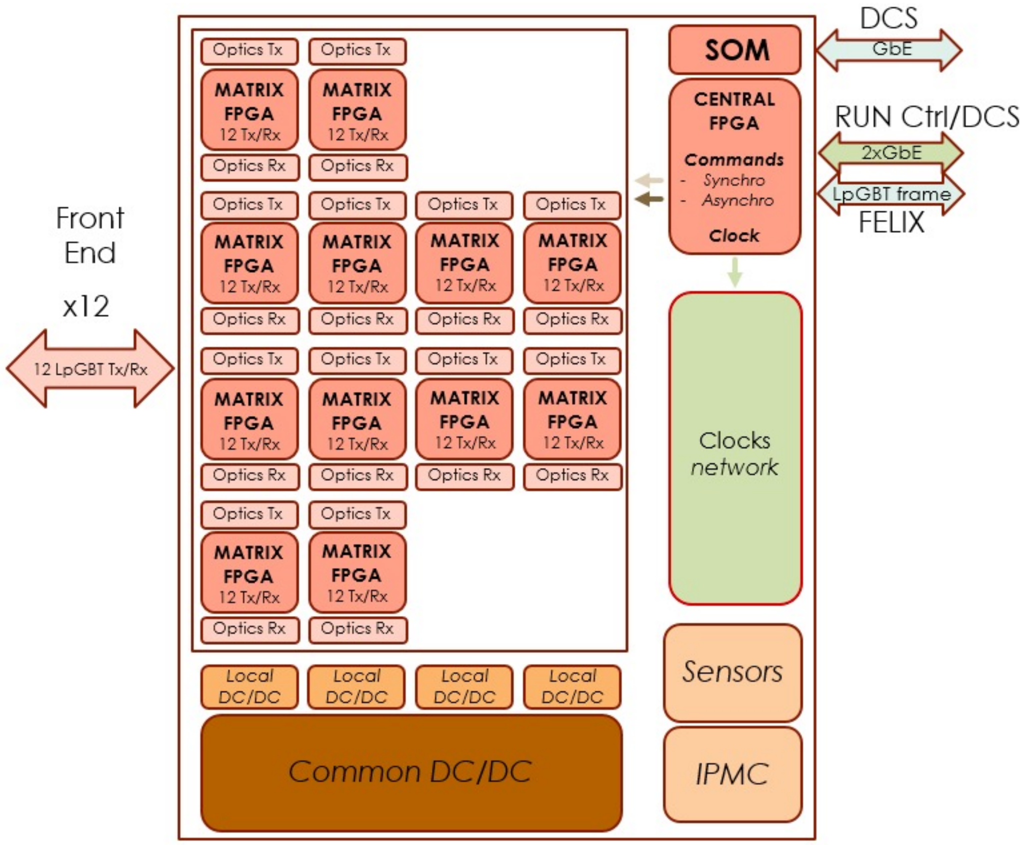
Timing System

Implement Trigger, Timing and Control (TTC)

- Requirements:

  TTC distribution, configuration and monitoring of 1524 FEBs & 122 calibration boards

- Liquid Argon Timing Trigger Control Distribution and Front-End Monitoring (LATOURNETT)
  - Central FPGA (Cyclone 10 GX): connections to FELIX, DCS/RunControl
  - Matrix FPGAs (Cyclone 10 GX): connections to front-end electronics
  - System on Module (SOM): embeds OPC UA, Linux distribution
  - IPMC: read critical sensors

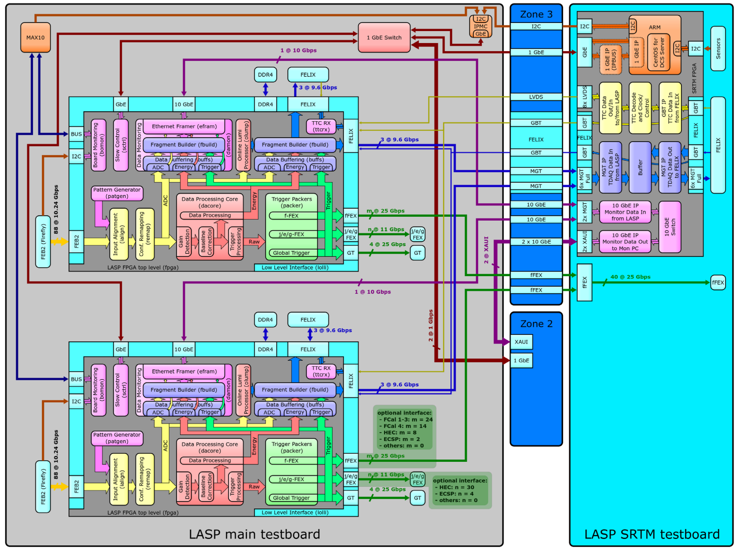


Signal Processing

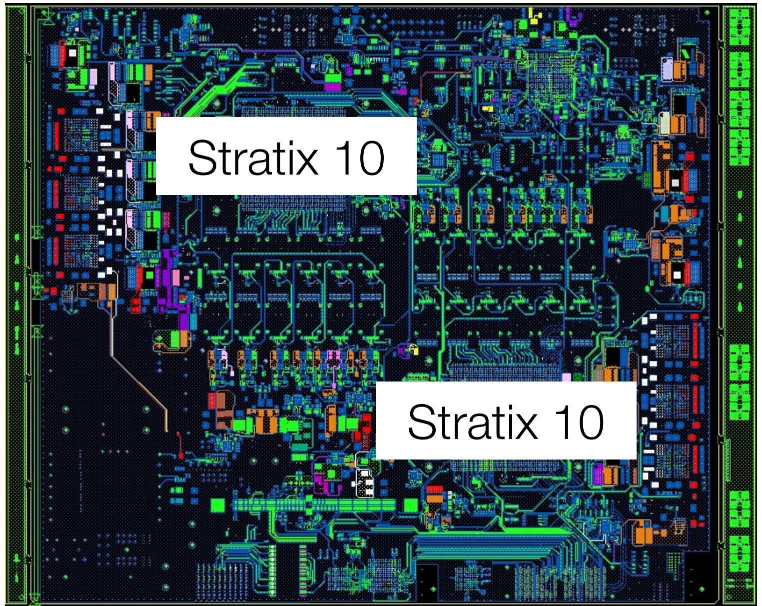
Receive the digitized waveforms, apply digital filtering, buffer and transmit data to the trigger and data acquisition (TDAQ) systems

- Requirements:

  Determine precision energy and deposition time for each calorimeter cell



- Liquid Argon Signal Processor (LASP)
  - Two main components: main blade + Smart Rear Transition Module (SRTM)
  - Each FPGA receives input from 512 front-end channels (4 FEBs) and outputs data to TDAQ @ 25 Gbps
  - LASP firmware development (targeting Intel Stratix 10) well underway
  - LASP test board design complete with full functional capability



Summary and Outlook

- For HL-LHC, LAr calorimeter will upgrade both on-detector and off-detector electronics
  - Calibration, analog readout, signal processing, trigger and timing systems will be upgraded in preparation for HL-LHC era
- Most of the ASICs developed for the HL-LHC upgrade are in prototype design stage
- Integrating early and often our on-detector and off-detector electronics
  - Slice Testboard demonstrates full digital functionality, slow control and monitoring, and full redundancy of bi-directional clock and control links
- Closely monitoring global chip shortages and foundry access issues

Despite the pandemic, still on track for installation during 3rd long shutdown with solutions found to continue testing the devices

Thank you!

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*Mittelhorn-Schreckhorn-Eiger panorama

Backup Slides

Radiation tolerance specifications

	TID [Gy]	**NIEL [n_{eq}/cm^2]**	**SEE [h/cm^2]**
ASIC	$8.61 \times 10^2 \pm 3.88 \times 10^1$ (1.5)	$2.13 \times 10^{13} \pm 1.63 \times 10^{11}$ (2.0)	$3.51 \times 10^{12} \pm 4.35 \times 10^{10}$ (3.0)
ASIC w/ safety factors	12.9×10^2	4.30×10^{13}	10.5×10^{12}

Safety Factor and Testing Procedure Recommendations of the Radiation Effects Task Force

FEB2 "Slice" Testboard

Slice Testboard Layout