Low Background Readout Electronics for
Large Area Silicon Photomultipliers

Andrea Fabbri on behalf of Roma Tre group
Outline

- Front end board design
- Readout scheme
- Readout controller
- Test setup
- Performances
Future experiment needs

• New generation astroparticles experiments requires:
  • High photodetection efficiency
  • High dynamics
  • Low background materials
  • Long term stability

• SiPM devices:
  • High PDE > 50%
  • Single photon counting capability
  • High Fill Factor (squared devices)
  • Should work at low temperature to reduce Dark Count Rate

• A dedicated electronic readout for SiPM should be:
  • Robust
  • Reliable at low temperature
  • Should have high timing and energy resolution
Proposed Front End Board Design for a SiPM-based detector

TIAs split SiPM capacitance to improve signal SNR.

TIA outputs added on a single analog output to reduce channel number in a large area experiment.
Proposed Front End Board Design for a SiPM-based detector

- Reference tile: 5 cm x 5 cm, made by an 8 x 8 array of 6 mm x 6 mm SiPMs
- Series/parallel connection allows to manage capacitance from SiPMs. Connection can be done on SiPM tile PCB or on FEB.
- SiPM elements of a tile can be split on 4 Transimpedance Amplifier. More TIA can be added to reduce input capacitance.
- Two gain stages to reduce TIA instability.
- 2Vpp output dynamic from the second stage adder.
- It works at -70°C degree.
- Low background PCB was tested (Piralux, Aramid).
Front End Board with differential output

ADC Driver stage added for differential output \(\rightarrow\) ensure 20 meter cables between FEB and FEC
FEB Dynamic Range

- Gain can be adapted by change TIA and Adder feedback resistors

- Single P.E. maximum amplitude ~ 8 mV
- 0V-2V output linearity range
- Dynamic Range 1 – 250 p.e.
Shaping time can be fine tuned by changing the resistor value according to the SiPM input capacitance.
FEB reliability

Longest run @ -50°: 8 days
Integrated days @ -50°: 65 days
Number of cycles +20°/-50°: ~100
Number of FEB prototypes: ~20
Number of failures: 0
Several run @ -70°

<table>
<thead>
<tr>
<th>Capacitor Ceramic</th>
<th>Value (µF)</th>
<th>OpVolts / RtdVolts</th>
<th>Lb</th>
<th>Pt</th>
<th>Pc</th>
<th>Pβ</th>
<th>Pβr</th>
<th>Pq</th>
<th>Pe</th>
<th>Lp [FIT]</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,00E-11</td>
<td>0,55</td>
<td>0,00099</td>
<td>0,01</td>
<td>0,10</td>
<td>1,77</td>
<td>1,00</td>
<td>0,10</td>
<td>15</td>
<td>0,00</td>
<td>OPA</td>
<td></td>
</tr>
<tr>
<td>1,00E-08</td>
<td>0,55</td>
<td>0,00099</td>
<td>0,01</td>
<td>0,12</td>
<td>1,77</td>
<td>1,00</td>
<td>0,10</td>
<td>15</td>
<td>0,01</td>
<td>OPA</td>
<td></td>
</tr>
<tr>
<td>1,00E-07</td>
<td>0,55</td>
<td>0,00099</td>
<td>0,01</td>
<td>0,23</td>
<td>1,77</td>
<td>1,00</td>
<td>0,10</td>
<td>15</td>
<td>0,01</td>
<td>bypass OPA</td>
<td></td>
</tr>
<tr>
<td>2,20E-07</td>
<td>0,55</td>
<td>0,00099</td>
<td>0,01</td>
<td>0,25</td>
<td>1,77</td>
<td>1,00</td>
<td>0,10</td>
<td>15</td>
<td>0,01</td>
<td>bypass HV</td>
<td></td>
</tr>
</tbody>
</table>

**Wafer Fabrication Data**

<table>
<thead>
<tr>
<th>MTBF (Mean Time Between Failure)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TOTAL FIT</strong></td>
</tr>
<tr>
<td><strong>MEAN TIME BEFORE FAILURE (HOURS)</strong></td>
</tr>
<tr>
<td><strong>MEAN TIME BEFORE FAILURE (YEARS)</strong></td>
</tr>
</tbody>
</table>

**Analog Design**
FEB test setup

- A very simple and fast system can be implemented to test and characterize FEBs with a simple microcontroller

Test Setup

TIAs

TIA Linearity test results using pulse generator
An Example Front End Board connection to SiPM Tiles
ADC + FPGA Controller for uTCA

Prototype system:
- ADC board with AD9083
- FPGA controller (Kintex7)
- Ethernet connection with PC
- Can be moved to uTCA crate

- 250 Msample/sec ADC, 125 MHz bandwidth
- 16 channels
- Differential 2 Vpp input
- JESD204B interface
- Dedicated Input for shared clock between board

- Extremely high data transmission, 10 Gb/s per port & 40 Gb/s per link
- Hot-swap capability ensures uninterrupted operation
- Rear I/O (useful with multiple cable connections)
- Redundancy is available: connection, logical bus, power, cooling
- Dedicated Module for synchronization (White Rabbit)
Test setup
Test setup
Test setup
Front End performances: timing

Data acquired with an FPGA controller, charge and time (filtering, fitting...) are evaluated online by devoted firmware.

Time distribution of the two SiPM signals coming from the same laser pulse
Front End performances: 1.7 mm² SiPM

S.E.R. = 3.74%
Laser @20 kHz

S.E.R. = 9.18%
Laser @500 kHz

S.E.R. = 3.08%
Laser @20 kHz

S.E.R. = 6.70%
Laser @500 kHz
Front End performances: 36 mm² SiPM

SER Spectrum FILT. WF ch. 0
S.E.R. = 5.13%
Laser @200 kHz

SER Spectrum FILT. WF ch. 1
S.E.R. = 4.29%
Laser @200 kHz

SER Spectrum FILT. WF ch. 2
S.E.R. = 4.03%
Laser @200 kHz

SER Spectrum FILT. WF ch. 3
S.E.R. = 4.44%
Laser @200 kHz
Front End performances with large area SiPM tile

2.5 cm x 2.5 cm tile @-50° (+4V OV)

S.E.R. = 9.7%

5 cm x 5 cm tile @-50° (+4V OV)

S.E.R. = 19.02%
Conclusion

• A very flexible electronics, based on Commercial On The Shelf (COTS) components has been presented:
  • High dynamic range
  • High reliability
  • Single photon counting capabilities
  • High performances in terms of energy and time resolution
  • Large area SiPM readout capabilities

• Well suited for the next generation astroparticle experiments