Upgrade of the ATLAS Monitored Drift Tube Frontend Electronics for the HL-LHC

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May 27th, 2021
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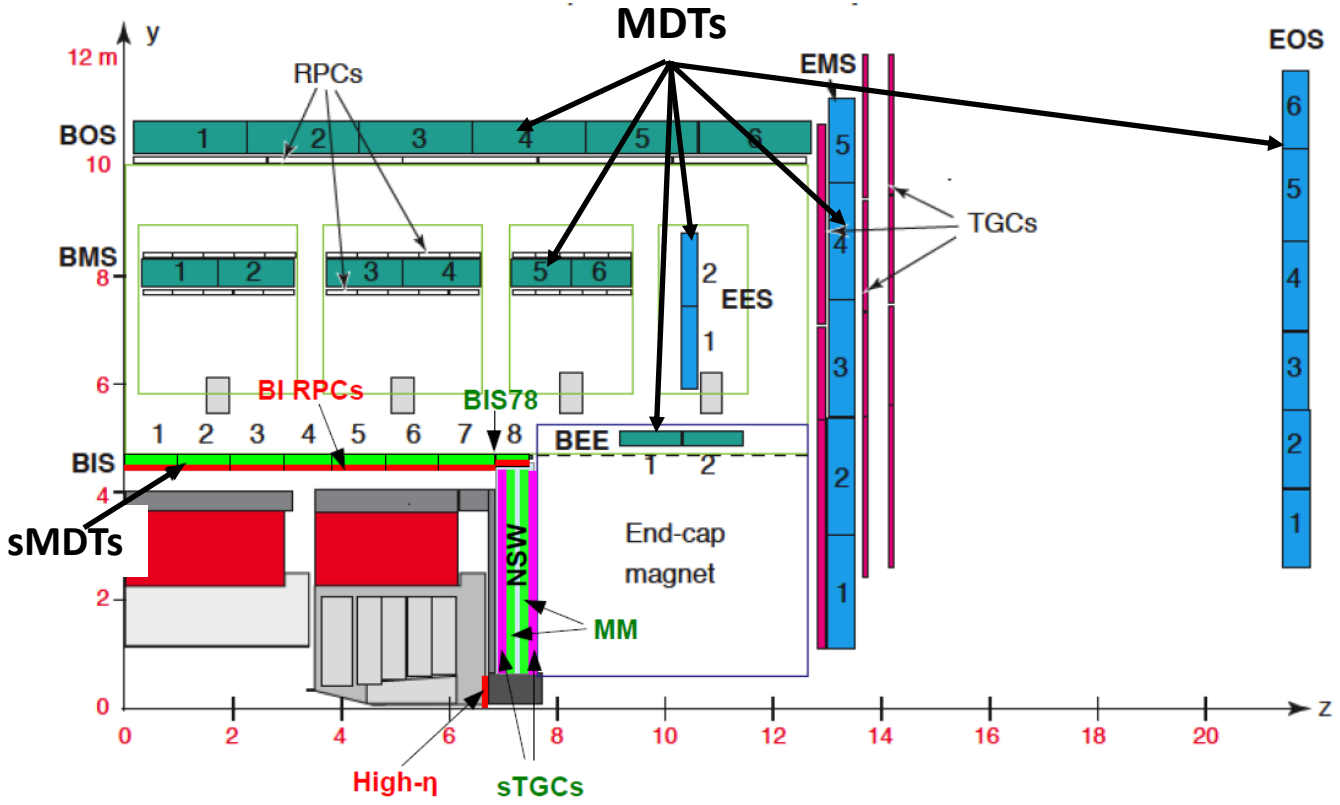
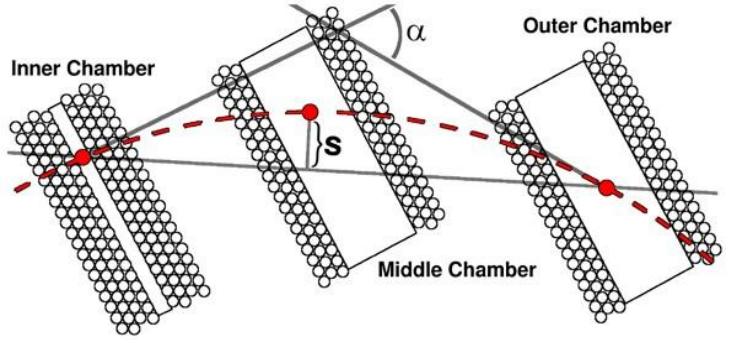
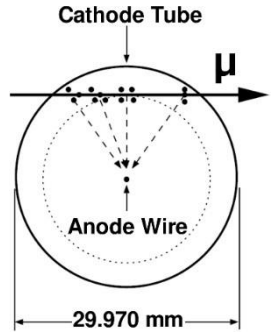
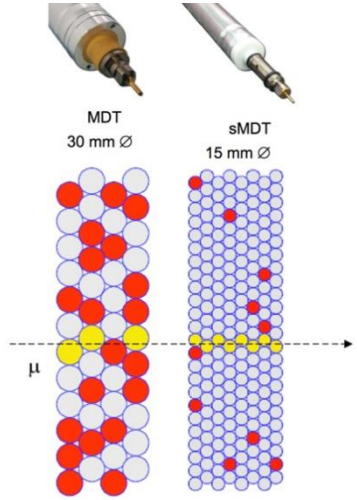
ATLAS Monitored Drift Tube (MDT) detector





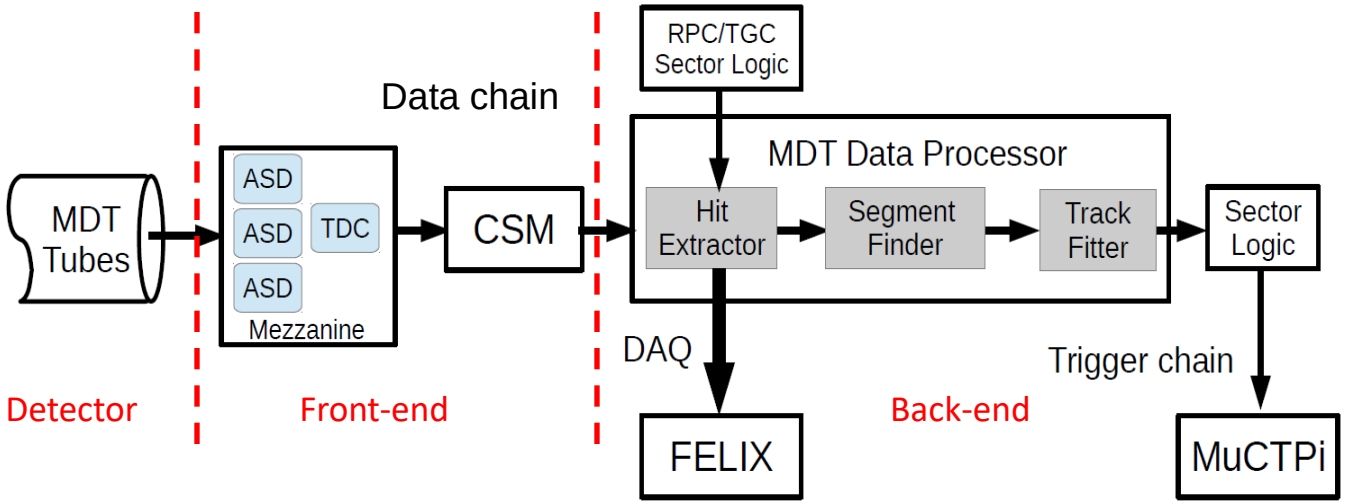




- ATLAS muon spectrometer is used for muon triggering, identification and momentum measurement;
- Provides a standalone transverse momentum measurement (10% at 1 TeV), mainly by the Monitored Drift Tube (MDT) chambers;
- 1150 chambers with 354k tubes covering an area of 5500 m^2.

MDT Frontend Electronics Upgrade

- Before upgrade: precise position readout
- Phase II upgrade: precise position readout and trigger (requires triggerless readout)
- MDT electronics needs to cope with the new ATLAS Trigger and DAQ scheme



Block diagram of the MDT trigger and readout electronics for HL-LHC runs

Amplifier, Shaper and Discriminator (ASD)

- Analog ASIC
- Lower peaking time delay
- larger sensitivity and higher SNR for a minimum charge of 5fC

Time-to-Digital Conveter (TDC)

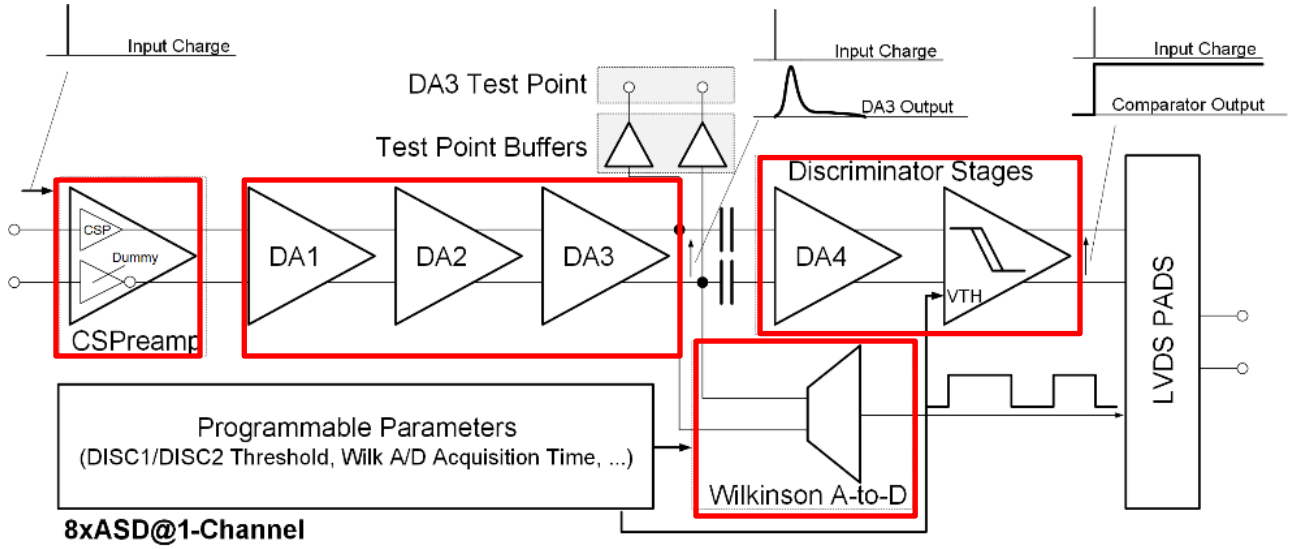
- Digital ASIC
- Triggerless mode
- 80 Mbps (before upgrade) -> 320 Mbps x 2

Chamber Service Module (CSM)

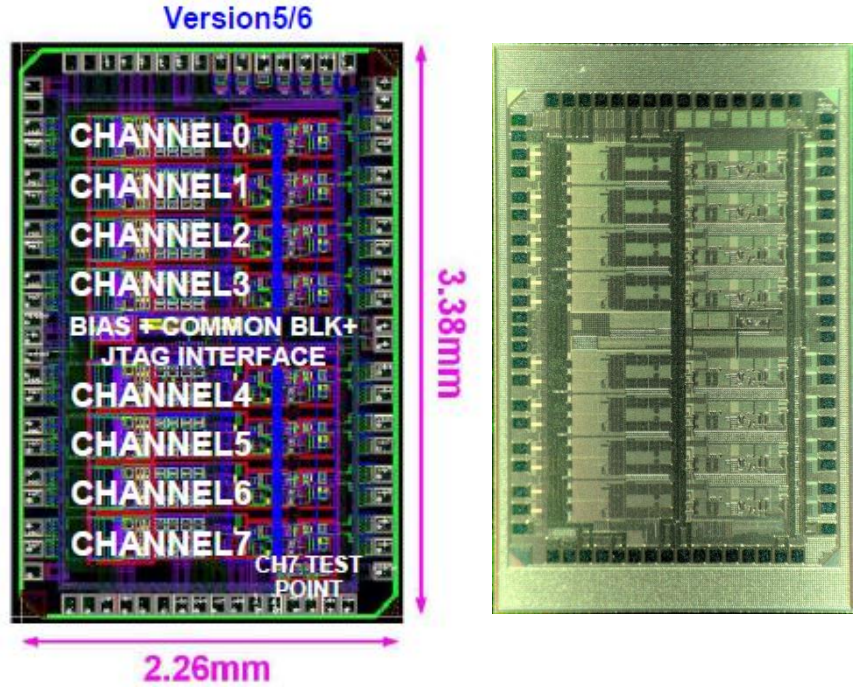
- Multiplexer board
- Low-power Gigabit Transceiver (lpGBT)
- 2 Gbps (before upgrade) -> 10.24 Gbps x2

Upgrade of the ASD ASIC

- 8 channels per ASD chip, IBM 130nm CMOS technology
- Charge sensitive preamplifier, 3-stage shaping circuit, discriminator stage and a Wilkinson ADC to convert input charge to a digital pulse
- LVDS output driver (reduced swing)
- Global programmable parameters for discriminator threshold and charge gain control



ASD Channel Block Scheme*



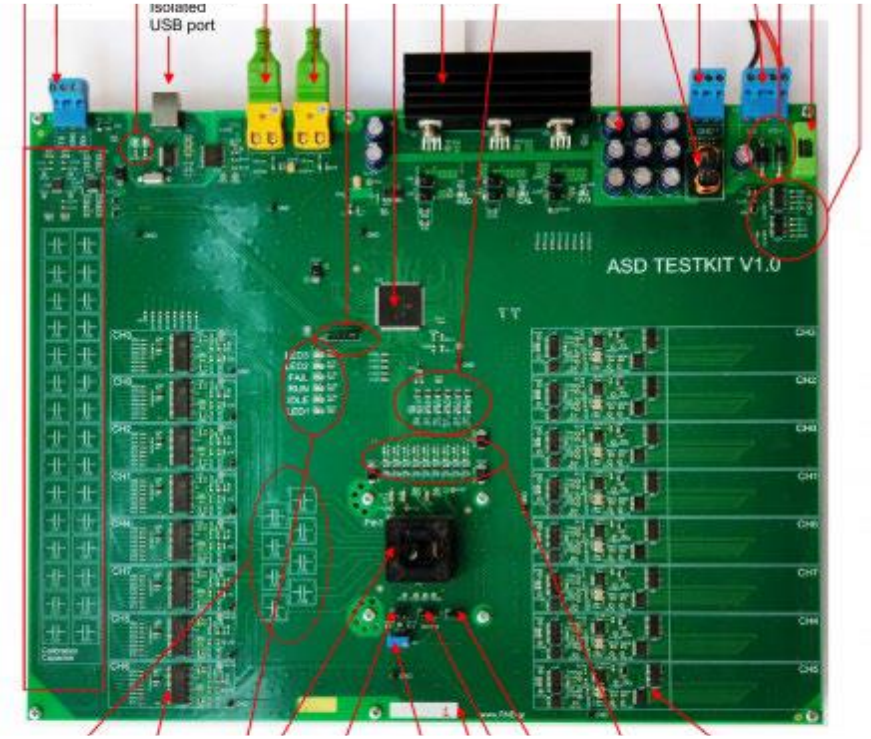
ASD Layout and microscope photo**

*M. De Matteis et al., Performance of the new Amplifier-Shaper-Discriminator chip for the ATLAS MDT chambers at the HL-LHC, Journal of Instrumentation 11.02 (2016): C02087

**R. Richter et al., Performance of the production prototype, Final Design Review of the ASD for MDT readout in Phase-II, June 25 (2018)

Upgrade of the ASD ASIC

- ~7.5k preproduction chips produced and packaged (with QFN88) in 2019
- A sample of 2k chips tested manually with the LMU chip tester (1k at MPI and 1k at LMU) and confirmed the 92.4% yield rate observed in the preproduction
- Lower peaking time delay, larger charge sensitivity
- ~83k produced ASD chips (packaged) delivered at the end of Jan 2021
- Automatic testing of all chips at a company planned for June 2021



ASD chip tester

Reason for rejection	Fraction
Chip not operable	0.10%
Bad LVDS output levels	0.90%
Abnormal total current	0.40%
Large threshold spread	1.00%
Dead channels	2.60%
Bad ADC measurements	2.60%
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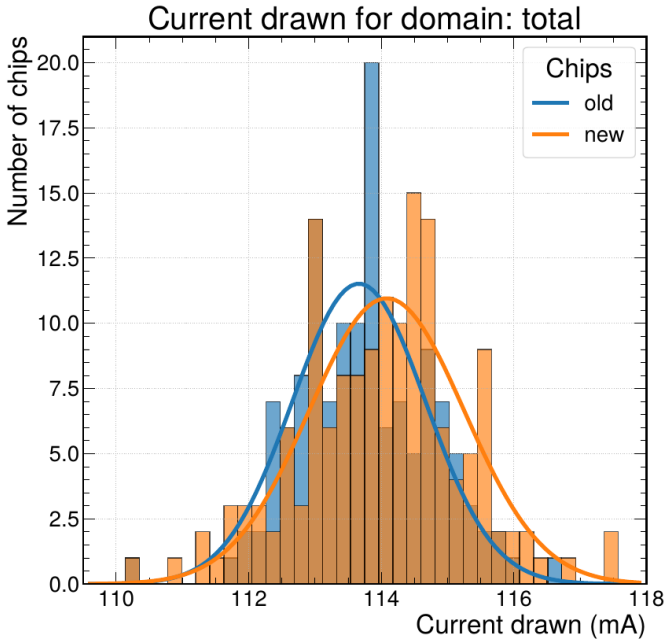
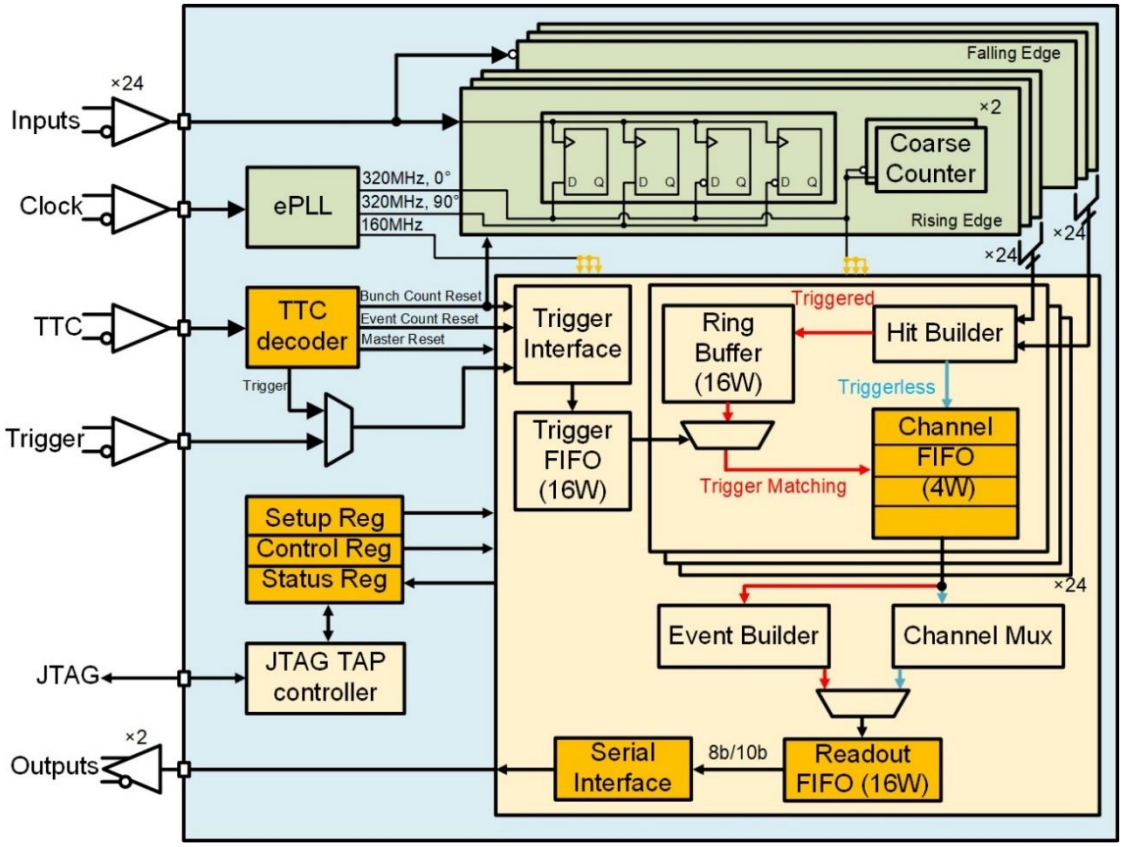
total	7.60%



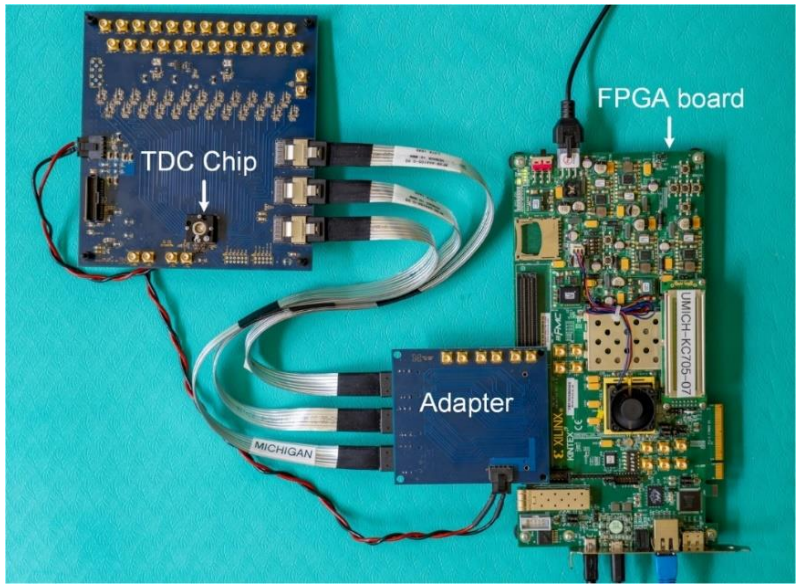
Upgrade of the TDC ASIC



TDCv2 overall block diagram*

- 24 channels per chip, TSMC 130nm CMOS
- 780 ps binsize, 102 us dynamic range
- Triggerless mode by default
- 320 Mbps x2 output data rate
- Implemented TMR protections for all configuration registers, key modules and clock trees

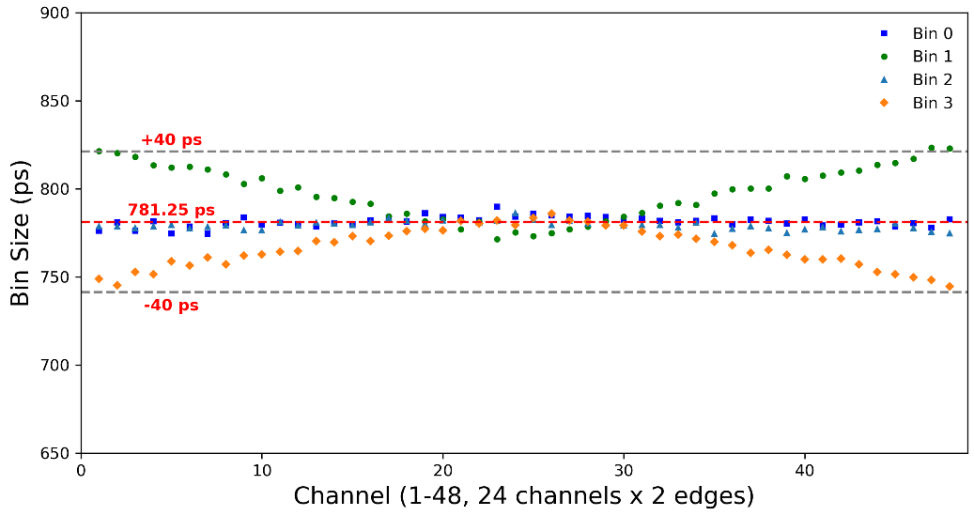
TDCv2



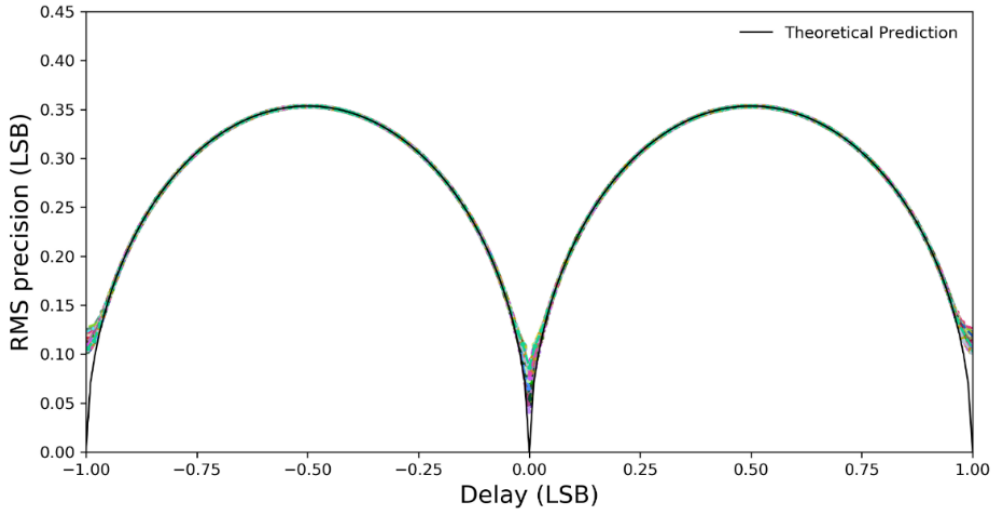
TDCv2 test platform

*Y. Guo et al., Design of a Time-to-Digital Converter ASIC and a mini-DAQ system for the Phase-2 upgrade of the ATLAS Monitored Drift Tube detector, NIMA vol 988 (2021): 164896

Test results of the TDC ASIC

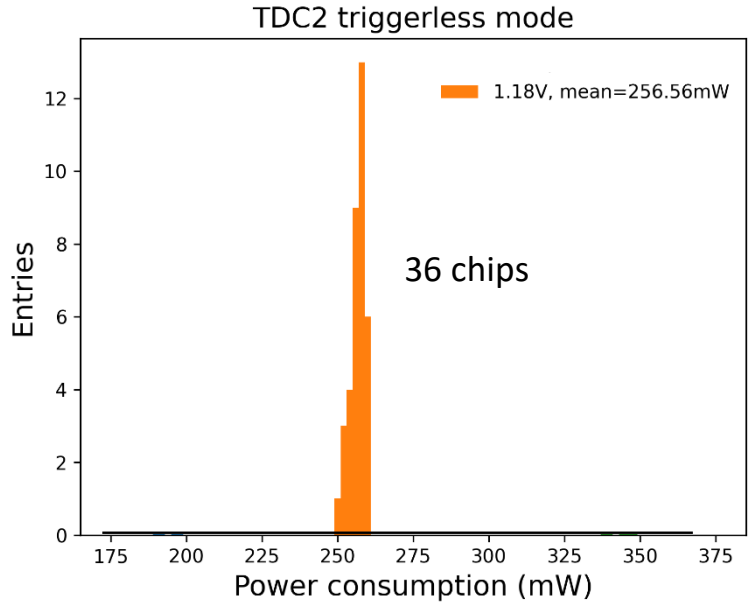


Fine-time bin size of 1 TDC (±40 ps)



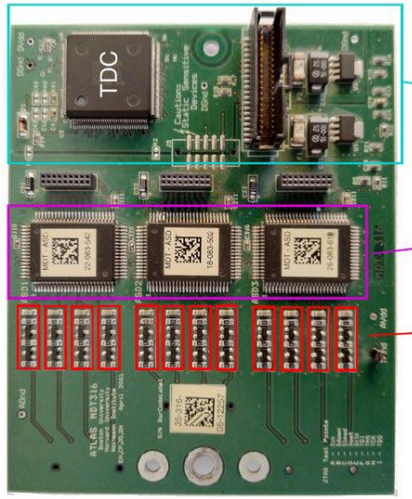
Timing resolution (RMS) of 1 TDC (80 ps at 0 delay)

- 100 prototype chips produced and 36 packaged (with BGA144) in Jan 2020
- No rejection for all 36 packaged chips
- Plan to have the TDC final design review this June after we finish irradiation tests at Fermilab and cosmic ray studies at CERN's GIF++

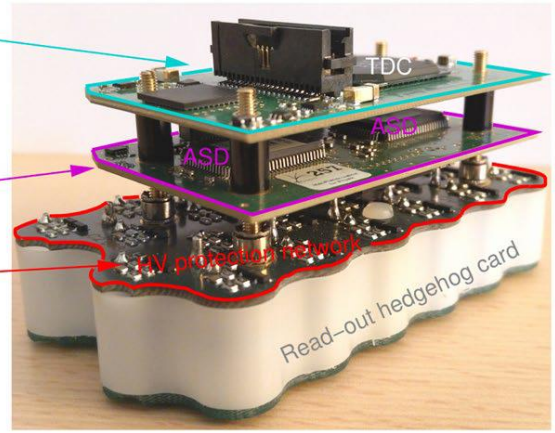


Upgrade of the mezz card

- 4 types of boards (MDT316, MDT436, MDT446, stacked mezz for sMDT) to fit different chamber layouts
- Preliminary designs of all mezzanine card types are ready
- Prototypes for all types exist and have been tested successfully
- Design can be finalized after LDO irradiation tests (TID and SEE)
- sMDT mezz cards are needed for integration and commissioning of sMDT chambers on surface around Jan 2023, MDT mezz cards are needed after Jan 2025

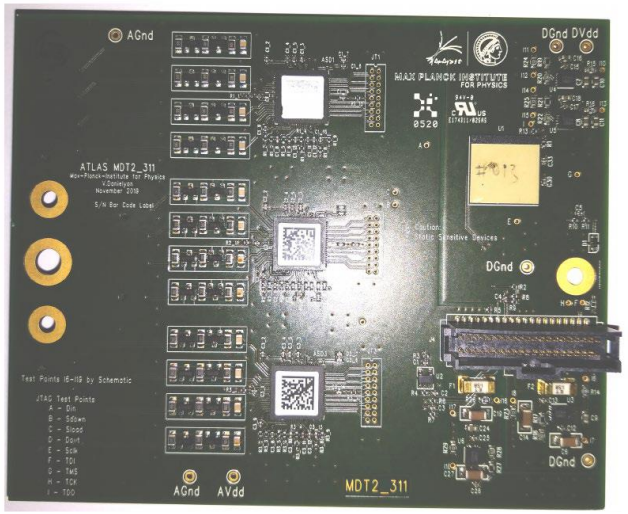


MDT mezzanine

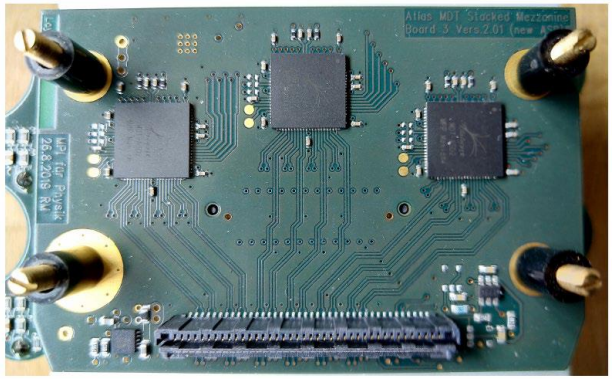


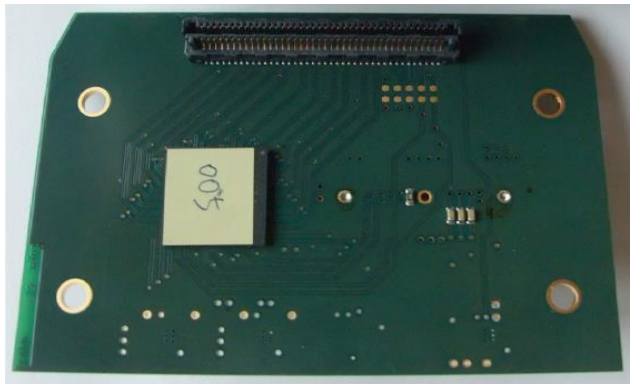
sMDT stacked mezzanine

Prototype MDT mezzanine card



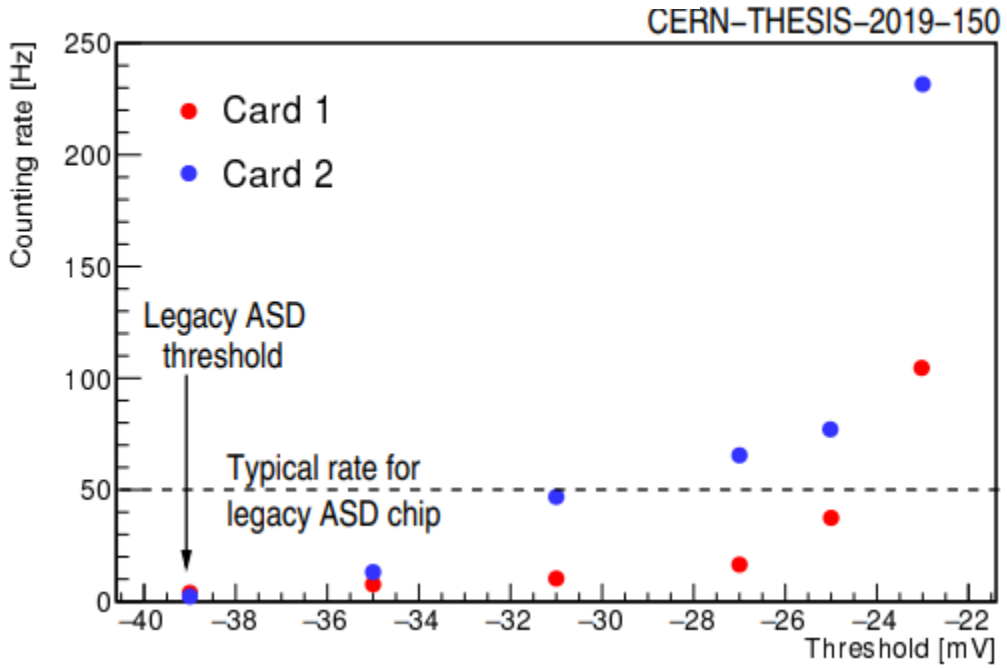
Prototype BIS sMDTmezzanine cards (ASD and TDC boards)



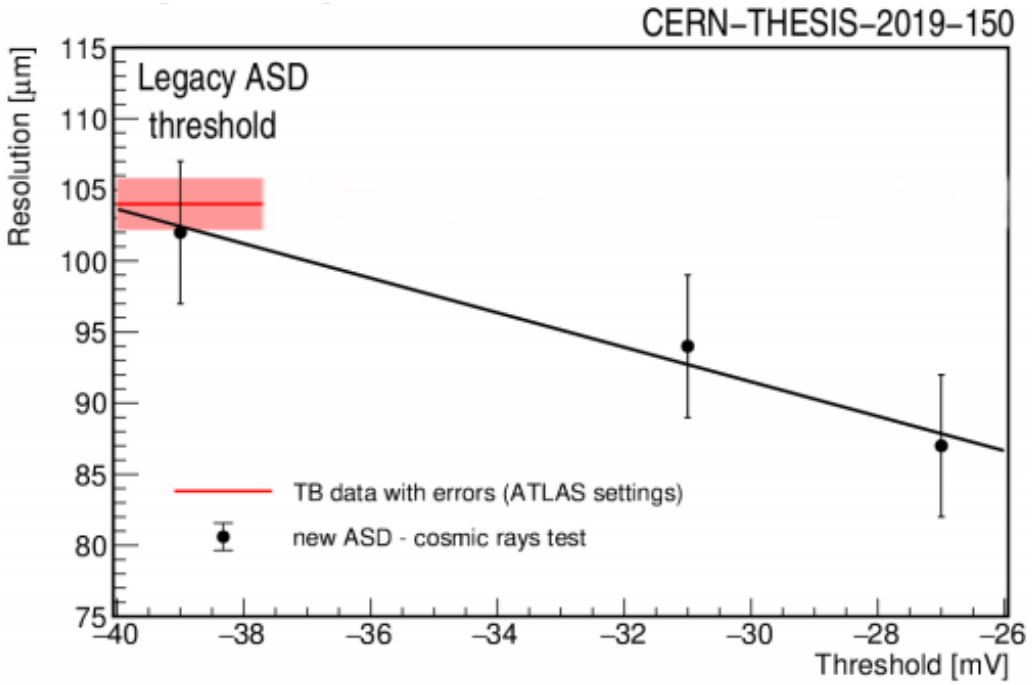


Upgrade of the mezz card

Accidental hit rate with new ASD



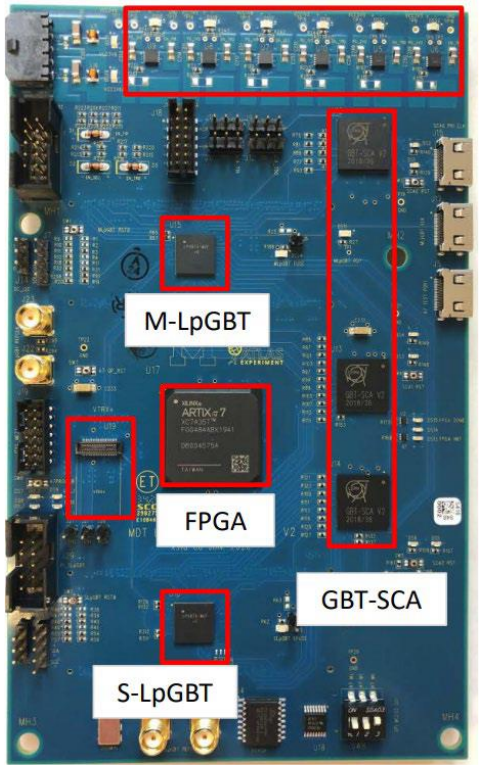
Average single tube resolution with new ASD (cosmic rays)

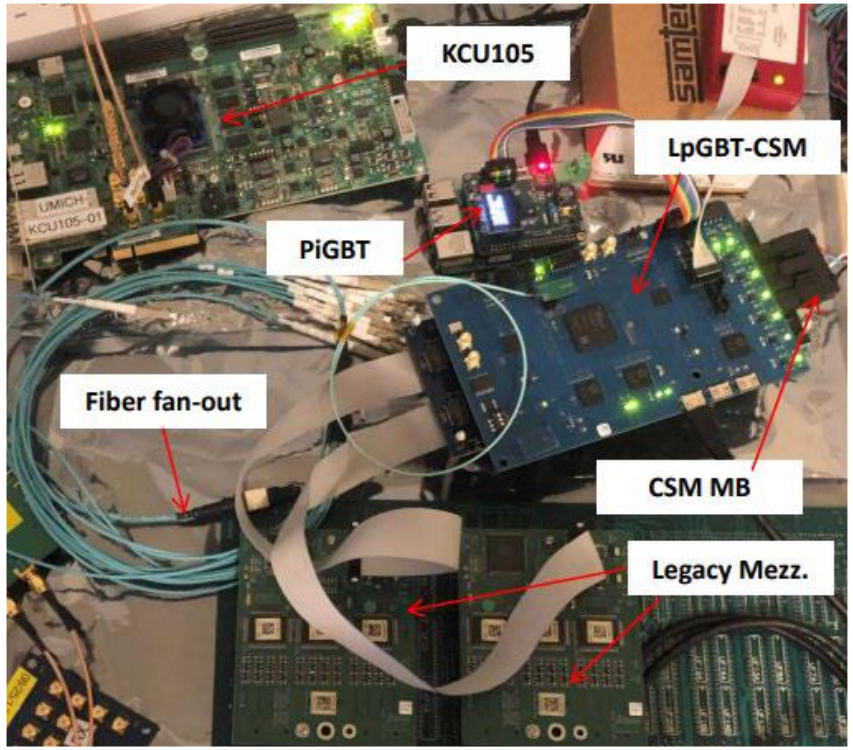


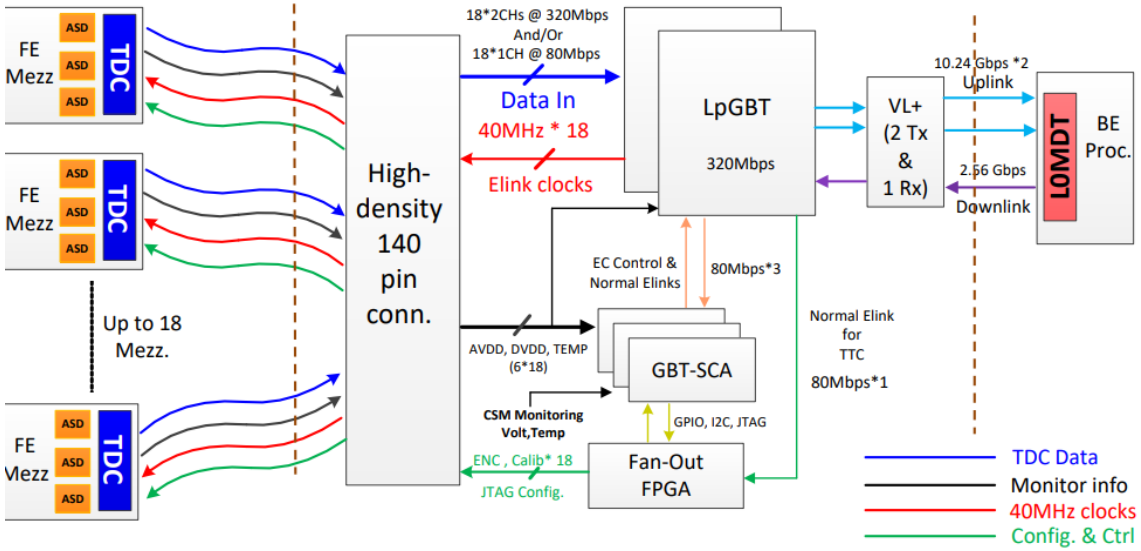
- Compared to the legacy ASD, significantly lower accidental hit rate with the new chip at the same discriminator threshold
- Operation of the new ASD with 10 mV lower threshold than the legacy chip possibly leads to a 20 µm better spatial resolution at the same accidental hit rate

Upgrade of the CSM board

- V2 prototype designed using lpGBT (low power GigaBit Transceiver, CERN)
- 18-TDC multiplexer, 10.24 Gbps output line x2
- Detailed standalone tests and joint tests with legacy mezzcards and new mezzcards performed
- CSM data successfully decoded by the KCU105 evaluation board
- Radiation tests for Artix7 FPGA planned (TID test at BNL and SEE test at LANSCE)

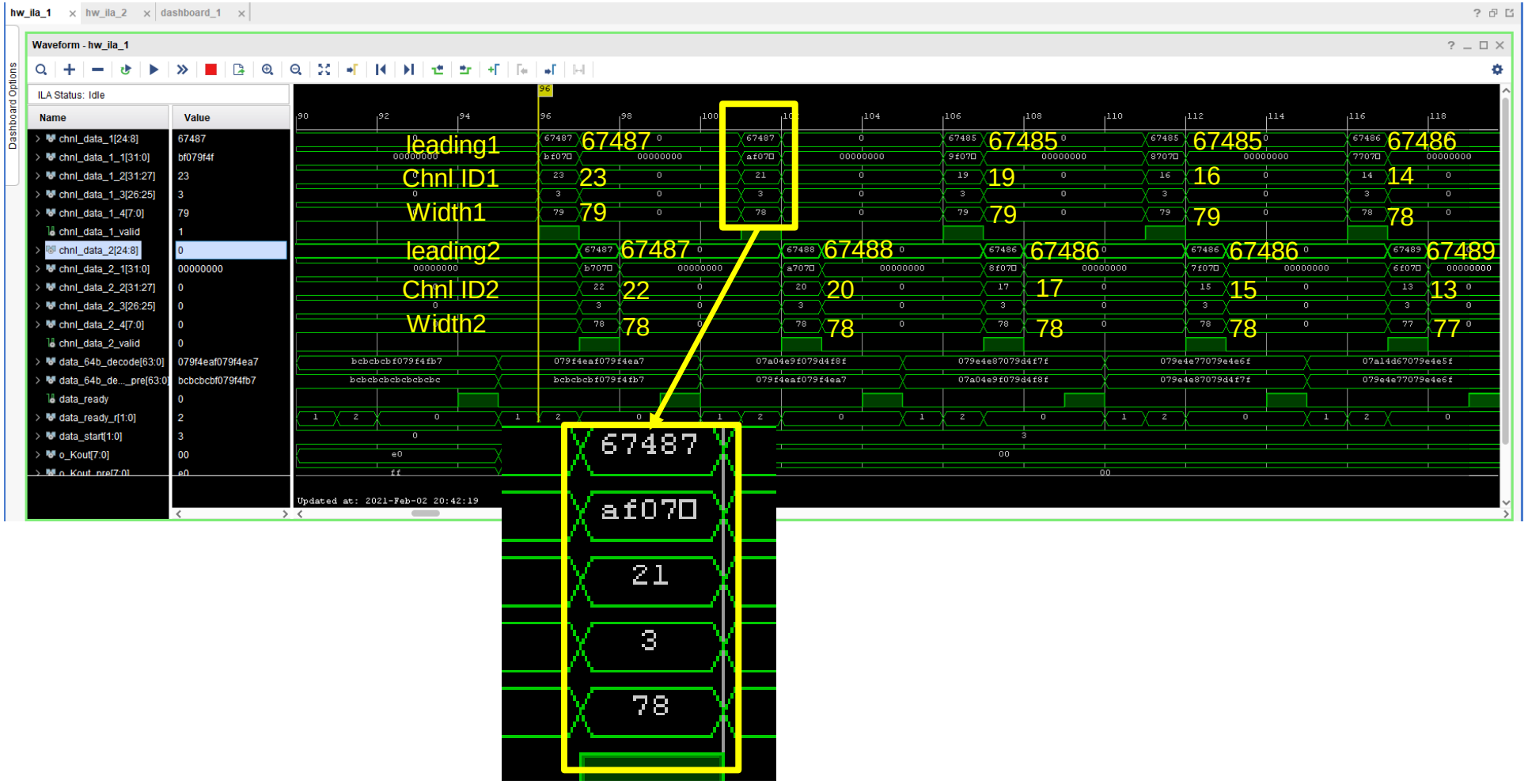






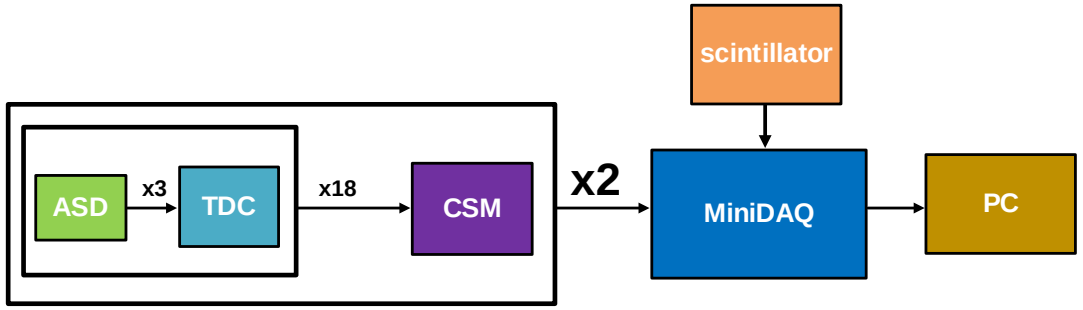
Upgrade of the CSM board

- Simultaneous hits sent to 24 channels, width = 62.5ns (80 LSB)
- Channel ID, leading edge, pulse width are decoded correctly

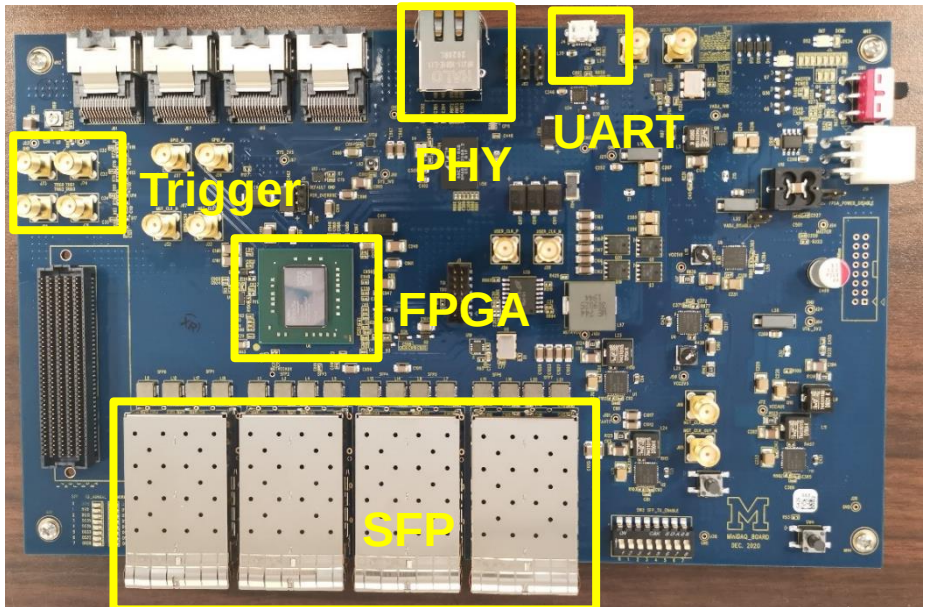


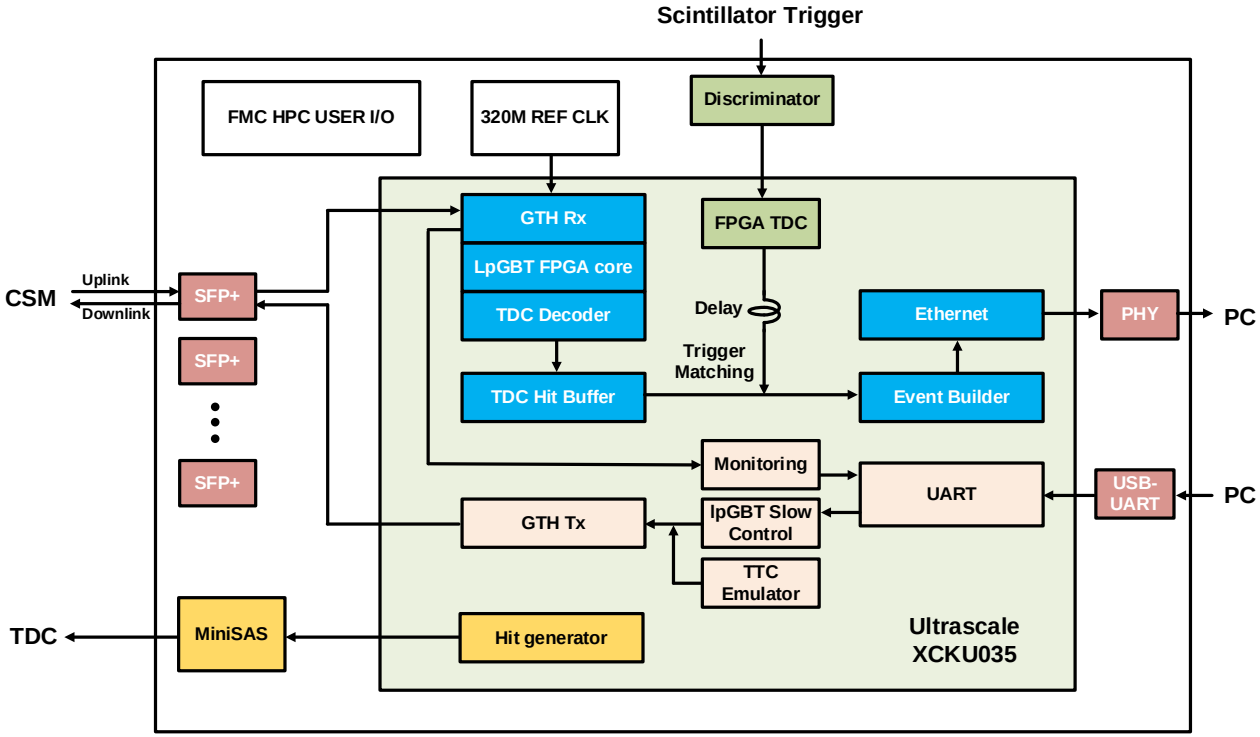
Design of a miniDAQ system

- MDT Data Processor (L0MDT) not available now
- Test of all new frontend electronics (ASD+TDC+Mezz+CSM) on a newly-built sMDTchamber
- A simplified DAQ suitable for single-chamber data readout
- Expect to use this miniDAQ system for the sMDT/MDT chamber integration and commissioning on surface and inside the ATLAS cavern



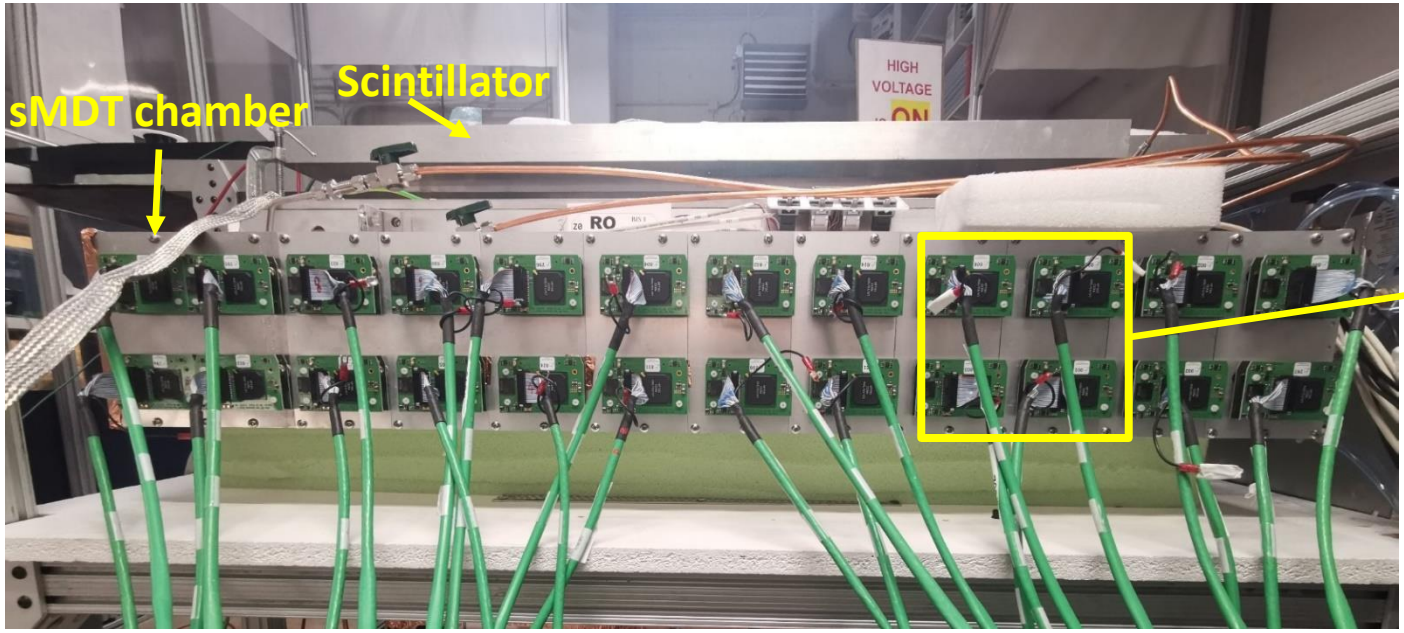
MiniDAQ board



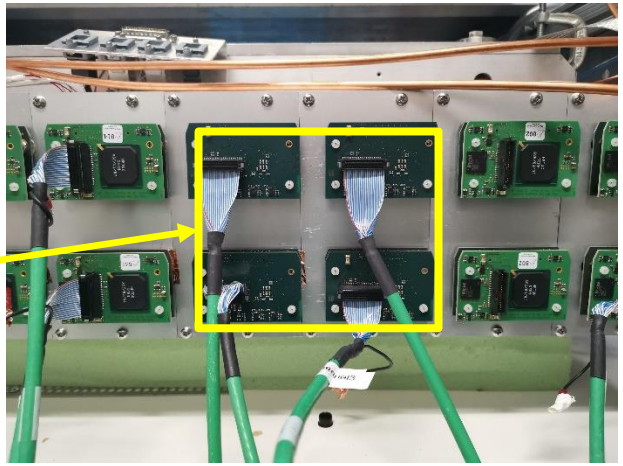


Architecture of the MiniDAQ board

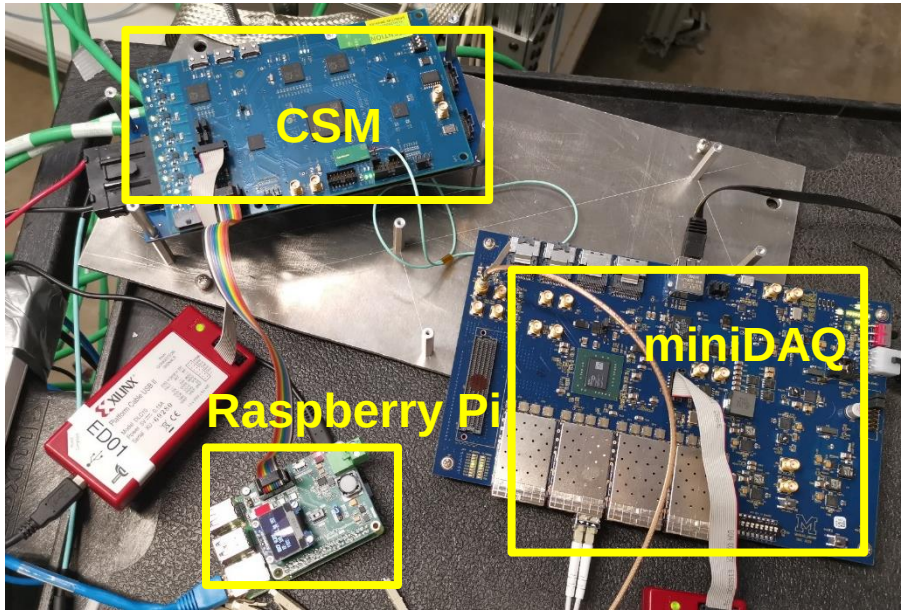
Joint tests of frontend electronics on an sMDT chamber



Newly built sMDT chamber (module0) at the University of Michigan equipped with legacy readout electronics



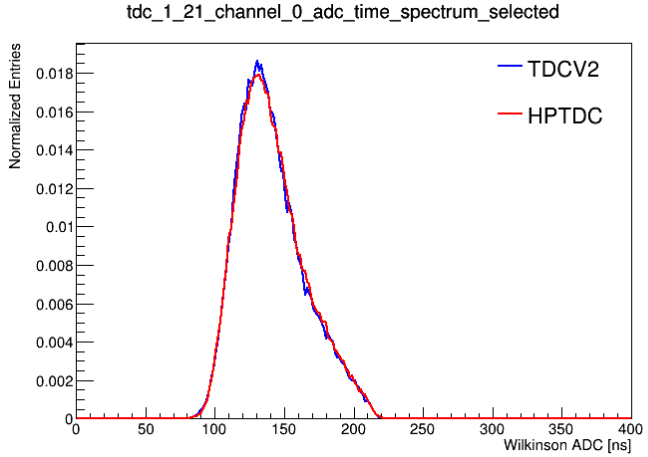
Replacing 4 legacy mezzanine cards with new TDC mezzanine cards



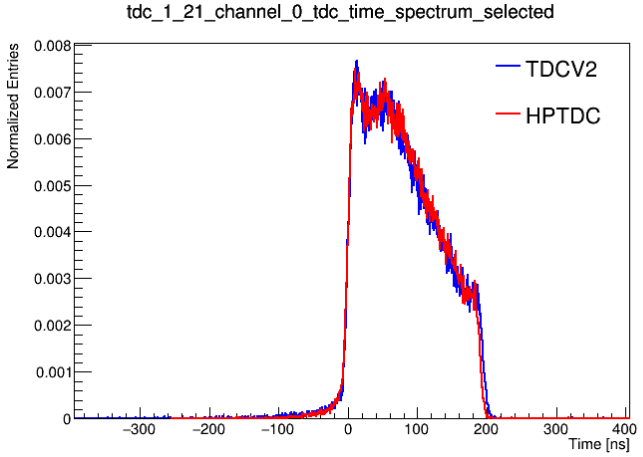
Off chamber connection

Joint tests of frontend electronics on an sMDT chamber

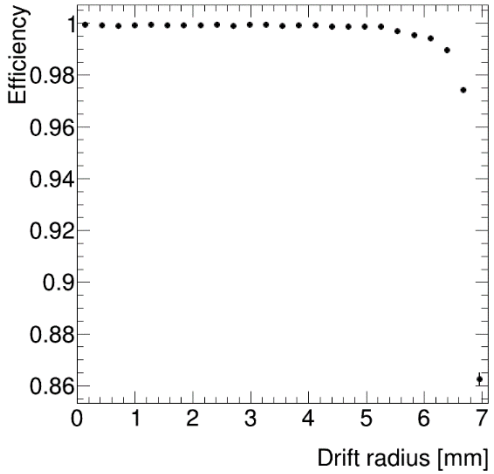
- First time to take cosmic ray data in the triggerless mode for a MDT detector
- Scintillator signals digitized by an FPGA TDC developed at Michigan
- Trigger matching performed inside the miniDAQ FPGA, and matched hits sent out to a PC
- TDC /ADC spectra and efficiency compared between the triggerlessmode and the triggered mode



Single tube ADC spectrum comparison



Single tube TDC spectrum comparison



Average tube efficiency

Summary

- ASD ASIC pre-production shows 92.4% yield rate, production finished and automatic test fixture to be finalized for QC tests of 80k ASICs
- A TDC ASIC with TMR protection is fabricated and tested. The design will be finalized after the planned irradiation test at Fermilab and the cosmic ray test at CERN GIF++
- All types of mezzanine card prototypes have been designed and tested. Design can be finalized after the LDO irradiation tests
- A CSM prototype with lpGBTs implemented has been designed and tested. Irradiation tests are planned for the onboard FPGA and LDOs
- A miniDAQ board has been designed to integrate all the available frontend electronics prototypes, which include the new ASD ASIC, new TDC ASIC, new mezzanine cards, new CSM board and new CSM motherboard