Development of Low Temperature Analog Readout for LAr-TPC

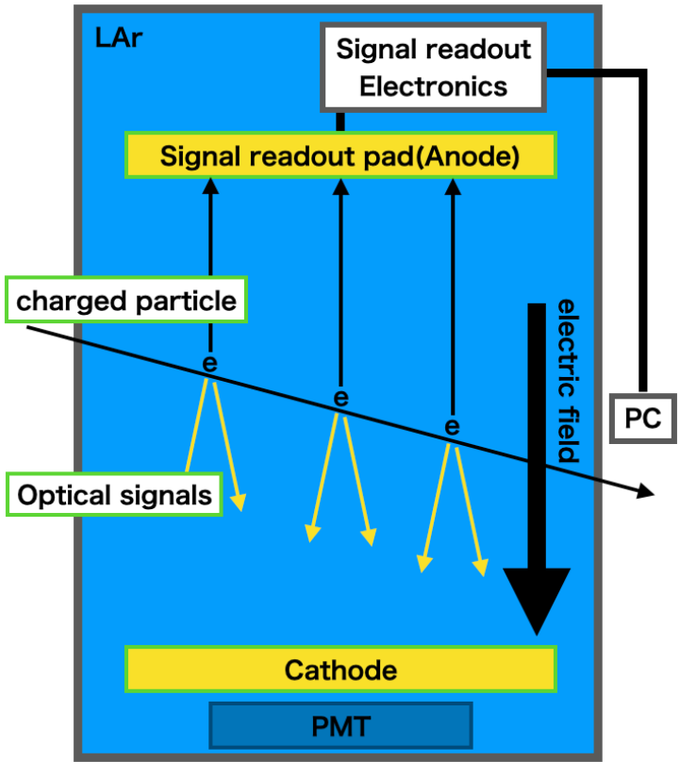
Takuto Kosaka, Shinya Narita, Kentaro Negishi, Shota Sumomozawa,
Iwate University

Ken Sakashita, Tetsuichi Kishishita, Manobu M Tanaka, Takuya Hasegawa, Masayoshi Shoji
High Energy Accelerator Organization(KEK)

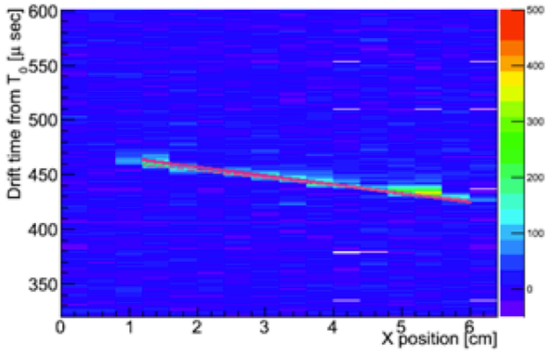
Kentaro Miuchi, Takuma Nakamura
Kobe University

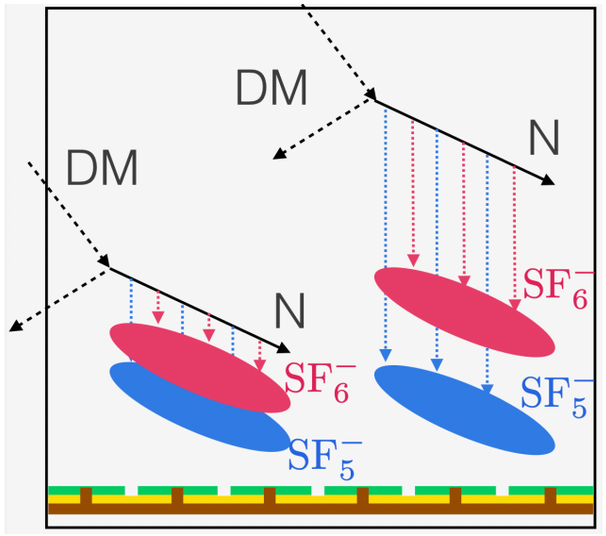
Introduction

Huge size TPC based 3D tacking detector is considered to be used for future neutrino experiment and directional dark matter search;

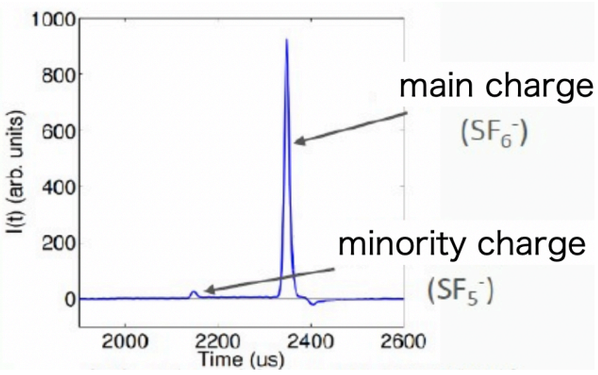


Liquid Ar TPC
(LAr-TPC)





Negative Ion Micro TPC
(NIμTPC)



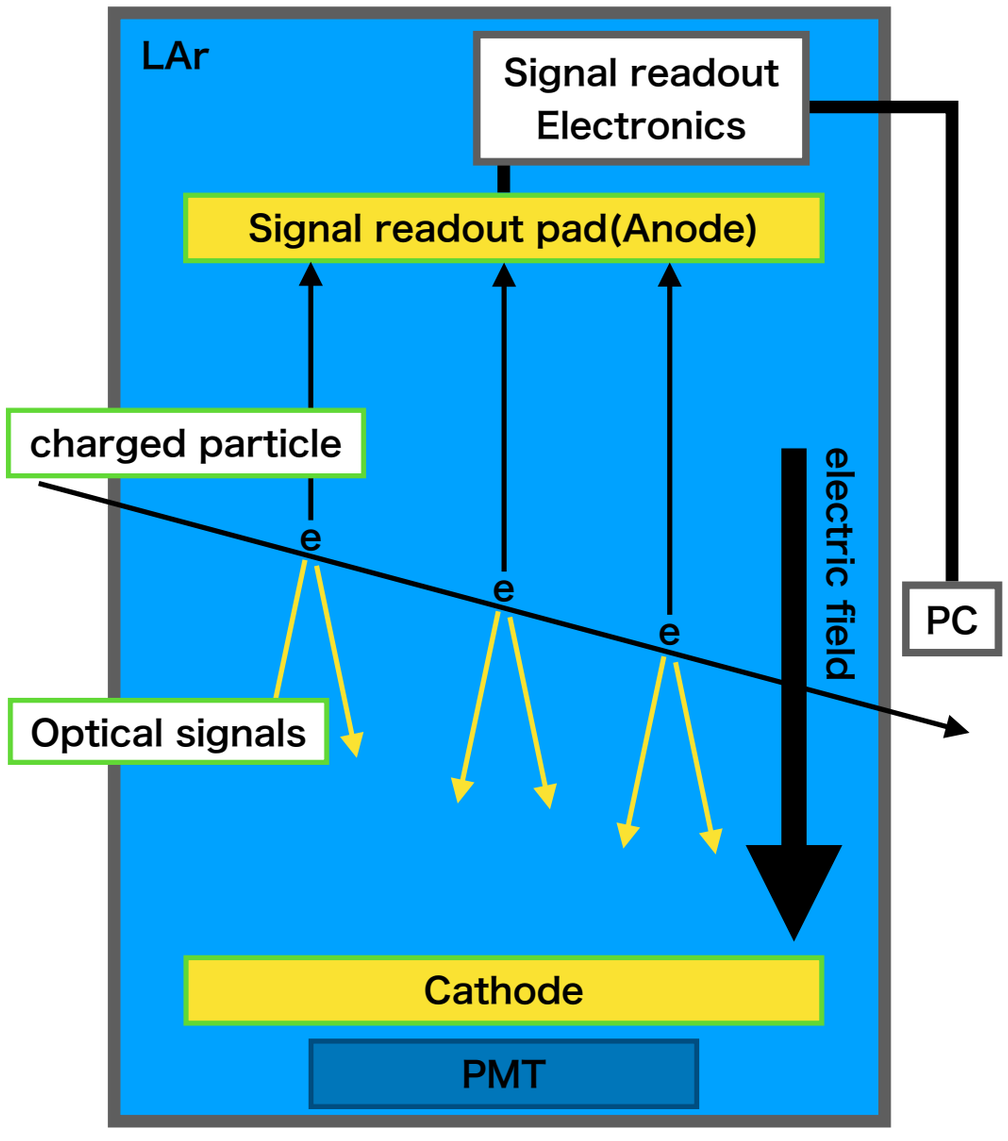
We have developed a signal readout electronics

LTARS (Low Temperature Analog Readout System)

based on ASIC technology for the detector

R&D goals of signal readout electronics

In this presentation, we mainly discuss the performance in terms of use for LAr-TPC.



LAr-TPC

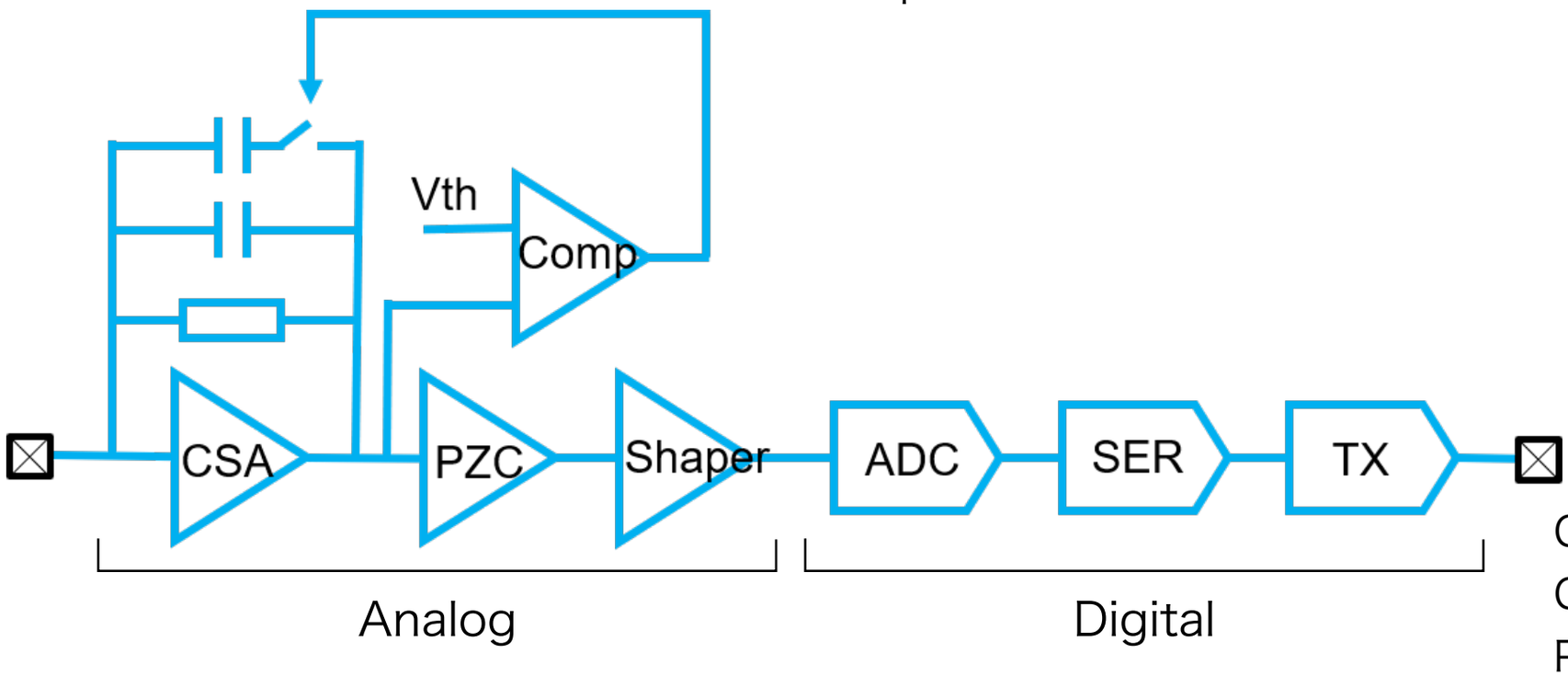
- High integration
- Low power consumption
- Stable operation in low temperature environment (LAr temperature: -185℃)
- **Low noise (ENC<3000e-)**
  - To read out the mip signal with the signal-to-noise ratio of higher than 10.
- **High gain (10mV/fC)**
- **Wide dynamic range (-1600 fC)**
  - To detect shower events with about 50 times larger than the mip signal

Circuit configuration of LTARS

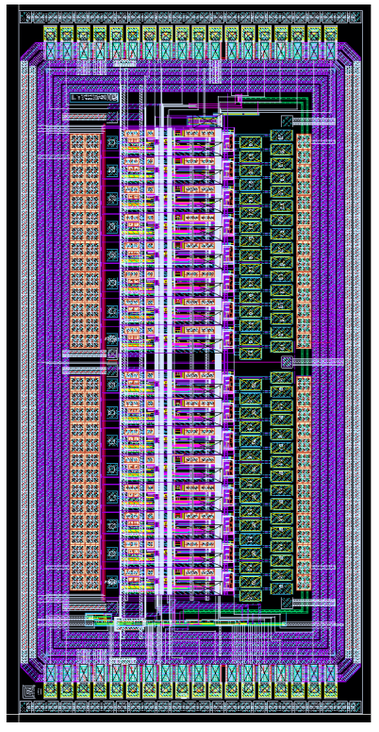
The unique points of LTARS are

- Automatic switch the gain mode, to keep proper dynamic range, using comparator,
- Two modes of peaking time,
- ADC function on the ASIC chip.

We named the ASIC we developed LTARS2018.



1ch of LTARS2018



LTARS2018

CSA…Charge Sensitive pre-Amplifier
Comp…Comparator
PZC…Pole Zero Cancellation circuit
Shaper…shaper amplifier
ADC…Analog to Digital Conversion
SER…Serialization
TX…Transmitter

Design specification

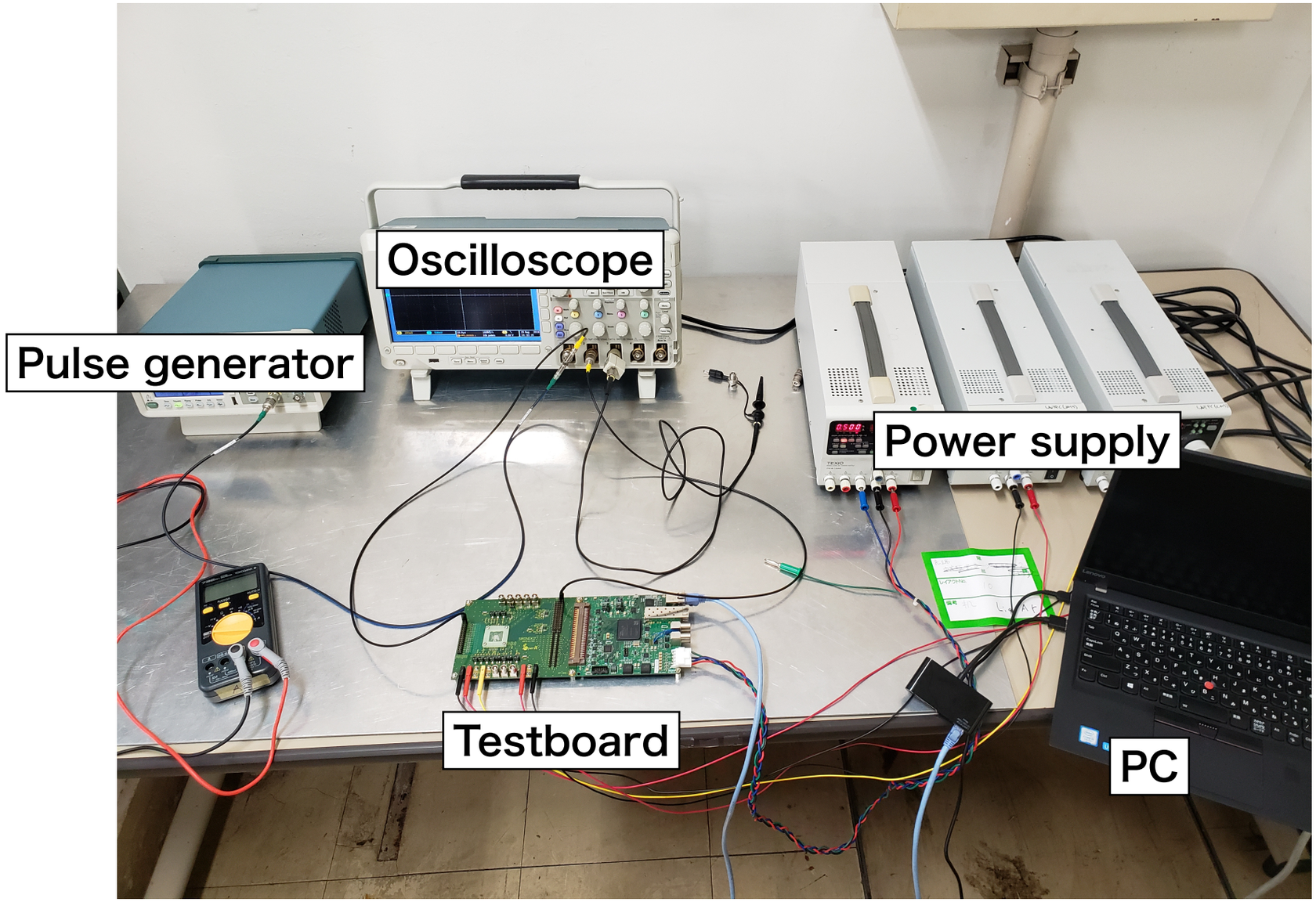
LTARS2018 performance targets

Parameter	High Gain mode(HG)	Low Gain mode(LG)
Peaking Time	1μs(Fast mode),4μs(Slow mode)	
Conversion Gain	10mV/fC	0.5mV/fC
Dynamic Range	±80fC	±1600fC
ENC	<3000e-	<62500e-

This ASIC also has a function to switch
the peaking time (Fast/Slow) to be versatile.

We investigated the LTARS2018 performance at room temperature and LAr temperature.

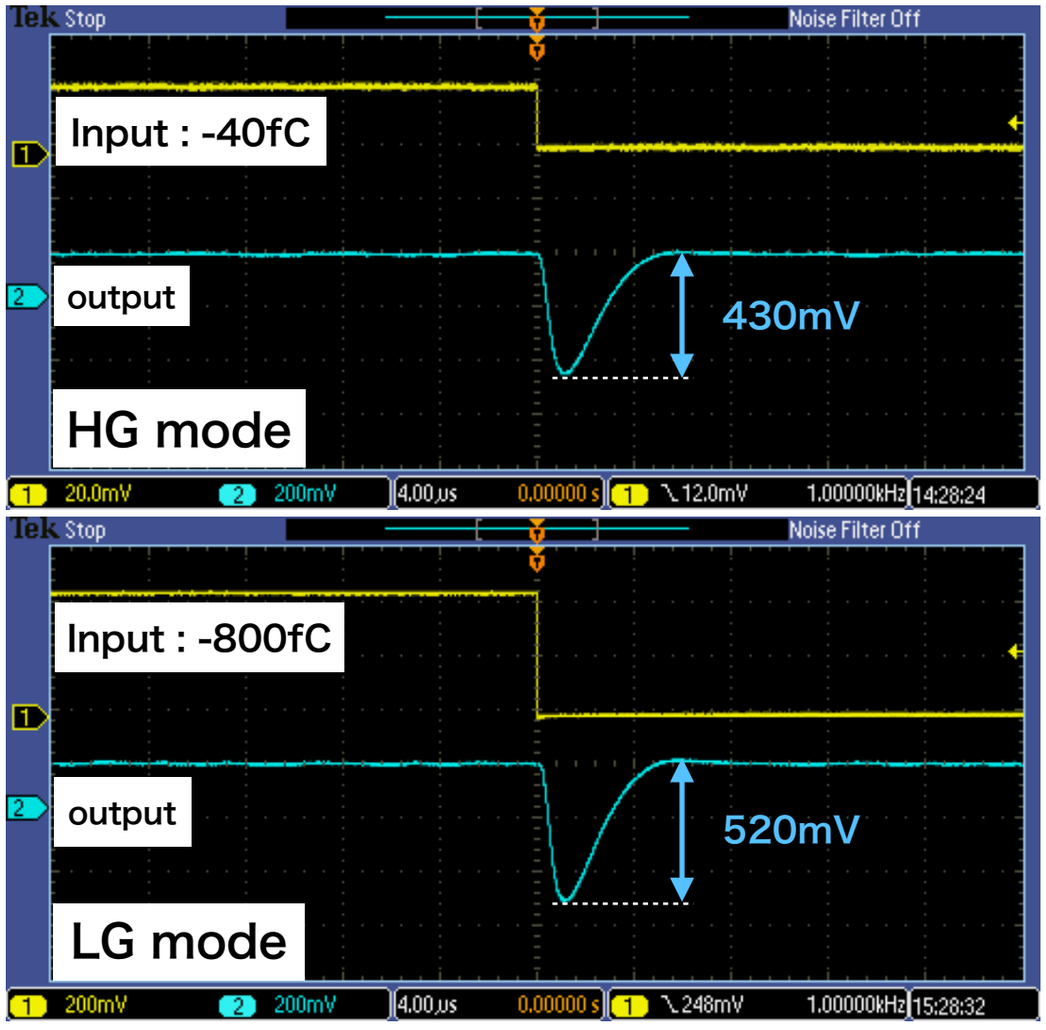
Experimental setup at room temperature



<Experimental method>

- Input signal from the pulse generator to the testboard.
  (The charge signal is input through voltage-charge conversion)
- Monitor the analog output and acquired the waveform with the oscilloscope.
- Acquire digital signals and display with the PC.

Results of analog signal processing @RT



Analog output (switch the gain)

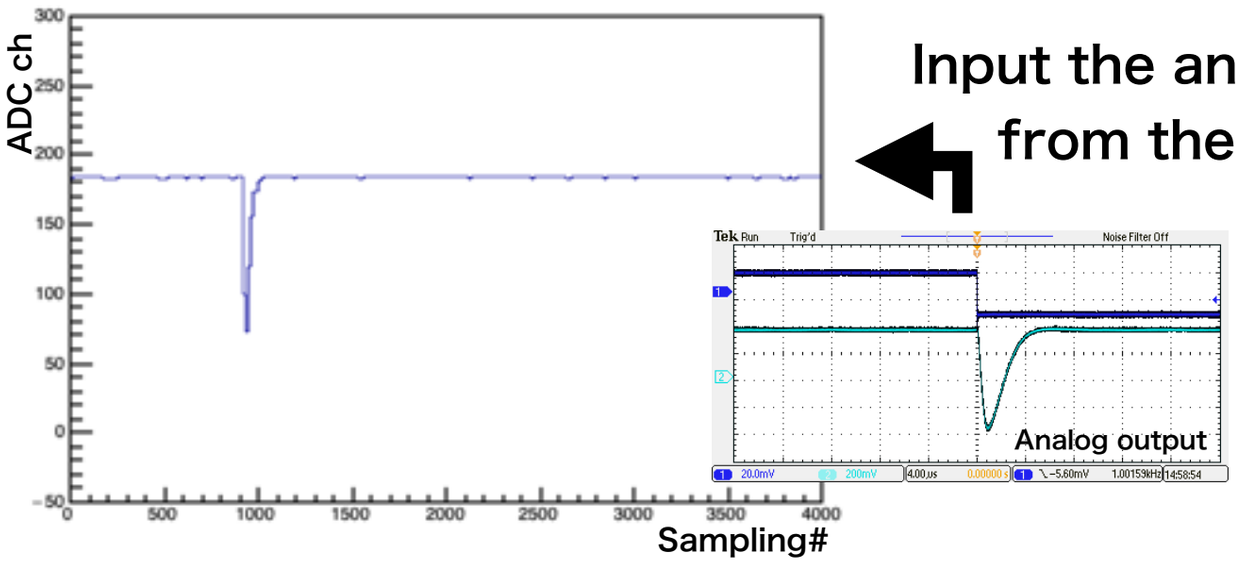
Parameter		High Gain(HG)	Low Gain(LG)
Peaking Time		1.2µs	1.0µs
Conversion Gain	Positive	10.0mV/fC	0.6mV/fC
	Negative	10.7mV/fC	0.65mV/fC
Dynamic Range		±100fC	±1600fC
ENC		2700e^-	37000e^-

Requirements

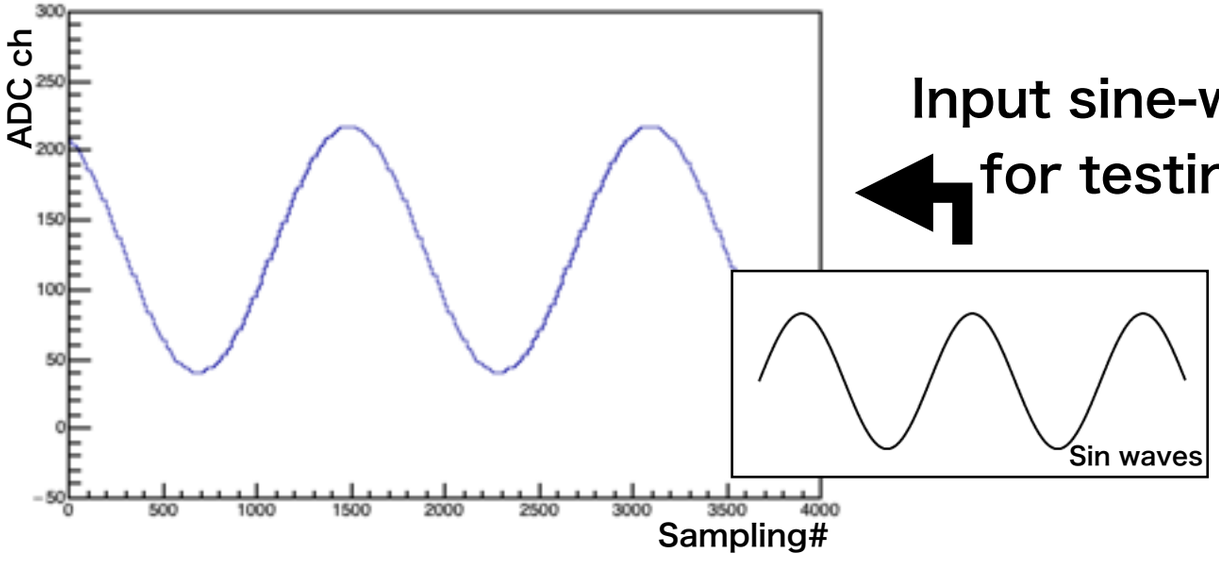
- Peaking Time：1µs,
- Conversion Gain：10mV/fC(HG), 0.5mV/fC(LG)
- Dynamic Range：±80fC(HG), ±1600fC(LG)
- ENC：<3000e^-(HG), <62500e^-(LG)

Each parameter satisfies the requirements.
Performance of analog signal processing part is an operational level.

Results of A/D conversion @RT



Input the analog signal from the shaper



Input sine-wave for testing

Digital output

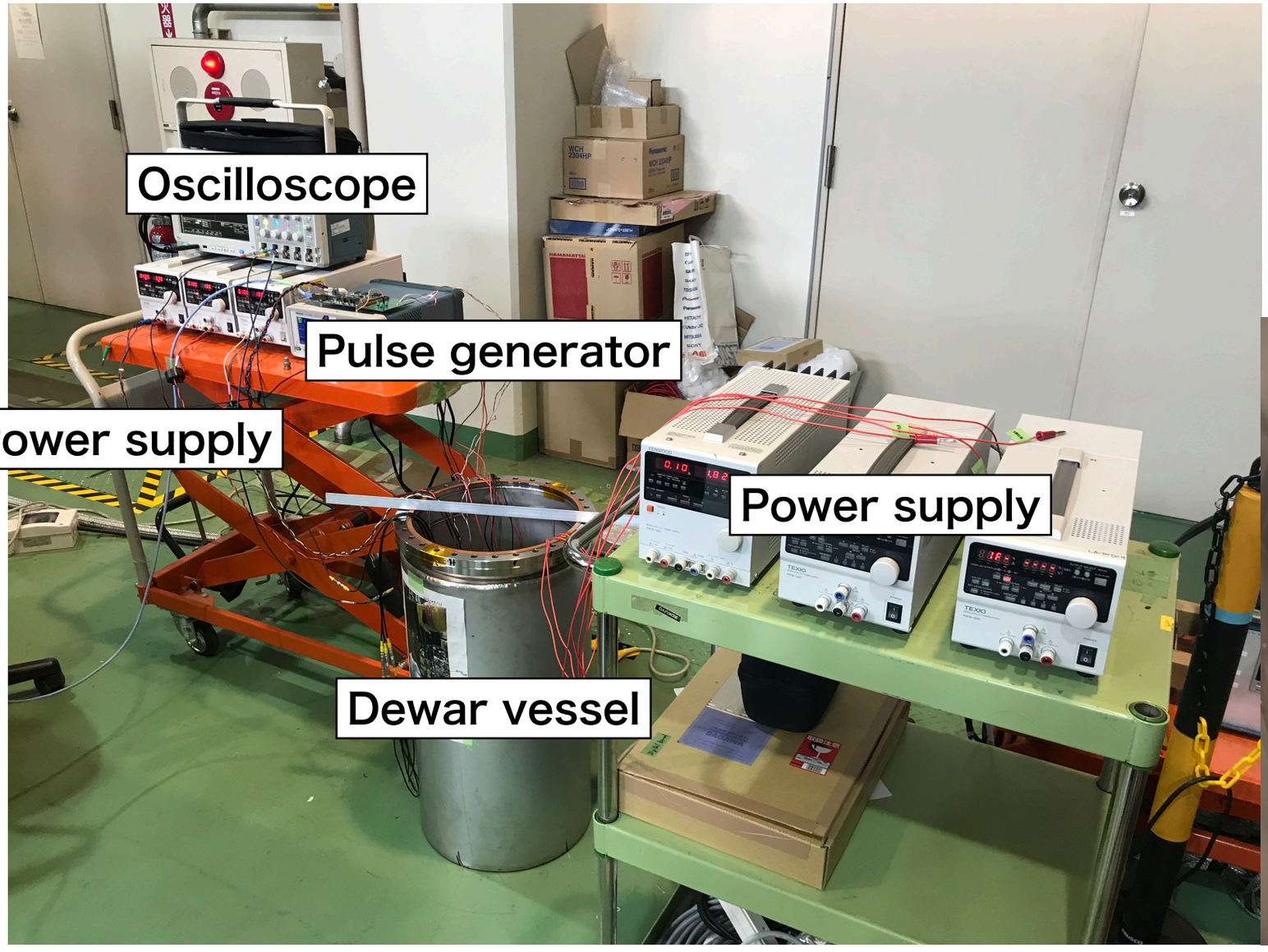
ADC spec.

- SAR ADC
- 8bit
- 10MHz sampling

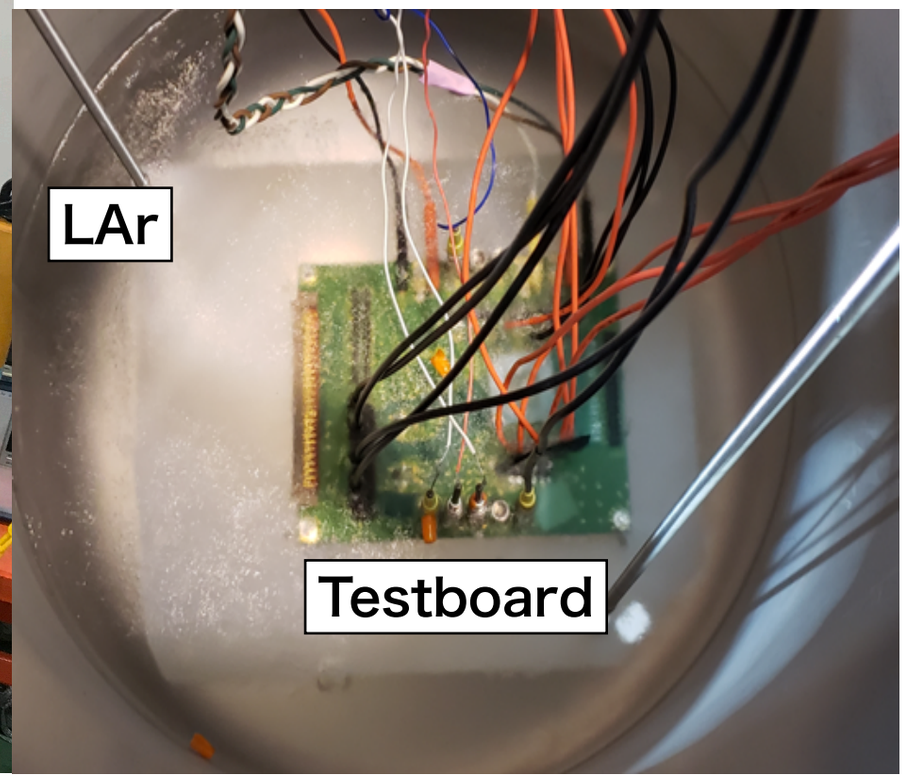
We acquired a digitized analog output and digitized sine-wave as expected.

A/D conversion is working properly

Experimental setup at LAr temperature



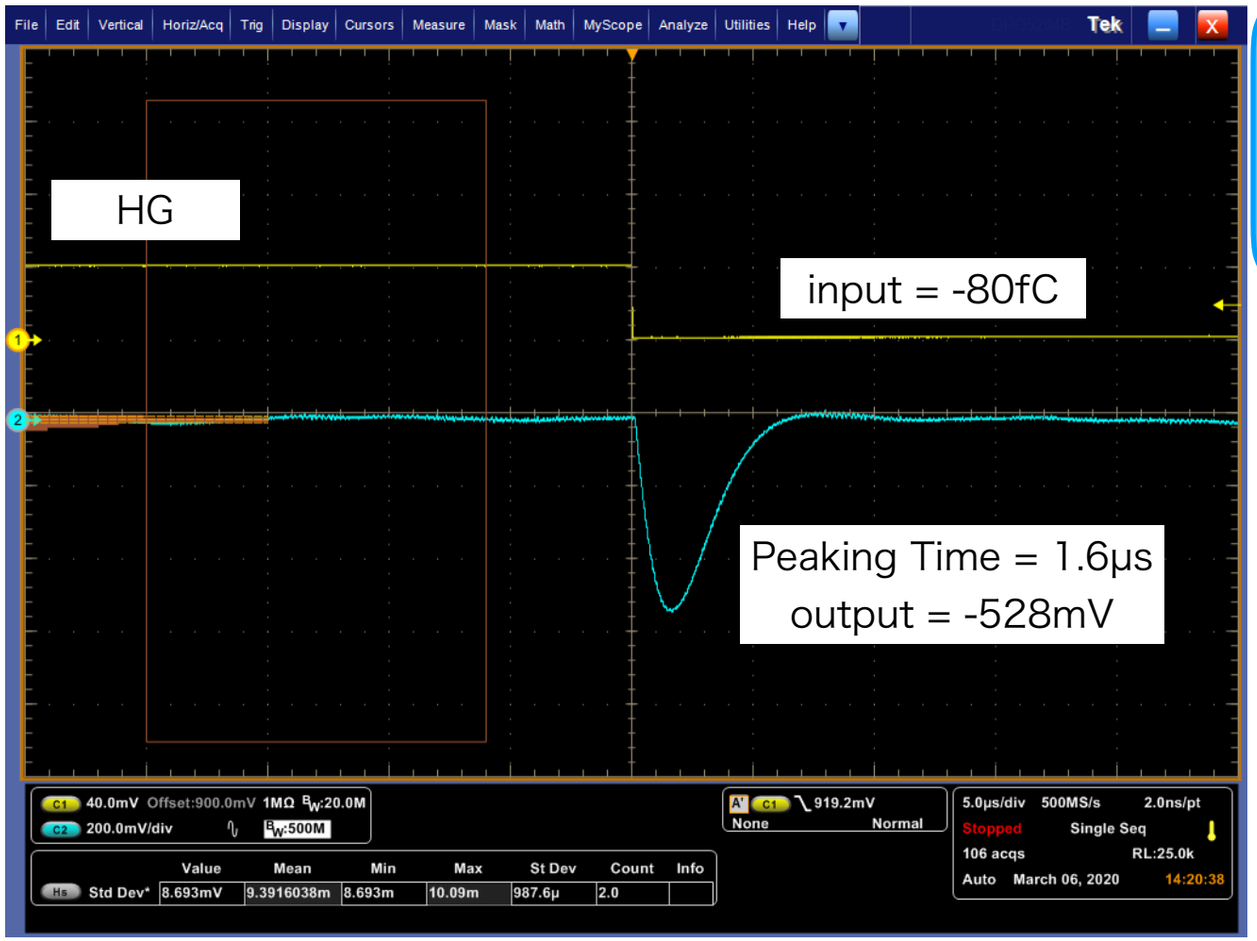
Inside the dewar vessel



<Experimental method>

- Direct immersion of the LTARS in a dewar vessel filled with LAr.
- Monitor analog output and acquired waveform with the oscilloscope connected outside the dewar vessel.

Results at LAr temperature



Averaged waveform at LAr temperature

- **Peaking Time : 1.6μs**
- **Gain : 6.6mV/fC**

Compared with the results at room temperature,
the peaking time increased by about 60% and
the gain decreased by about 40%.

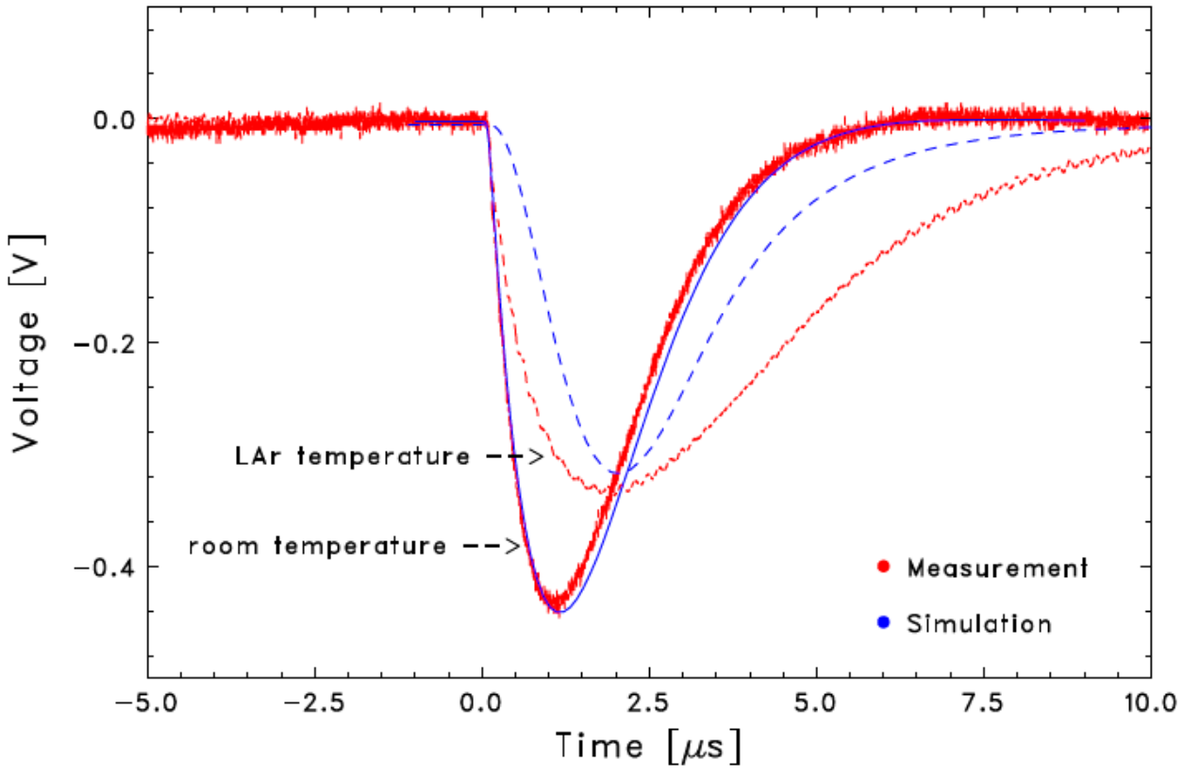
The performance was degraded at LAr temperature.

We think this cause is the threshold voltage of the transistor increases as temperature decreases, thereby changing the operating point of the device and not supplying the proper bias current.

Low temperature simulation

We describes a unique simulation method for reliable electronics at low temperature, which utilizes the body effect to mimic the threshold shifts.

- Instead of modifying the individual transistor parameters, we attempt to utilize the body effect by changing the substrate voltage.
- We could reproduce the same performance degradation as the measurement.



Waveform at room temperature and LAr temperature

Body effect

The change in the threshold voltage by an amount approximately equal to the change in the source-bulk voltage.

$$V_{th} = V_{th0} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|})$$

V_{th} : Threshold voltage of Tr,

V_{th0} : Threshold voltage of Tr at room temperature,

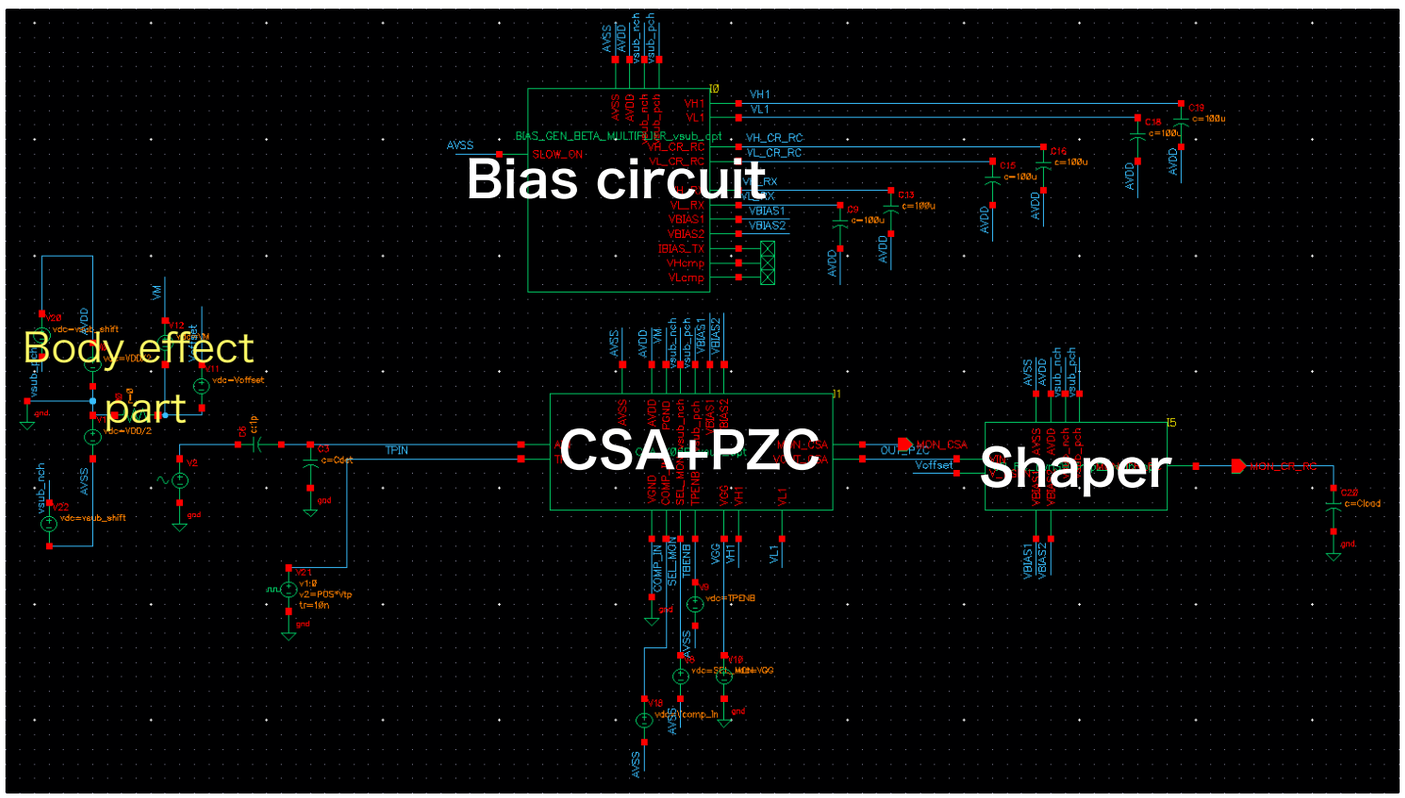
γ : Body effect coefficient,

Φ_F : Fermi potential of bulk silicon,

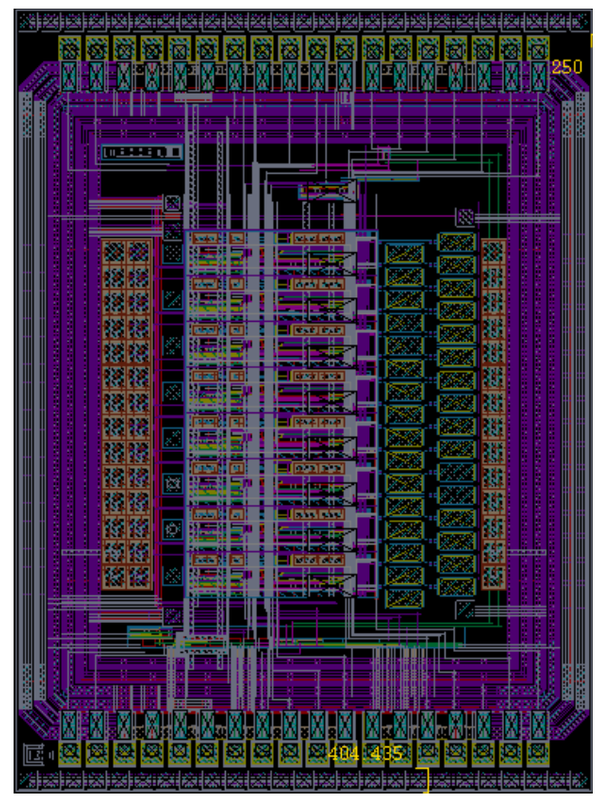
V_{SB} : source-bulk potential difference

- The width of the pulse measured at LAr temperature is wider than that of the simulation since it is mounted on the testboard in the measurement.

Design of modified ASIC (LTRAS2020)



1ch of LTARS2020



chip layout

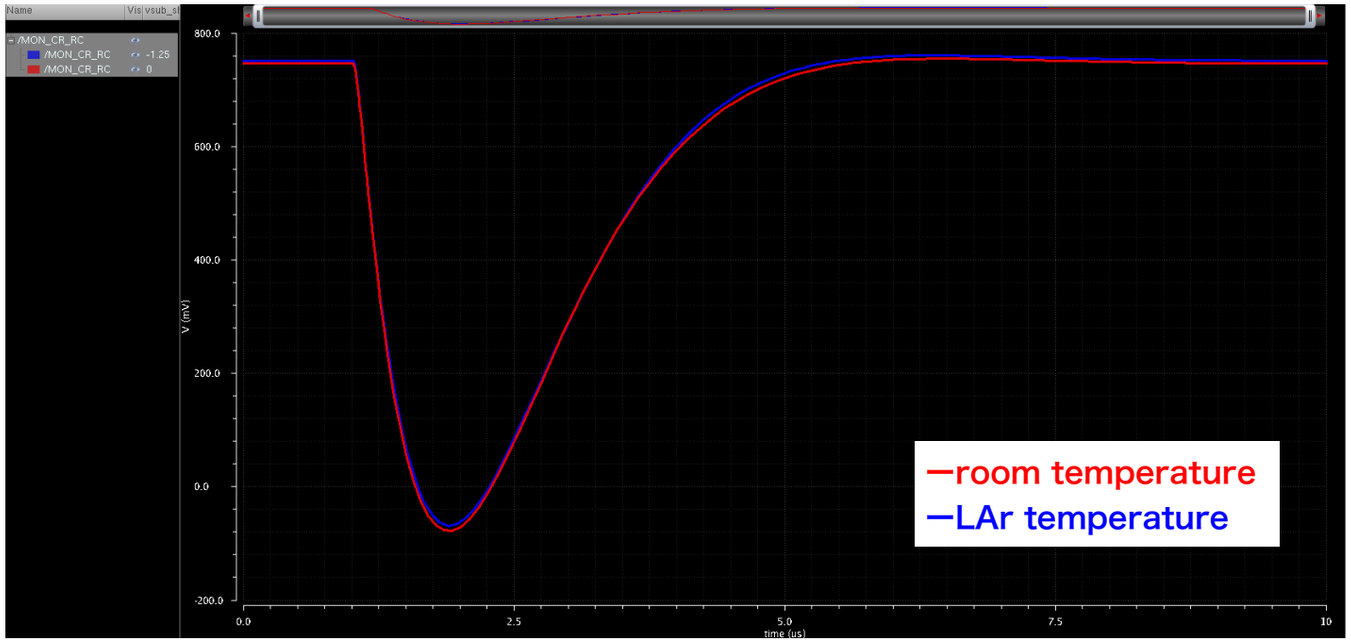
LTARS2020

Modified version of LTARS2018 with better low temperature performance.

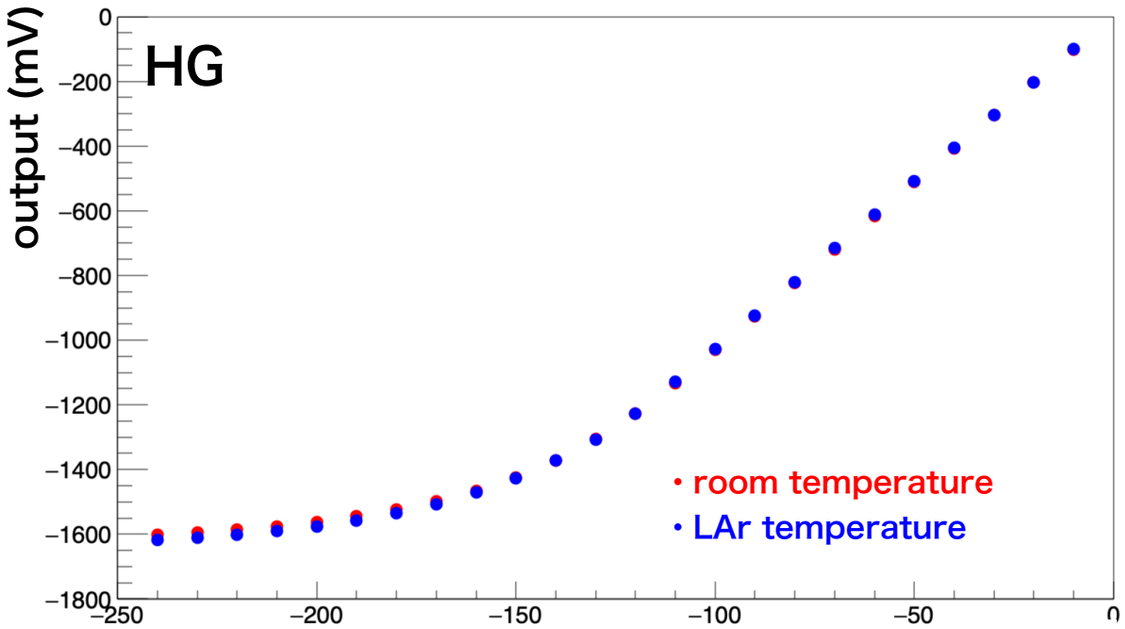
- **A feedback-based bias circuit generates and supplies the bias current internally in the ASIC.**
  - Even if the threshold voltage of the transistor changes at LAr temperature, a constant bias current is supplied to the ASIC.

The LTARS2020 performance at LAr temperature was evaluated using low temperature simulation.

Results of simulation



Analog output



Conversion gain

LTARS2020's performance at LAr temperature was evaluated with low temperature simulation considering the body effect.

- No clear difference was found between room temperature and LAr temperature. **-> There is no degradation.**
- Each parameter satisfies the requirements.

Summary

We have developed signal readout electronics (LTARS2018).
In this presentation, we mainly discuss the performance in terms of use for LAr-TPC

We have tested the LTARS2018 of room temperature and LAr temperature

- Working properly at room temperature.
- The performance was degraded at LAr temperature.
  - We think this cause is the threshold voltage of the transistor increases as temperature decreases.

LTARS2020 (modified version of LTARS2018)

- A feedback-based bias circuit generates and supplies the bias current internally in the ASIC.
- No clear difference was found between room temperature and LAr temperature, there is no degradation in the simulation.

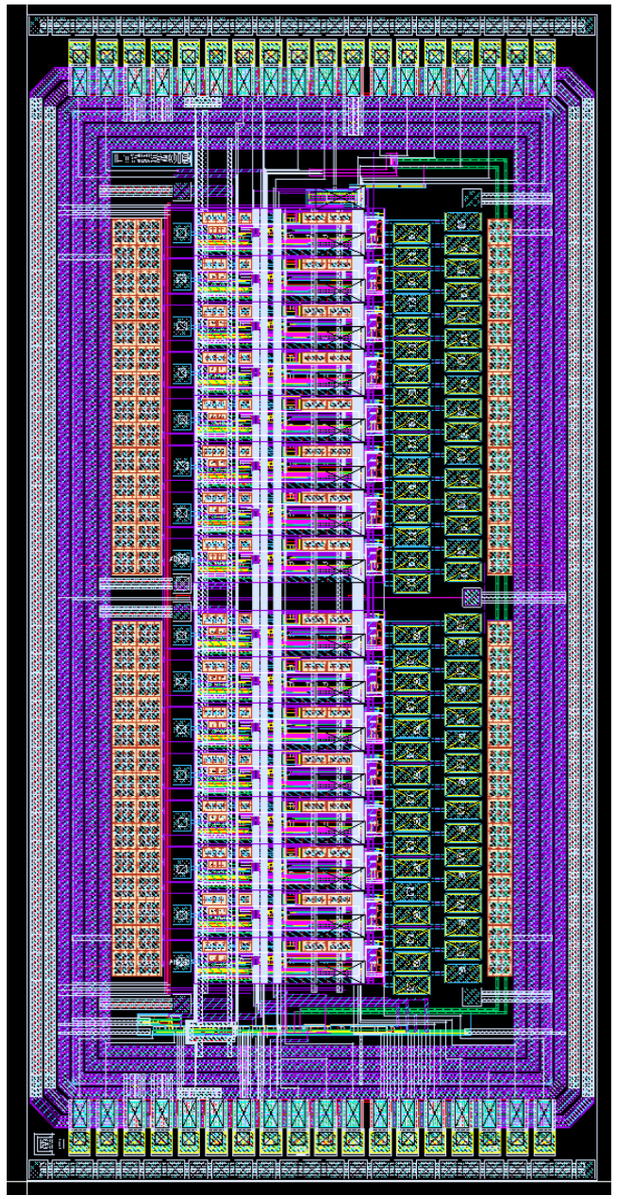
T.Kishishita et al. : JINST 15 T09009 , 2020.

Next plans

- LTARS2020's performance tests at room temperature and LAr temperature.
- Cosmic ray test implemented to LAr-TPC.

Backup

- The physical layout of the readout ASIC implemented in the Silterra 180 nm CMOS technology is shown in figure.
- The chip includes 16 identical signal processing channels.
- Chip size is 5mm×2.5mm.

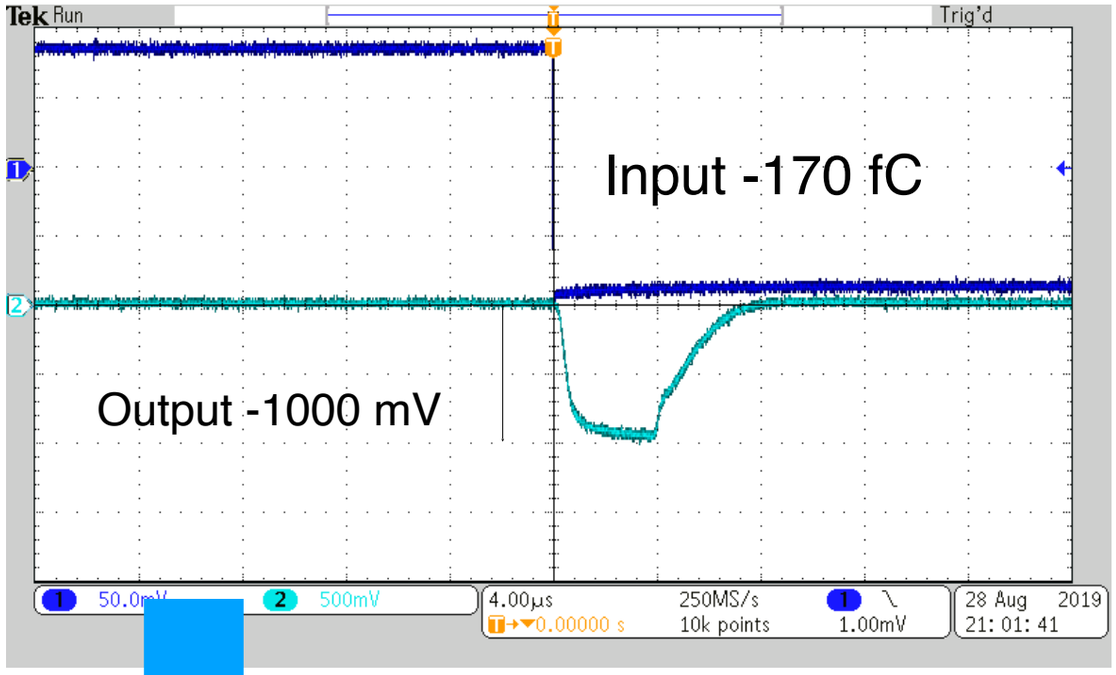


LTARS2018

Automatic gain mode switching

- CSA output < Vth
  → High gain mode
- CSA output > Vth
  → Low gain mode

Vth : comparator threshold voltage (variable)



Switched to low gain mode