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Development of a timing chip prototype in 110 nm CMOS technology

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We present a readout chip prototype for future pixel detectors with timing capabilities. The prototype is intended for characterizing 4D pixel arrays with a pixel size of 100x100 μm², where the sensors are LGADs. The long term focus is towards a possible replacement of disks in the extended forward pixel system (TEPX) of the CMS experiment during the HL-LHC. The requirements for this ASIC are the incorporation of a TDC (Time to Digital Converter) in the small pixel area, low power consumption and radiation tolerance up to 5E15 neq/cm² to withstand the radiation levels in the innermost detector modules during HL-LHC. A prototype has been designed and produced in 110 nm CMOS technology at LFoundry and UMC with different versions of TDC structures, together with a front end circuitry to interface with the sensors. The design of the TDC will be discussed, with the test set-up for the measurements, and the first results comparing the performance of the different structures.

TIPP2020 abstract resubmission?

No, this is an entirely new submission.

Funding information

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