Electronics and Triggering Challenges for the CMS High-Granularity Calorimeter

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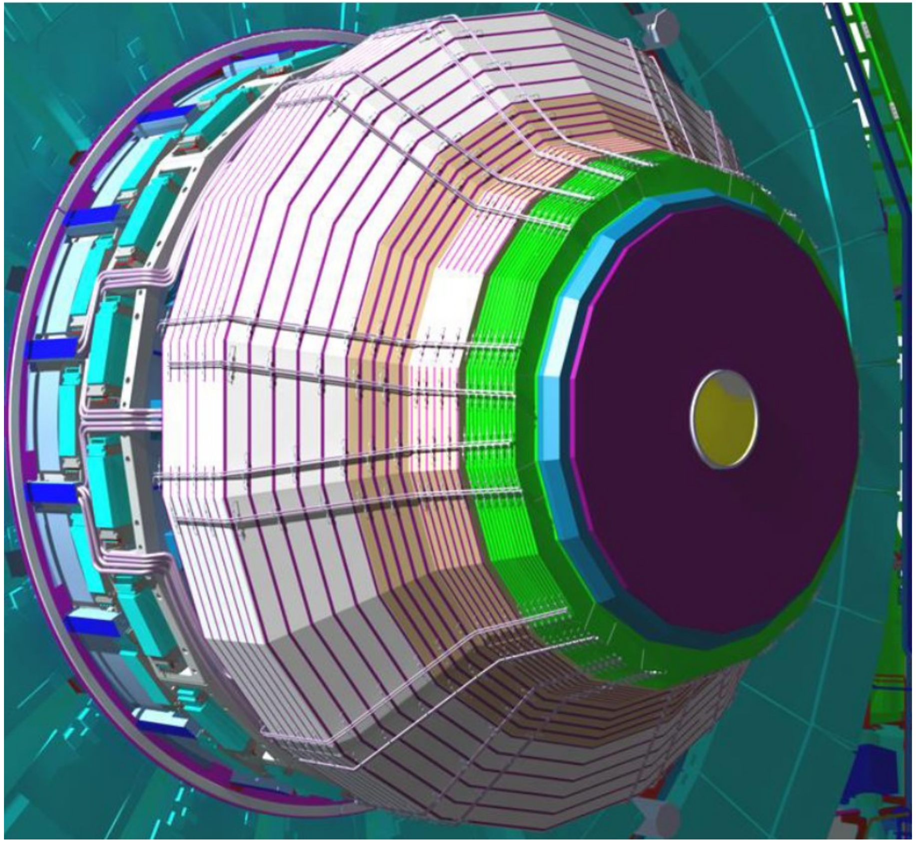
On behalf of the CMS Collaboration

Outline

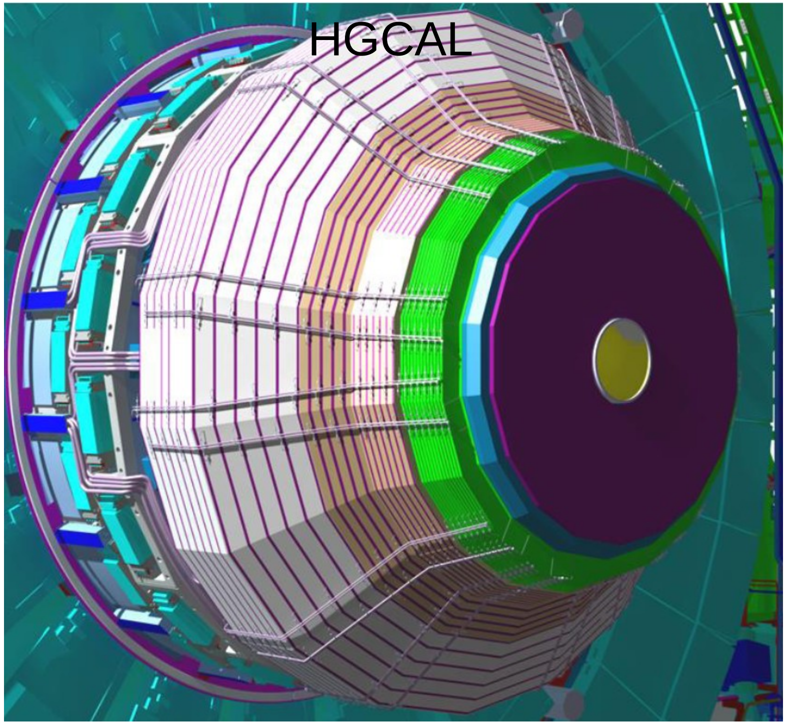
- Brief Overview
  - Structure
  - Requirements
  - Constraints
- Tiling and Variants
- Readout Architecture
  - Data & Trigger Paths
- LD-HexBoard Design
- Power Tree
  - Power Modelling
- Mechanical Mockup
  - Phenomenology & design feasibility studies



Out with the old, in with the new...

Present CMS EndCap Calorimeters

HGCAL



- Calorimeter Endcap
  - Weight ~ 250 tonnes
  - Sampling calorimeter
  - CE-E(lectromagnetic) and CE-H(adronic)

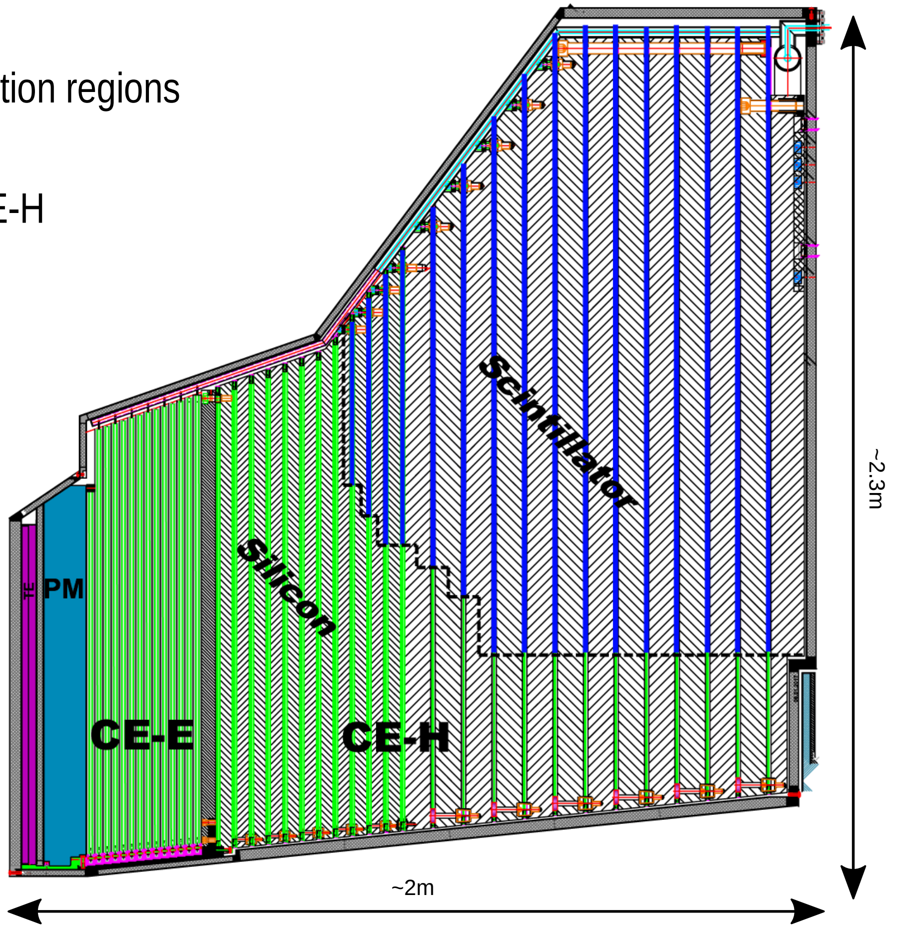
Detector Structure and Key Parameters

Active Elements:

- Hexagonal modules based on Si sensors in CE-E and high-radiation regions of CE-H
- Scintillating tiles with SiPM readout in low-radiation regions of CE-H

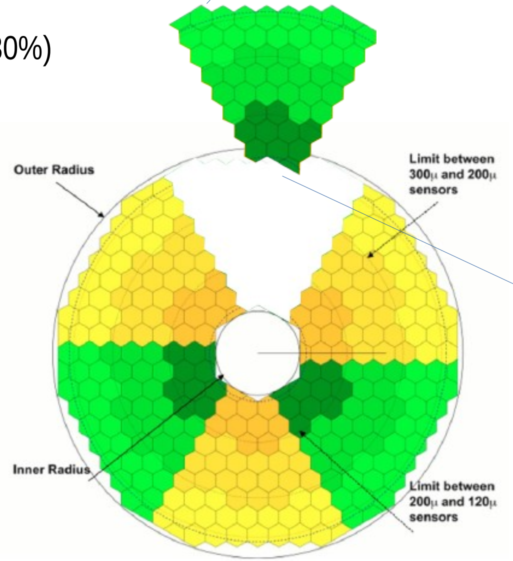
Key Parameters:

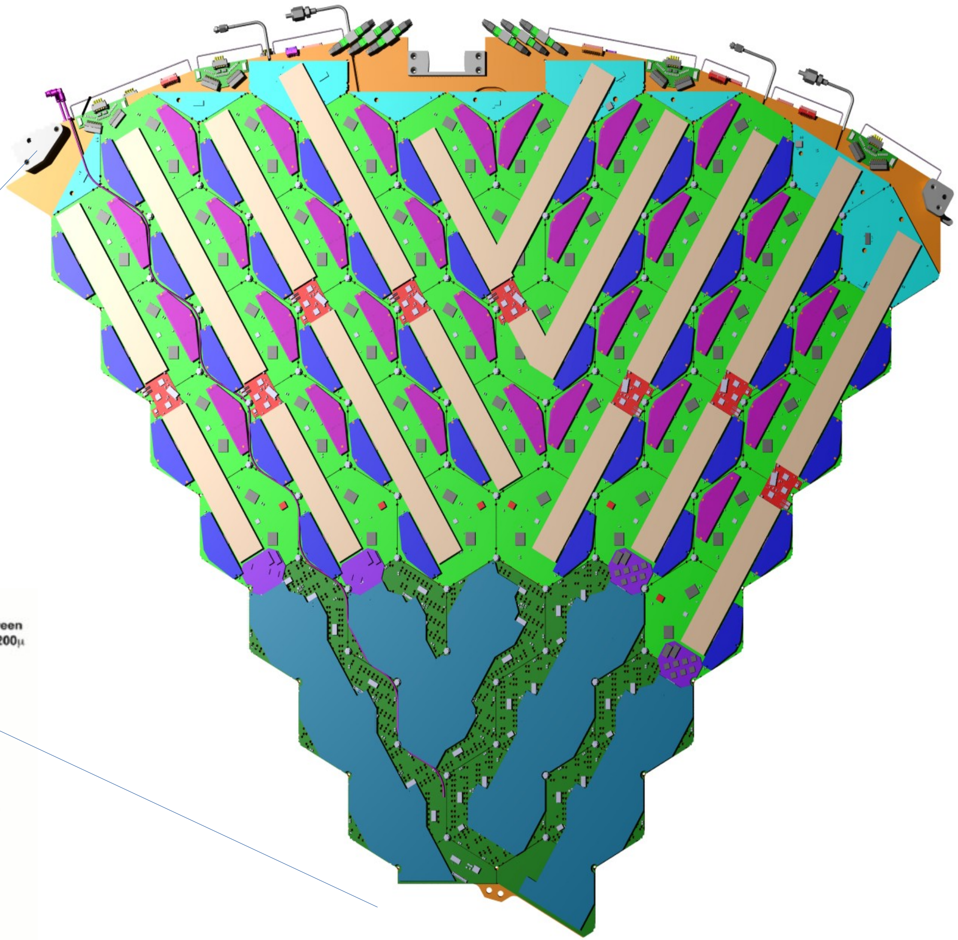
- HGCAL covers 1.5 < η < 3.0
- Up to 200 Mrads ; $8x10^{15}$ n/cm^2
- Full system maintained at -30 ^{o}C
- ~400 m^2 of scintillators
- ~620 m^2 of silicon sensors
- ~28000 Si modules
- **6M Si channels**, 0.5 cm^2 or 1.1 cm^2 cell size
- Data readout from all layers
- Trigger readout from alternate layers in CE-E and all layers in CE-H
- **~280 kW**



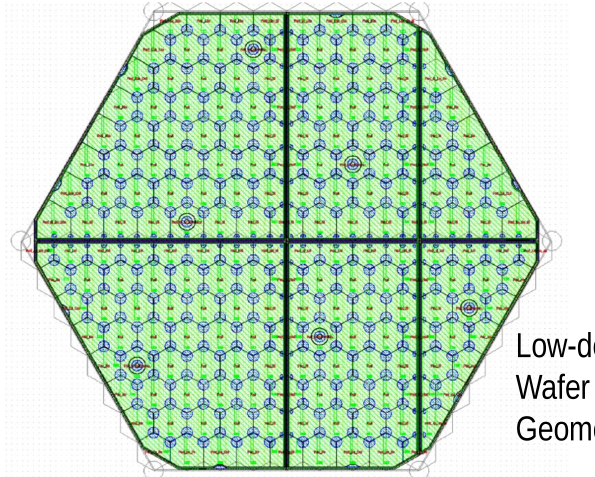
Cassettes: CE-E (Double Sided)

- Layers 1-28
- Silicon-only design
- 6-fold rotational symmetry
- High Density (HD) in inner regions
  - 0.5cm^2 diode pad
- Low Density (LD) in outer regions
  - 1.1cm^2 diode pad
  - Occupancy (=rate) and radiation field determined
- Hexagons optimise silicon wafer usage
  - Significant cost reduction cf rectangular (30%)
  - 200 mm wafers used
- Partials at inner/outer perimeters
  - Increases coverage
  - Increases # variants
  - Novel “multi-geometry” wafer

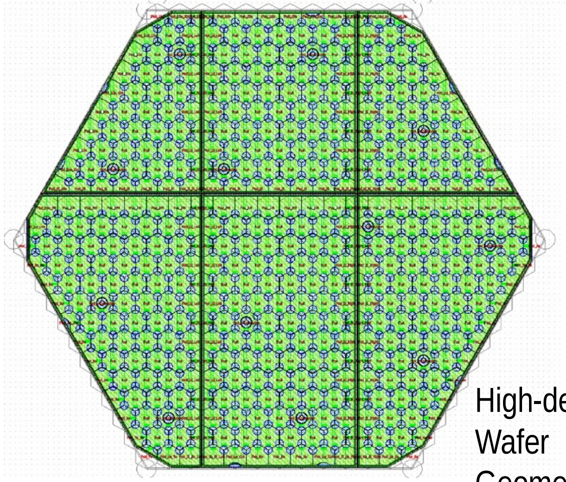




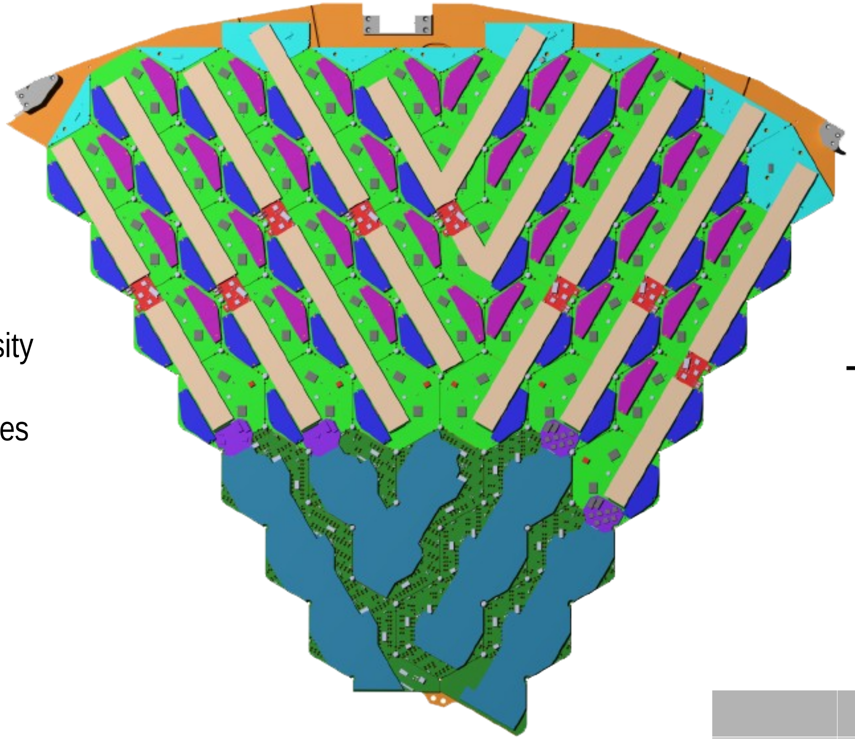
Coverage, Tiling and Partial Types



Low-density Wafer Geometries

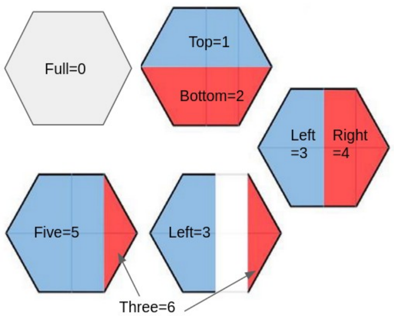


High-density Wafer Geometries

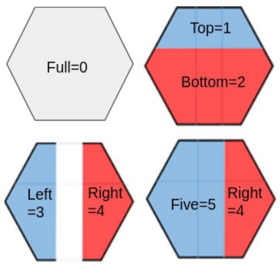


Large number of variants required →
Significant design task

LD partial sensor layouts



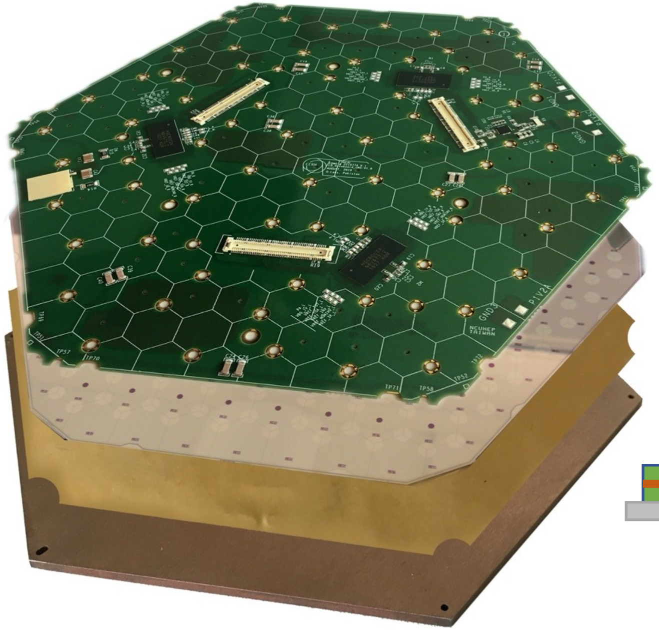
HD partial sensor layouts

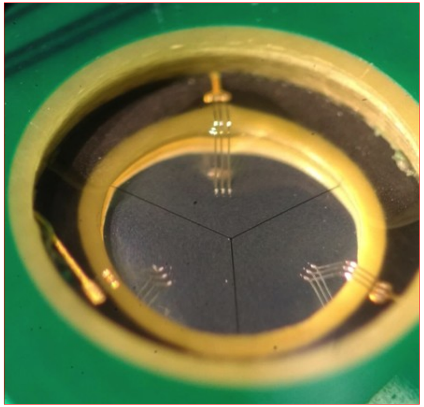


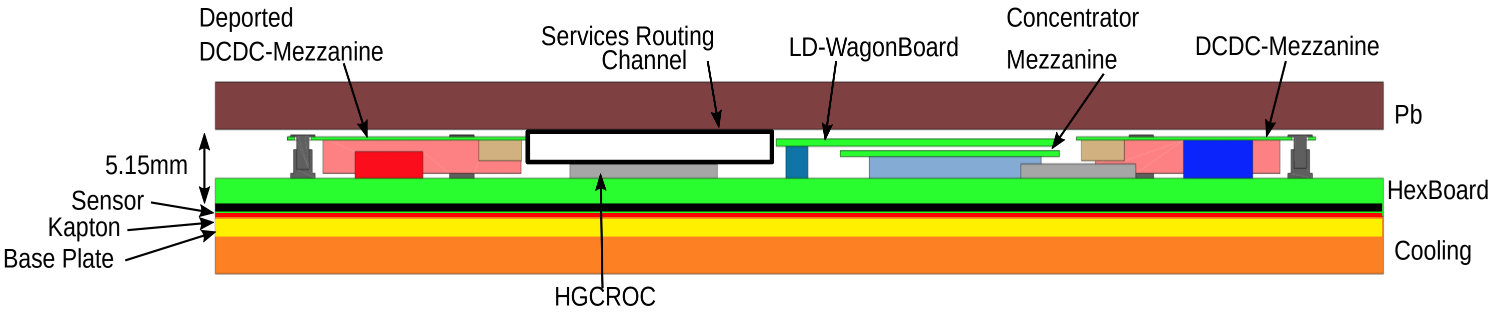
	HD		LD		Total
	Full	Partial	Full	Partial	
CE-E	3576	672	10056	2520	16824
CE-H	900	156	8046	2130	11232
Total	4476	828	18102	4650	28056
Fraction	16%	3%	64%	17%	100%

Vertical Stackup and Space Constraints

- 5.15mm between Cu & Pb
- Stepped holes
  - Connection through the PCB to sensor
  - Wire bonds used for CTE
  - Swiss cheese
  - Component placement and signal routing is difficult
- Cassette access is radial
  - Power,
  - Triggering, Timing, & Control,
  - Data (DAQ + Trigger)
  - Bias voltage
  - All must pass through outer periphery
- -30°C operation
  - Requires dry environment → pipe

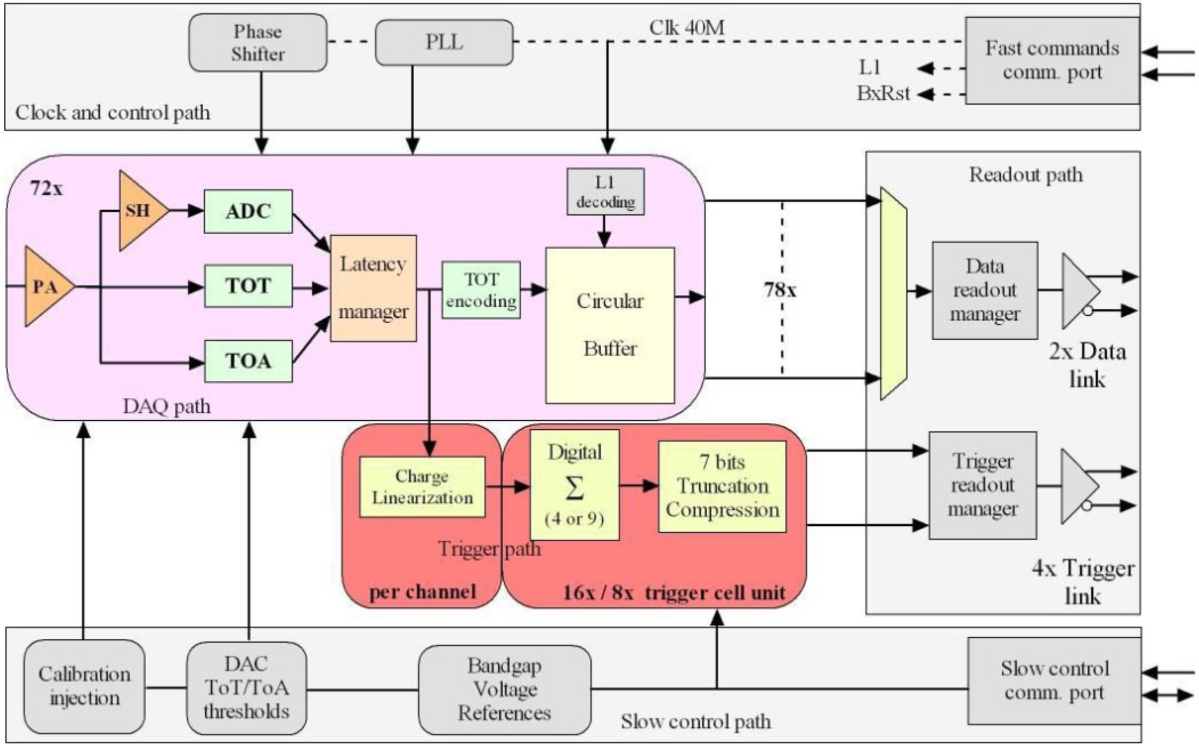




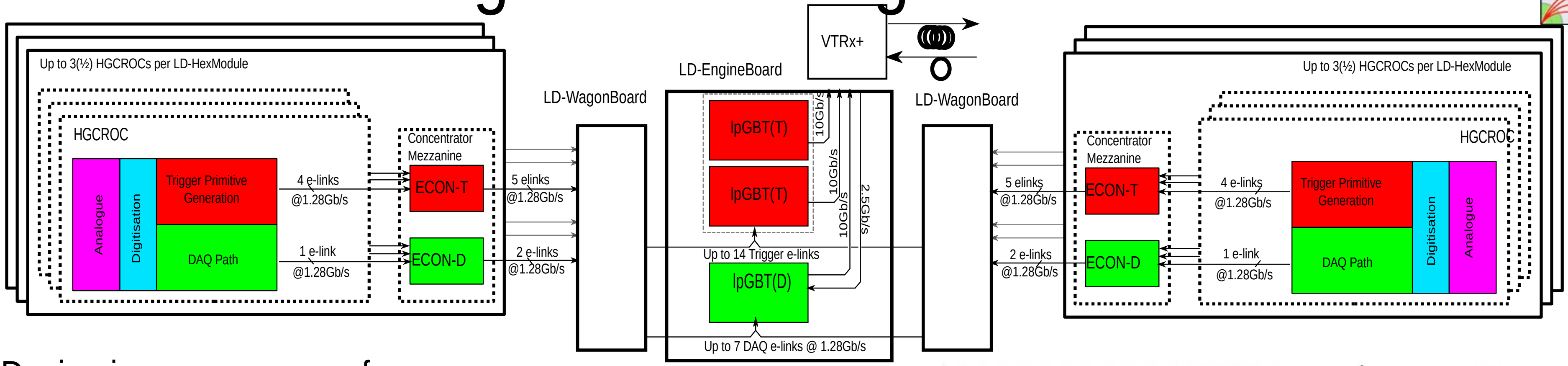


Main Si Front End Requirements

- Dynamic range:
  - 0.2fC → 10pC
- T_{res} ~20ps → 30ps rms (shower)
- HGCROC deals with these points
  - High Granularity Calorimeter Read-Out Chip
  - See Damien's talk tomorrow
- ~20 mW/channel
  - Analog + digital
- L1 Trigger Sums (fixed latency)
  - Alternate layers in CE-E
  - All layers in CE-H
- DAQ data zero suppression
  - 750 kHz trigger rate
  - Latency up to 12.5 μs

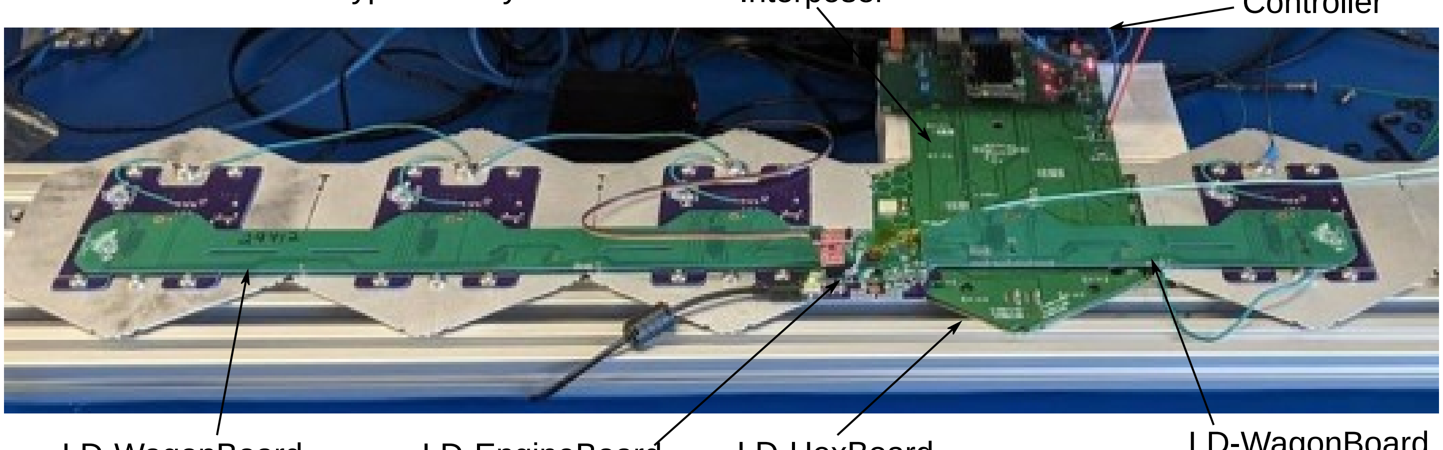


ReadoutTrain: Engines and Wagons

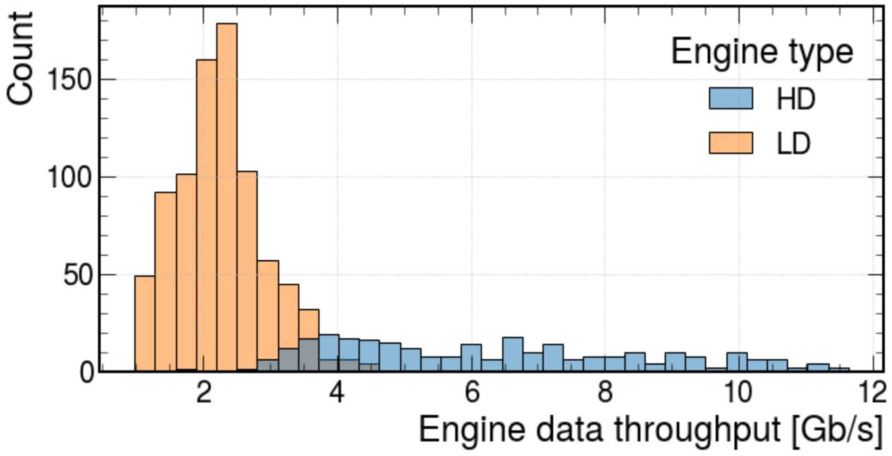


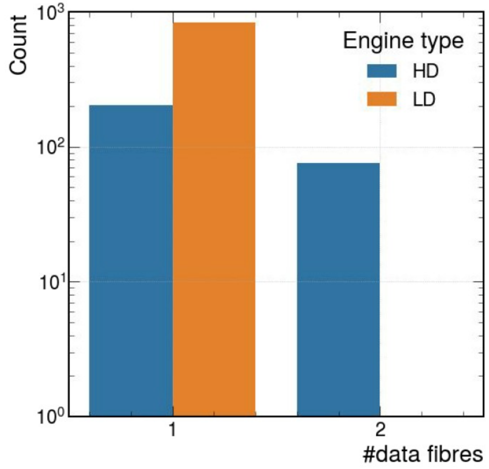
- Design is consequence of
  - Large and irregular area
  - Inaccessibility
  - Fine pitch of components
  - Wide range of data rates
  - Space constraints
  - Cost
  - + others

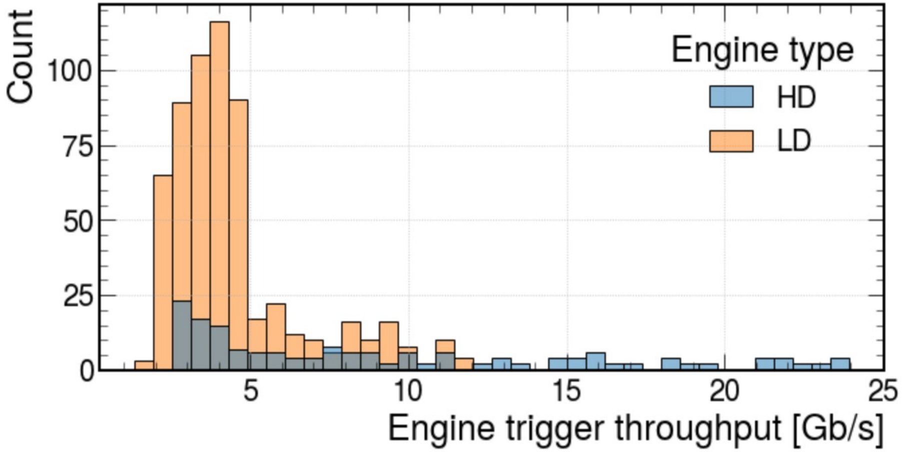
LD-ReadoutTrain Prototype Test System

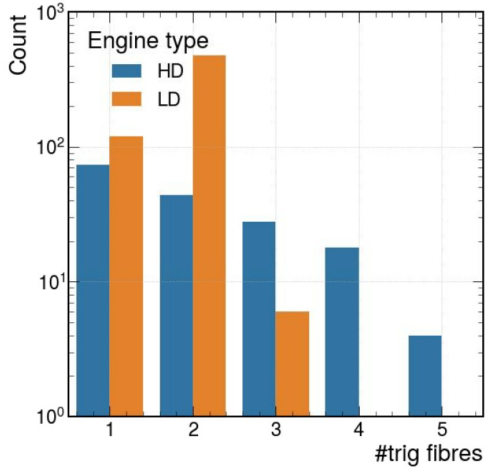


EngineBoard Data and Trigger-Rate Requirements





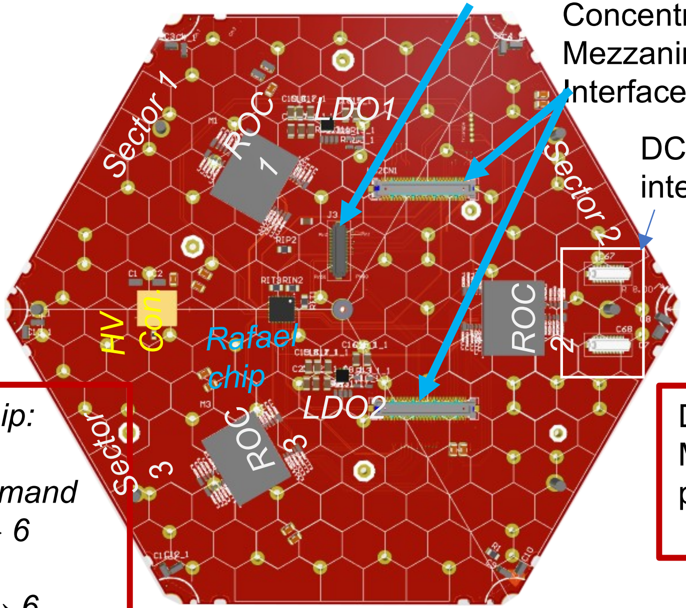




- Very high-rate capacity required
- Data links
  - All LD fit in 1x 10Gb/s link
  - 25% of HD require 2
- Trigger
  - A few LD s require 3 links
    - Threshold
  - A few HD s require up to 5 links
- Mapping
  - Detailed matching of bandwidth requirements to fibres essential

V3-LD-HexBoard Design

3 sectors and reads 192 Si channels (64 ch/sector)
Hosts 3×HGCROC
2× LDOs, Rafael Chip, HV connector,
LD-WagonBoard & DCDC Interfaces



Rafael Chip:

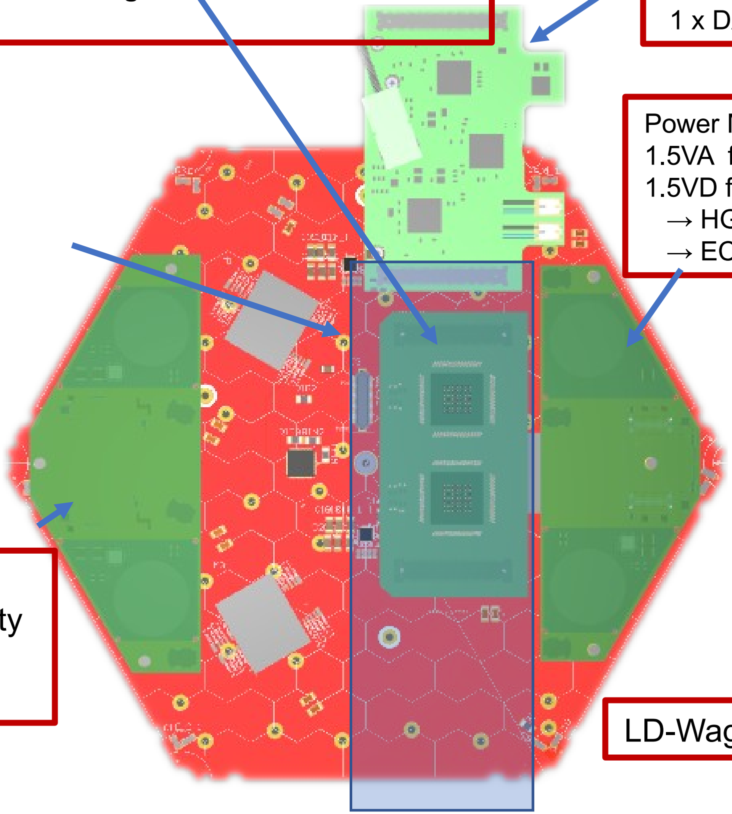
Fast Command
1→ 6
CLK320
1 → 6

LD-HexModule Assembly

Concentrator Mezzanine (CM) :
Inputs from V3-LD-HexBoard
Outputs to Wagon

LD-EngineBoard:
2 x Trigger lpGBTs
1 x DAQ lpGBTs

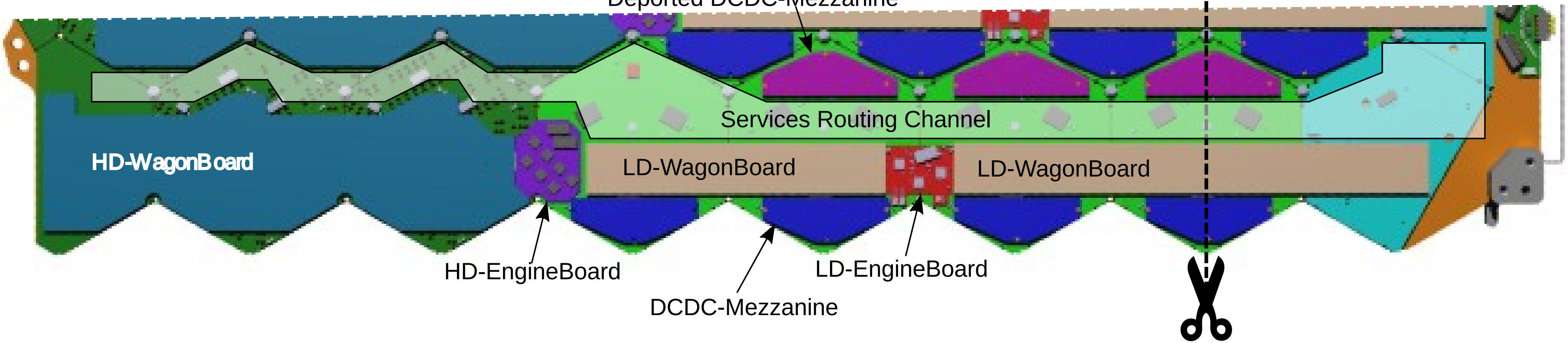
Power Module :
1.5VA for LDO1
1.5VD for LDO2
→ HGCROCs
→ ECONs

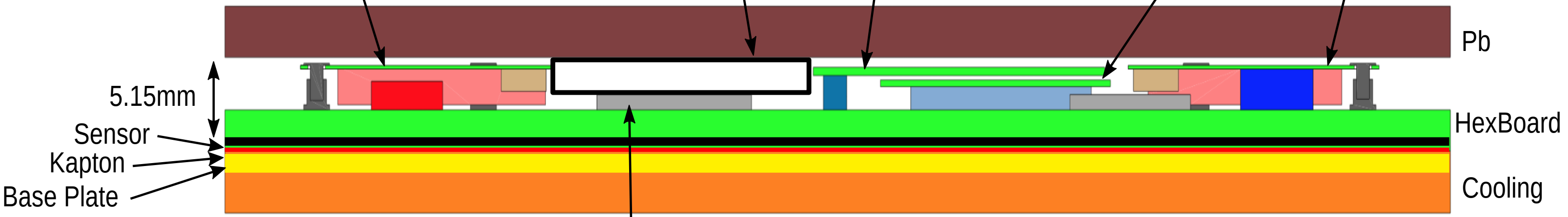


Deported Power Module: High-Density power regulation

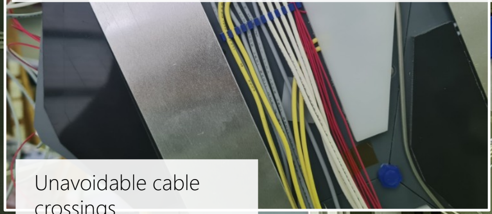
LD-WagonBoard

Services Routing Challenge

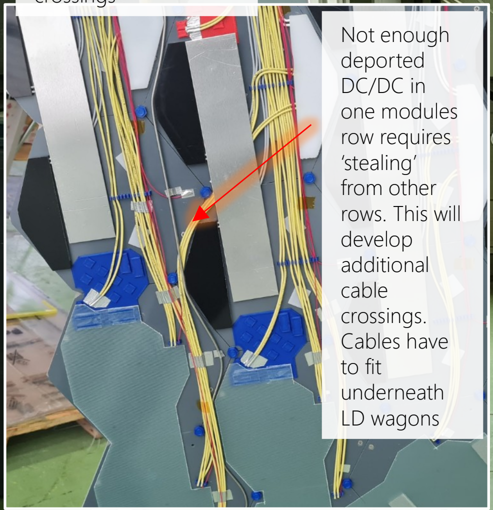




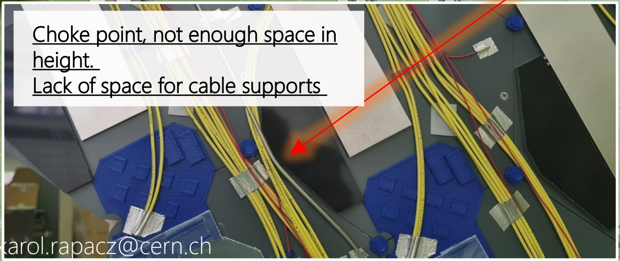
Cassette mockup activity – cassette internal routing



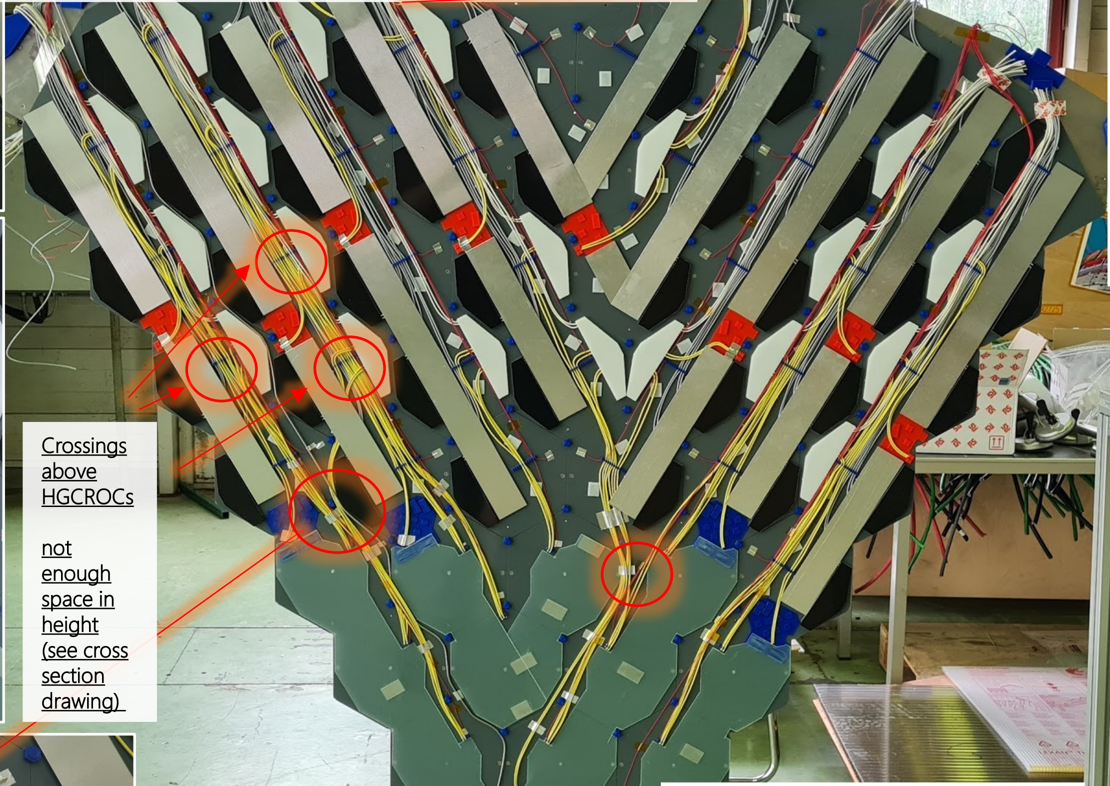
Unavoidable cable crossings



Not enough deported DC/DC in one modules row requires 'stealing' from other rows. This will develop additional cable crossings. Cables have to fit underneath LD wagons

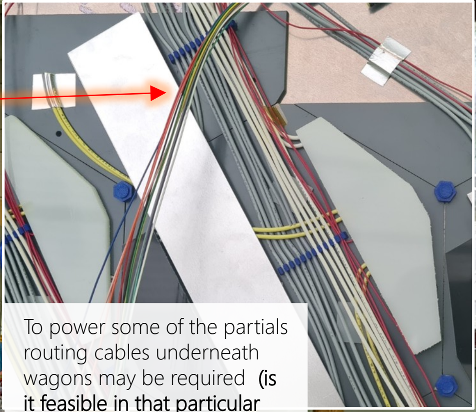


Choke point, not enough space in height.
Lack of space for cable supports

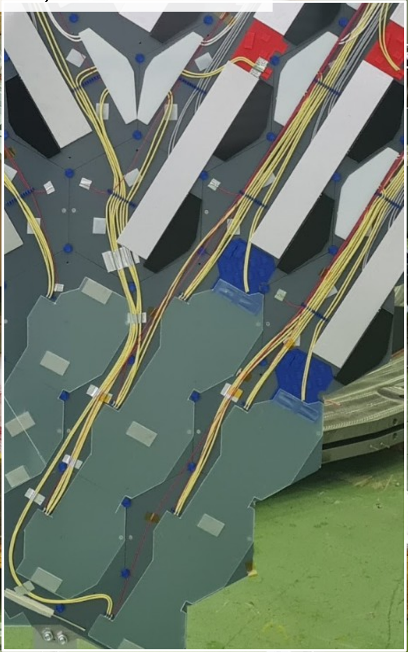


Crossings above HGCROCs

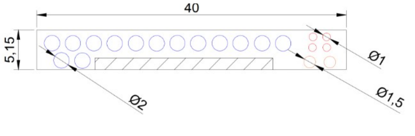
not enough space in height (see cross section drawing)



To power some of the partials routing cables underneath wagons may be required (is it feasible in that particular place?)



Services routing space occupied with cables (with HGCROC)



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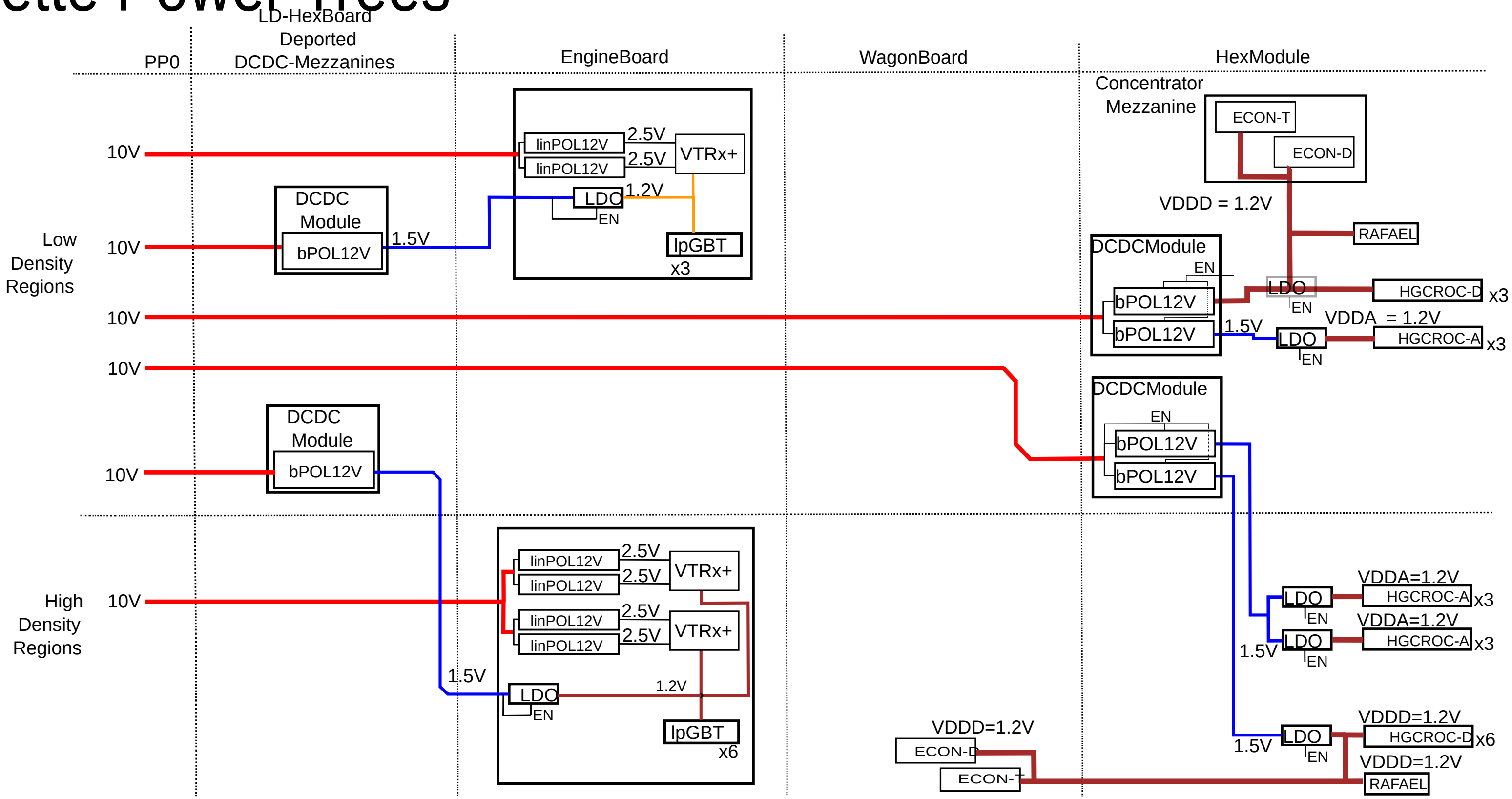
On-Cassette Power Trees



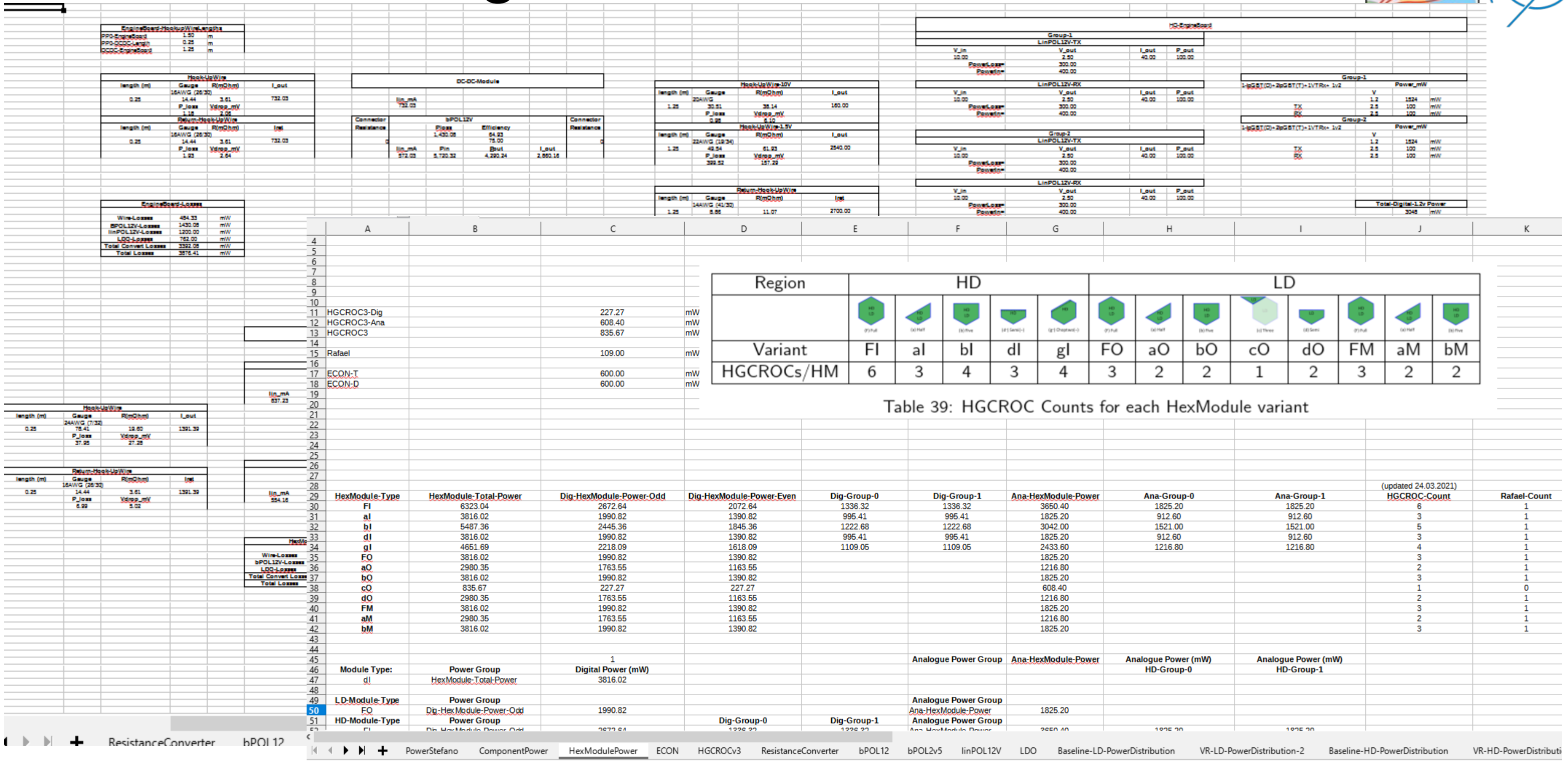
- Common developments where possible
- 10V from outside
  - to go as far as possible into the cassette
  - Routing space

- bPOL12V
- 10V→1.5V/1.2V
- DCDC-Mezzanine cards
- Custom development
- Careful coil optimisation (shape/space)

- LDO
  - 1.5V→1.2V
  - Rad hard custom development for HGCAL
- linPOL12V
  - 10V→ 2.5V
  - Recently adopted to remove bPOL2V5
  - Greatly eases space requirements

On-Cassette Power Modelling

- Geometry and component based model
  - Power referred to at the cassette periphery
- Active components
  - HGCROC, ECONs, RAFAEL
  - VTRx+, lpGBT..
- Converter losses
- Cable losses
- Allows detailed evaluation of
  - Where power is consumed
  - What the losses are
  - Consequences of cable choices
- Cable dimensioning
  - Supply droop and ground offsets
- Measured power consumptions will improve accuracy



HGCROC3-Dig	227.27	mW
HGCROC3-Ana	608.40	mW
HGCROC3	835.67	mW
Rafael	109.00	mW
ECON-T	600.00	mW
ECON-D	600.00	mW

Region	HD					LD							
Variant	Fl	al	bl	dl	gl	FO	aO	bO	cO	dO	FM	aM	bM
HGCROCs/HM	6	3	4	3	4	3	2	2	1	2	3	2	2

Table 39: HGCROC Counts for each HexModule variant

HexModule-Type	HexModule-Total-Power	Dig-HexModule-Power-Odd	Dig-HexModule-Power-Even	Dig-Group-0	Dig-Group-1	Ana-HexModule-Power	Ana-Group-0	Ana-Group-1	HGCROC-Count (updated 24.03.2021)	Rafael-Count
Fl	6323.04	2672.64	2072.64	1336.32	1336.32	3650.40	1825.20	1825.20	6	1
al	3816.02	1990.82	1390.82	995.41	995.41	1825.20	912.60	912.60	3	1
bl	5487.36	2445.36	1845.36	1222.68	1222.68	3042.00	1521.00	1521.00	5	1
dl	3816.02	1990.82	1390.82	995.41	995.41	1825.20	912.60	912.60	3	1
gl	4651.69	2218.09	1618.09	1109.05	1109.05	2433.60	1216.80	1216.80	4	1
FO	3816.02	1990.82	1390.82			1825.20			3	1
aO	2980.35	1763.55	1163.55			1216.80			2	1
bO	3816.02	1990.82	1390.82			1825.20			3	1
cO	835.67	227.27	227.27			608.40			1	0
dO	2980.35	1763.55	1163.55			1216.80			2	1
FM	3816.02	1990.82	1390.82			1825.20			3	1
aM	2980.35	1763.55	1163.55			1216.80			2	1
bM	3816.02	1990.82	1390.82			1825.20			3	1

Nominal	HD			LD		
Type	Full	Partials	Engine	Full	Partials	Engine
Power (W)	14.0	7.6 to 11.5	7.3	6.4	2.1 to 6.4	3.8
Loss (W)	7.6	3.7 to 6.0	3.9	2.6	1.3 to 2.6	2.1
Loss (%)	55	50 to 52	53	41	41 to 60	54

Total Power and losses at PP0 for 2 x 50 layer End-Caps						
	Min		**Nom**		**Max**	
	Power	Loss	Power	Loss	Power	Loss
Total (kW)	223.44	110.86	239.86	112.05	257.34	113.04

Summary and Outlook

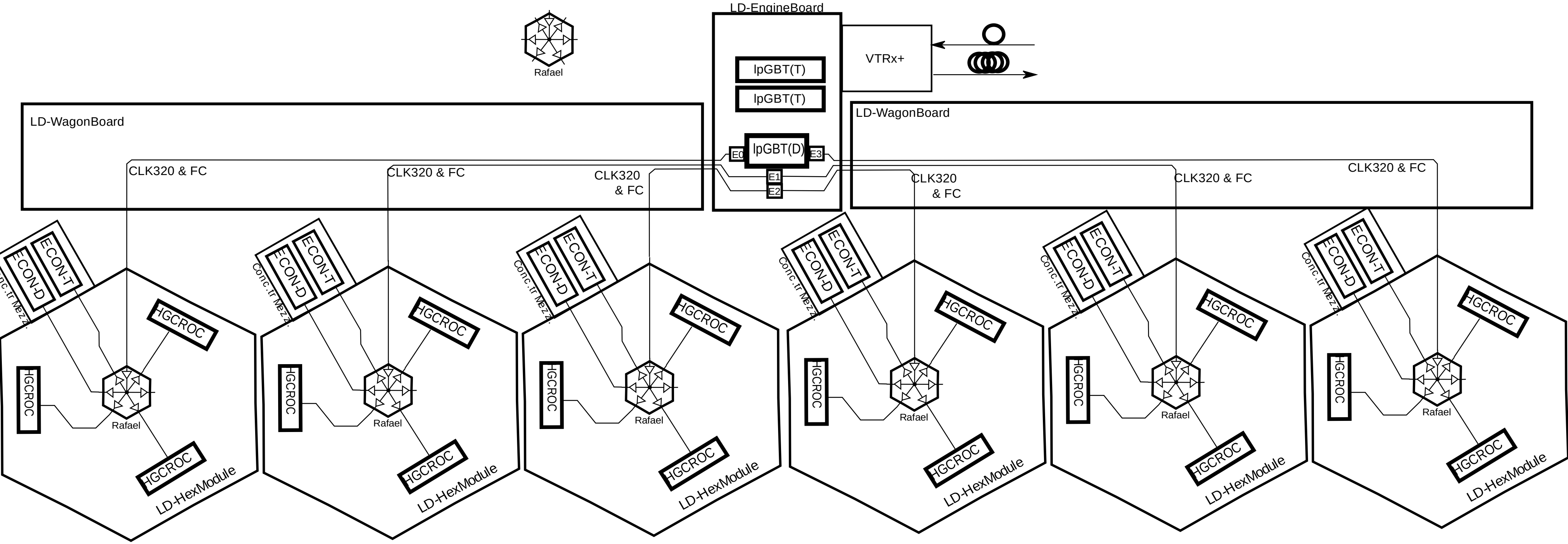
- Very demanding system requirements
  - High data rates
  - Tightly constrained physical volume
  - Huge number of channels
  - Optimal coverage introduces a plethora of variations
  - System has a phenomenology that needs to be explored
- Engine-Wagon architecture defined to respond to this complexity
  - Prototype system under evaluation
- Integrated electromechanical design process is required
  - Electronics engineers must work in synergy with the mechanical engineers
- Mechanical mockup developed in conjunction with very detailed modelling and design in use
- Huge design task remaining
  - Every partial needs similar attention to detail

Thank you for your attention!

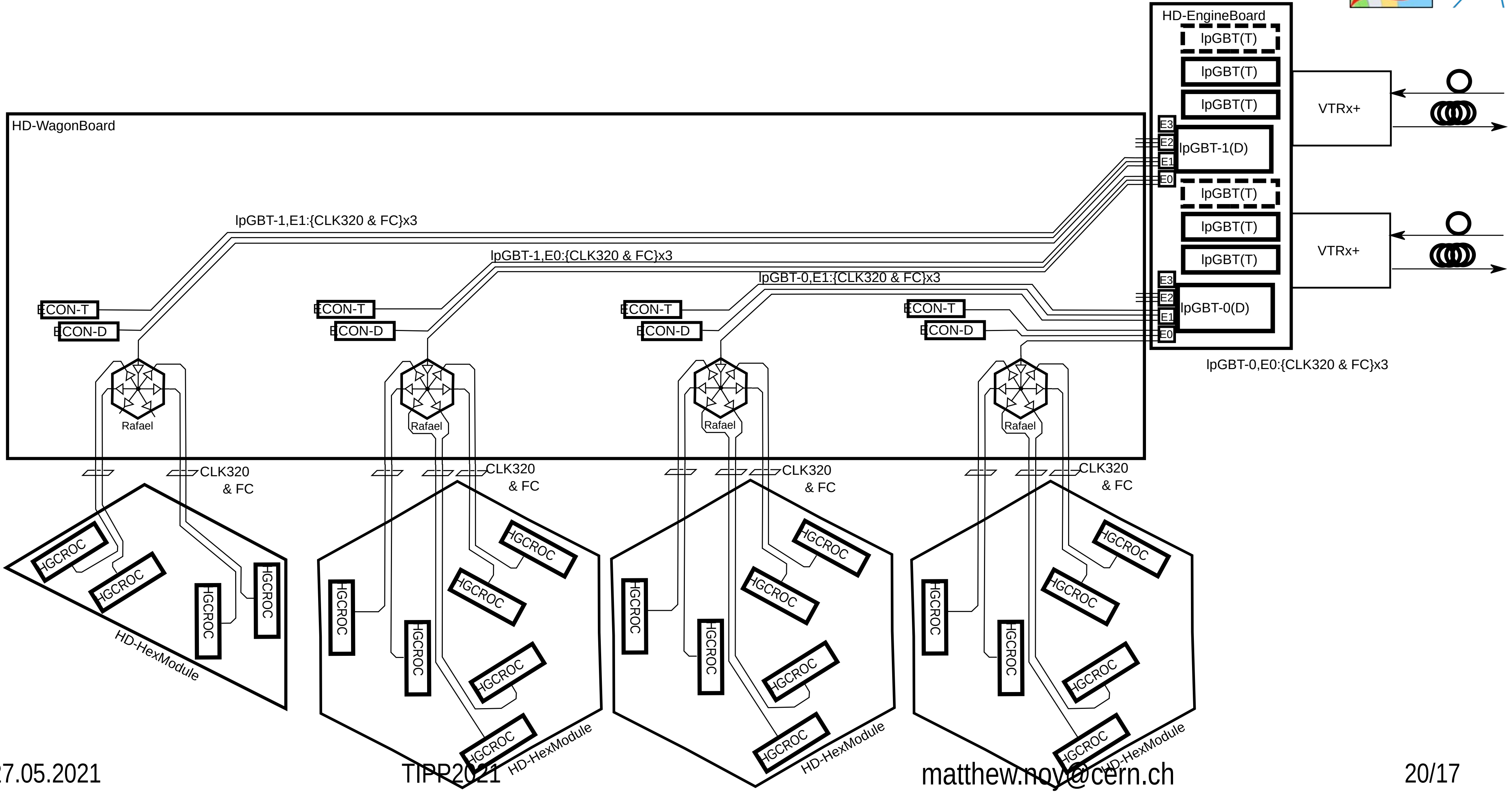
Other HGCAL Contributions

- Clemens Lange: 26.05.2021
  - Beam Tests
  - https://indi.to/nGjyq
- Thorben Quast: 26.05.2021
  - Subdetector Overview
  - https://indi.to/qS3tX
- Mathias Reinecke: 26.05.2021
  - Scintillator Tileboard
  - https://indi.to/BY9Qs
- Damien Thienpont: 28.05.2021
  - HGCROC
  - https://indi.to/6xk3R

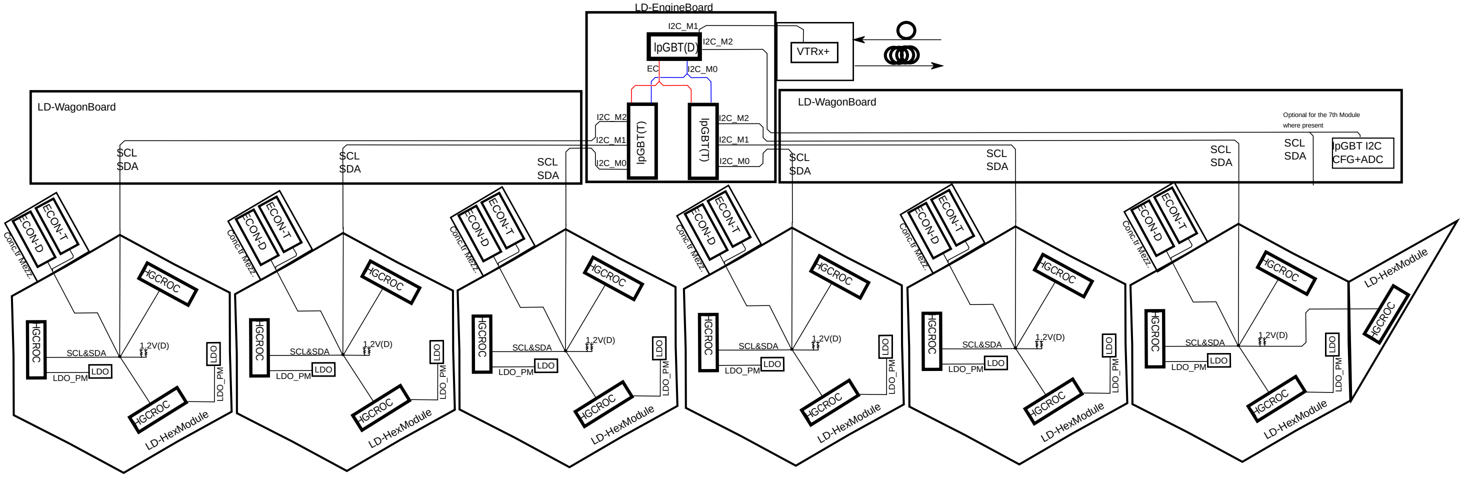
Control Architecture: LD Fast Command



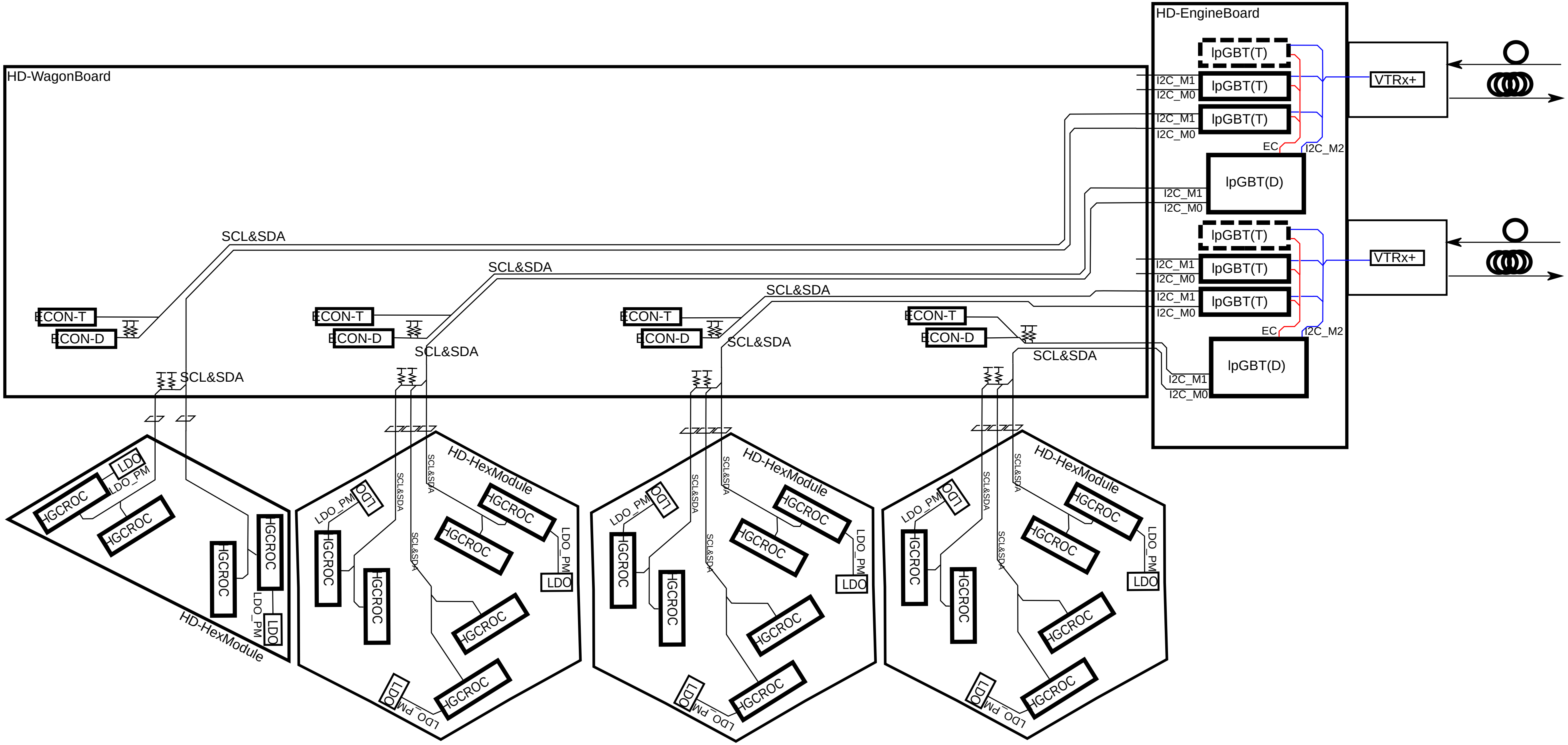
Control Architecture: HD Fast Command



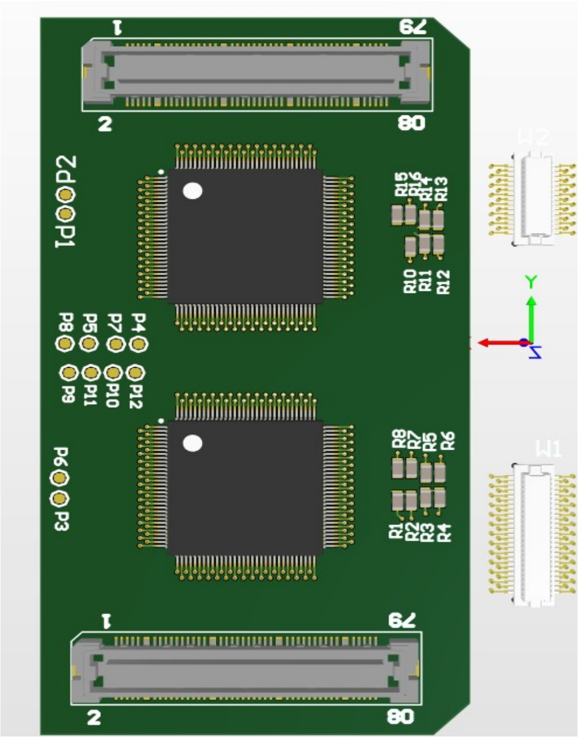
Control Architecture: LD Slow Control

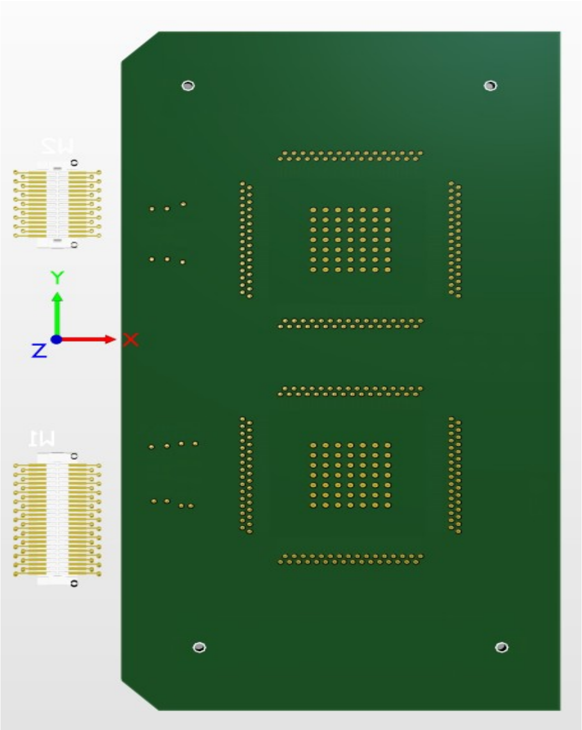


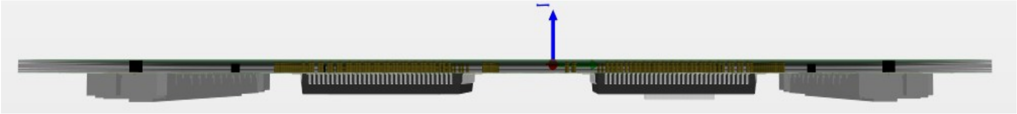
HD Slow Control



Concentrator Mezzanine Card







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