Readout Design Concept for Light Detection in Noble Liquid TPCs using Large Capacitance SiPMs

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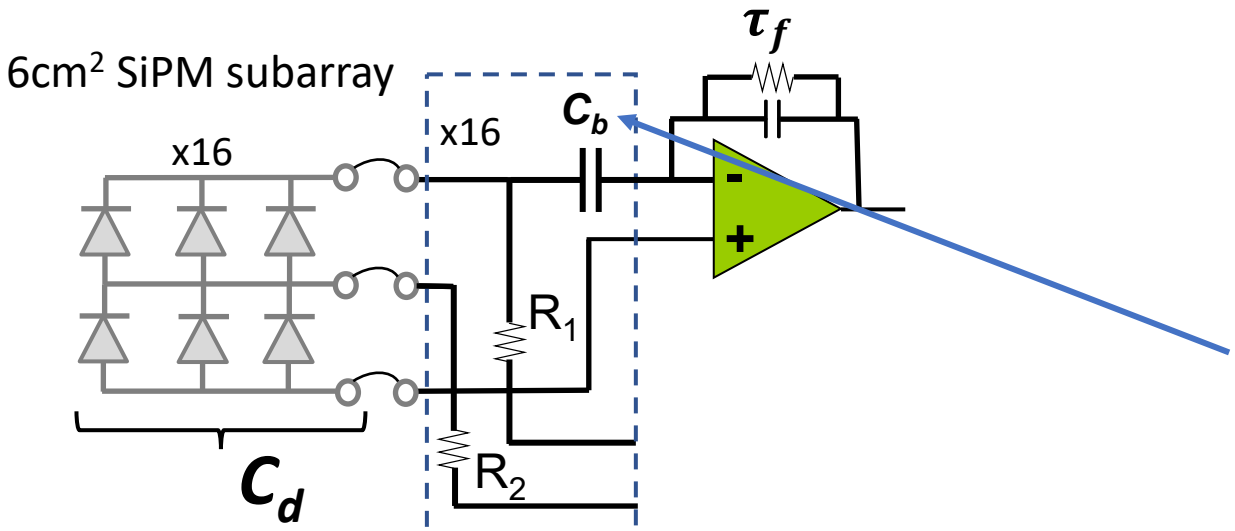
Outline

- The need for large area SiPM light detectors:
  - nEXO SiPM area ~4.6 m^2 ; DUNE ~ tens of m^2
- There is a large mismatch between the "giant" SiPM capacitance C_d (many nanofards) and a tiny input transistor gate capacitance C_g (a few picofarads).
- Conventional approach: Transfer all the SiPM avalanche charge onto an ("current") amplifier – not optimal for $C_d/C_g >> 1$
- *A <u>different approach</u>*: Transfer only a charge that we can "naturally see", due to sharing among the capacitances, onto the input transistor gate.
- *Advantages*: instead of a "giant" (de)coupling capacitor to close the signal circuit, a much smaller capacitor is sufficient; lower power dissipation; SiPM and electronic gain calibration.
- Single and multiple photoelectron response, S/N and timing resolution are demonstrated for 20 nF (6 cm^2) SiPM subarrays operated at low temperature (LN2).

“Giant” SiPM Capacitance

Technology	“HPK”	“FBK”
C/A [nF/cm^2]	3.5	8.5
V_{op} [V]	60	30
C_{6cm^2} [nF]	**21**	**51**
C_{2s} [nF]	**5**	**12.5**
V_{2s} [V]	120	60



Assumptions (approx.):

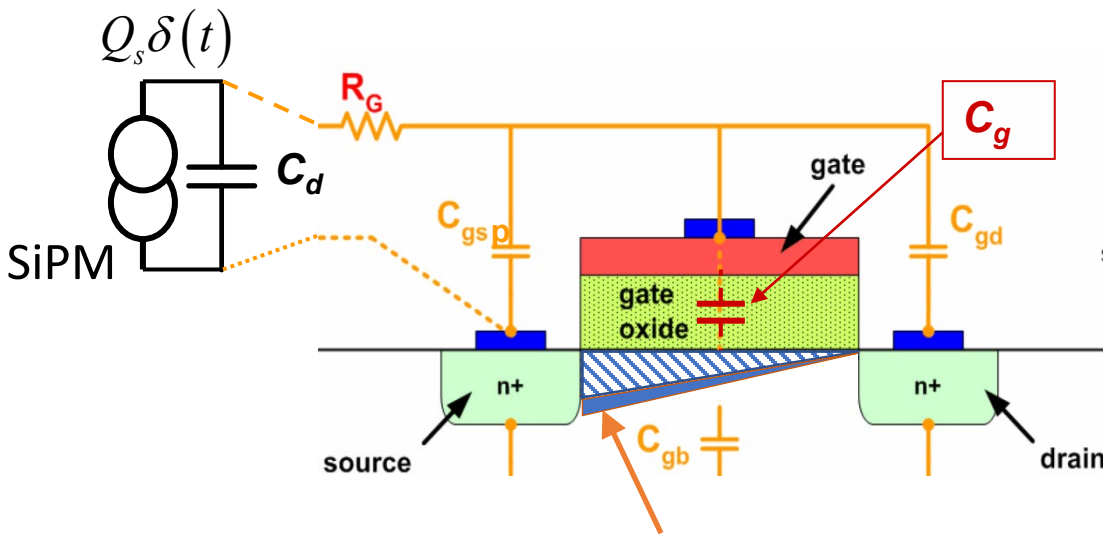
- Number of readout channels in nEXO ~8000x6cm² for a SIPM area of ~4.8 m²

Why “*Giant*”?

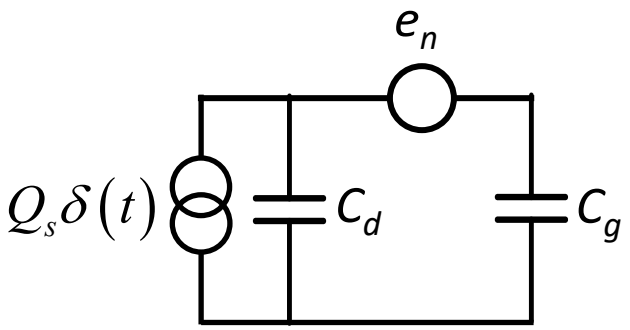
SiPM capacitance C_d (in any practical arrangement) is much higher than in any known detector

- C_d is large, but so is the charge/pe, Q_s ~ 0.4 pC (2.4 x 10^6 e^-)
- *The charge is bound to that giant capacitance: can we “see” it??*
- *How to “extract” the charge while applying the bias to SiPMs?*
- *Does C_b, the decoupling (radio pure) HV capacitor have also to be “giant”?*

SiPM – transistor capacitance mismatch
- how much of the avalanche signal charge do we really "see"?



"useful" charge: Q_g modulates the channel and with transistor noise determines S/N



$$\frac{Q_g}{Q_s} = \frac{C_g}{C_g + C_d} \cong \frac{C_g}{C_d}$$

for $C_d \gg C_g$

Example:

C_d=10 nF

C_g =25pF (very large transistor)

$(Q_g/Q_s)=(Cg/Cd)=1/400$

We "see" only **1/400** of the SiPM avalanche charge.

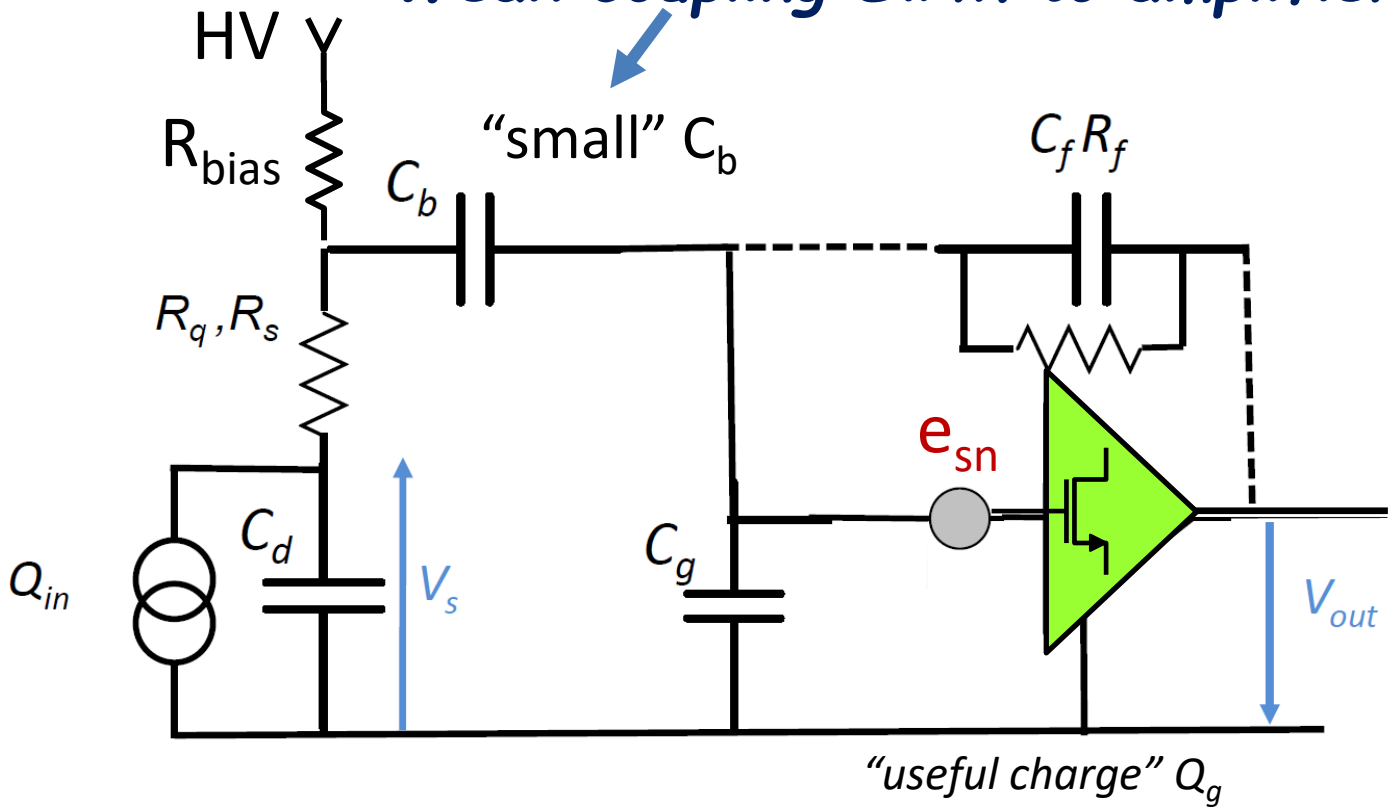
A long way to an ideal capacitance match:

$(Q_g/Q_s)_{max}$ = ½

for $(C_g/C_d)=1$

Should we think of something different?

Weak coupling SiPM to amplifier



$$\frac{v_{out}}{Q_{in}} = \frac{1}{C_f} \cdot \frac{1}{1+\frac{C_d}{C_b}}$$

$$for\ \frac{C_d}{C_b} \gg 1 \rightarrow \frac{v_{out}}{Q_{in}} \approx \frac{1}{C_f} \times \frac{C_b}{C_d}$$

Do we need ***feedback***? Not needed but useful; it defines the gain (charge sensitivity) and the response.
Feedback cannot improve S/N (it "feeds" back both signal and noise).
With feedback this is just a classical Charge Sensitive Amplifier.

The result: ***C_b has to be larger than C_g, but can be much smaller than C_d:***

$$\left(\frac{S}{N}\right)_n = \frac{Q_{in}/C_d}{e_{sn}/t_p^{1/2}} \cdot \frac{n}{1+C_g/C_b+n^2 C_g/C_d}$$

n= series connection
(slide 7, n=2)

"useful charge" Q_g

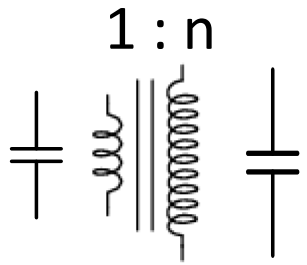
$$\frac{Q_g}{Q_{in}} = \frac{C_g}{C_d} \cdot \underbrace{\frac{1}{1+\frac{C_g}{C_b}+\frac{C_g}{C_d}}}_{\sim 1\ for\ \frac{C_d}{C_b} \gg 1\ ;\ \frac{C_b}{C_g} \gg 1}$$

$C_d > C_b >> C_g$

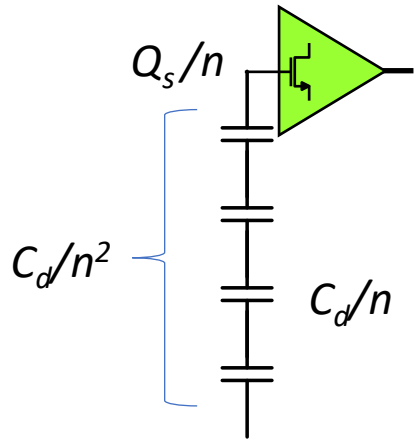
Toward matching …

$$ENC = \frac{e_n}{\tau^{1/2}}\left(\frac{C_d}{n} + nC_{gs}\right) \qquad n_{opt} = \left(\frac{C_d}{C_{gs}}\right)^{1/2} \qquad \boldsymbol{ENC_{sopt}} = 2\frac{\boldsymbol{e_n}\left(\boldsymbol{C_d C_{gs}}\right)^{1/2}}{\boldsymbol{\tau_p^{1/2}}}$$

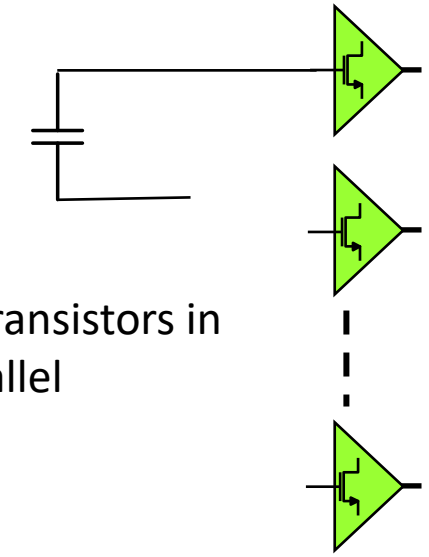
n= transformation ratio for EM and ES transformers = (number of transistors in parallel)$^{1/2}$



EM transformer, the best and proven, but not radio pure



Electrostatic transfomer



n² transistors in parallel

For C_d=10000 pf:

$$C_g = 25pF \rightarrow n_{opt} = \sqrt{C_d/C_g} \cong 20$$

ENC is reduced by: $\frac{1}{2}\sqrt{C_d/C_g} = 10$

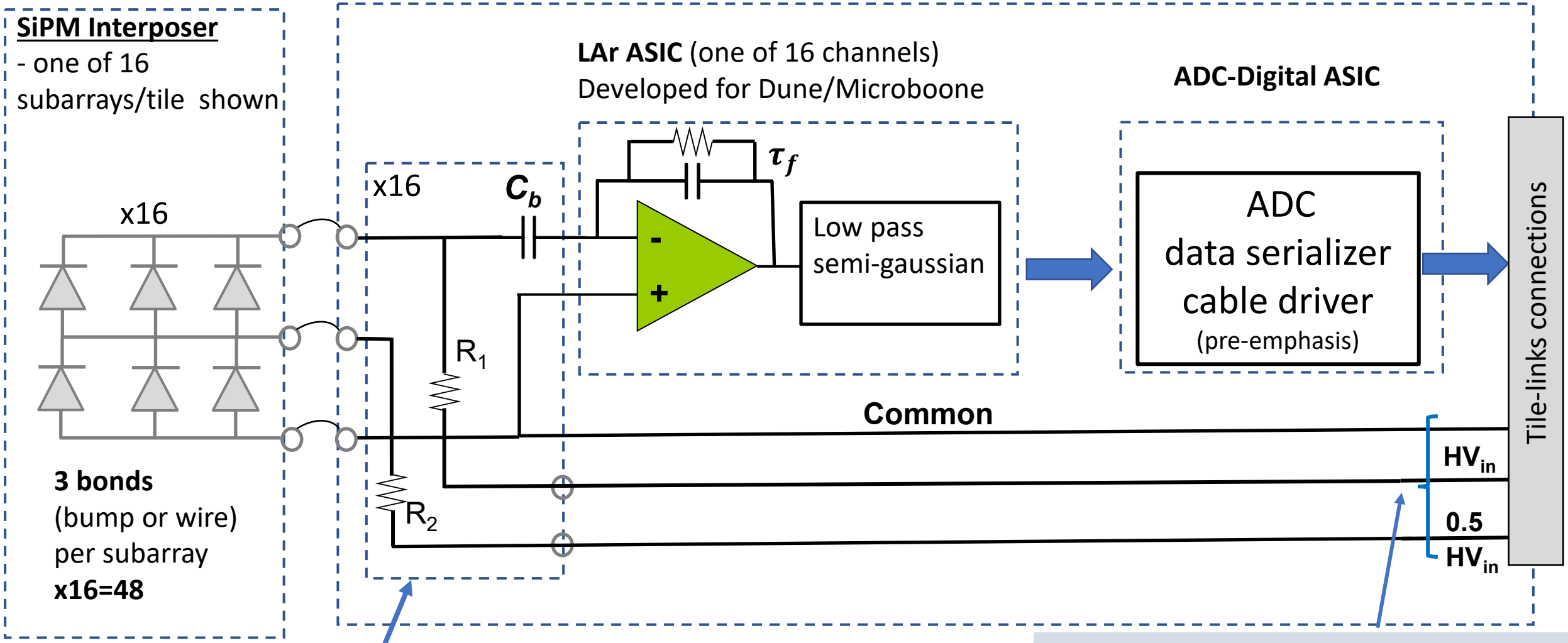
ES transformer n=4 will improve S/N by a factor of ~ 3.95 ; n=2 by a factor of ~2, compared to parallel connection of SiPMs.

It would take **16(4)** times as many transistors ***and power*** for the same result as with ES transformer

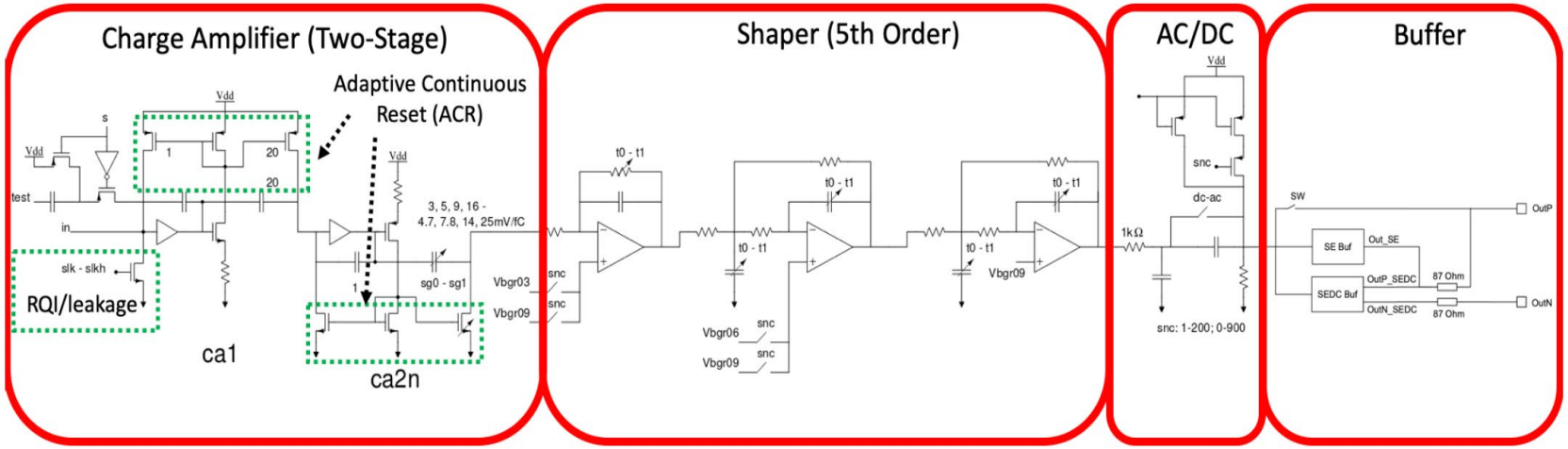
Cannot connect too many in SiPMs in series: excessive high voltage, need of HV capacitor

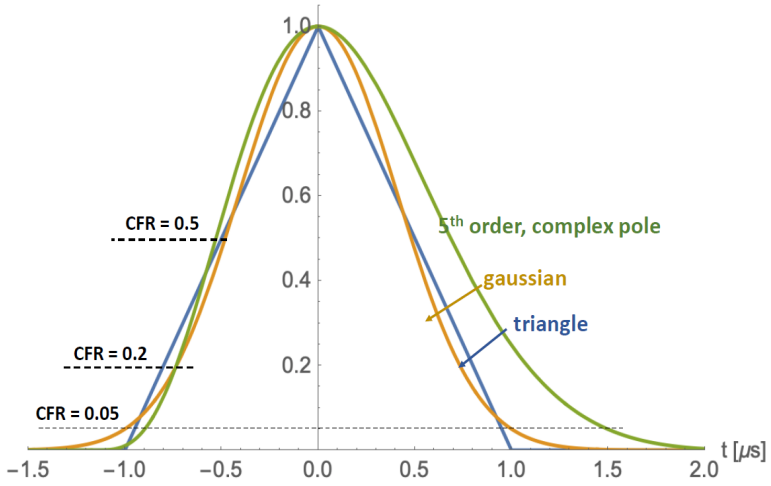
SiPM Readout: Interposer and Electronics Daughterboard

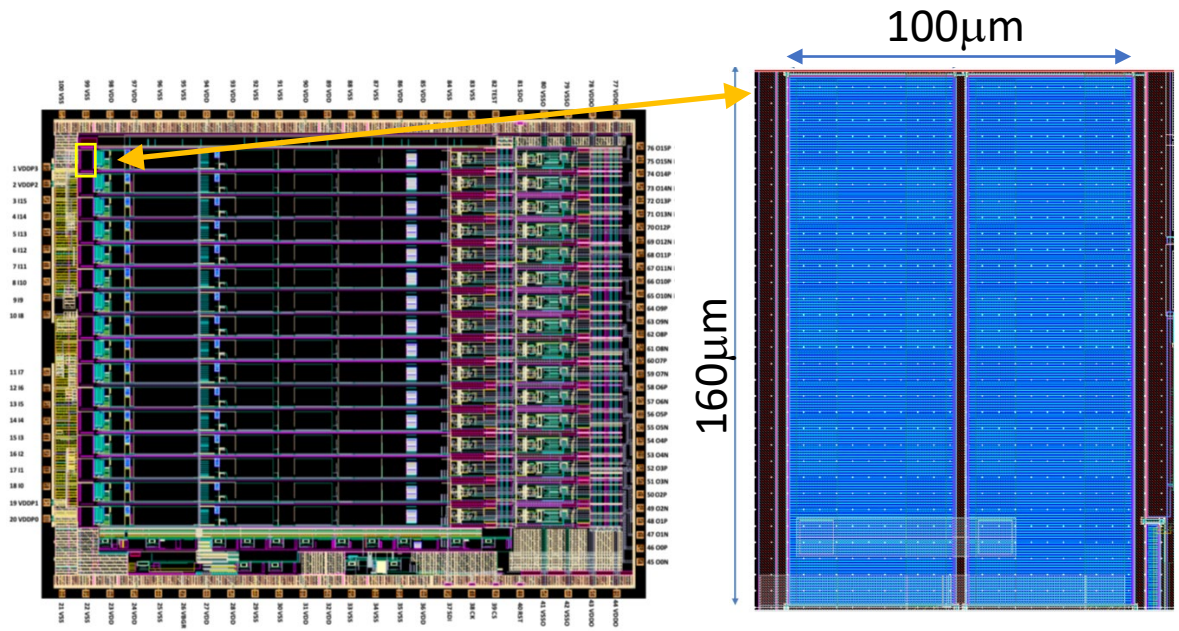
Two-ASICs approach -



LArASIC = Antialiasing Filter

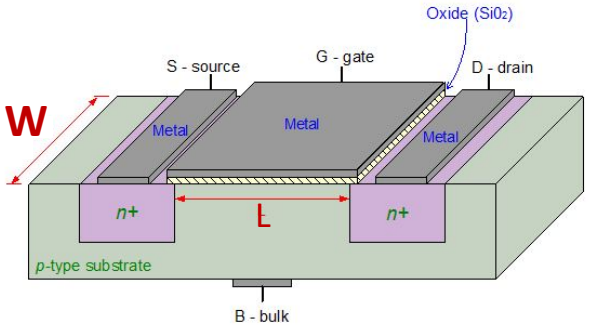






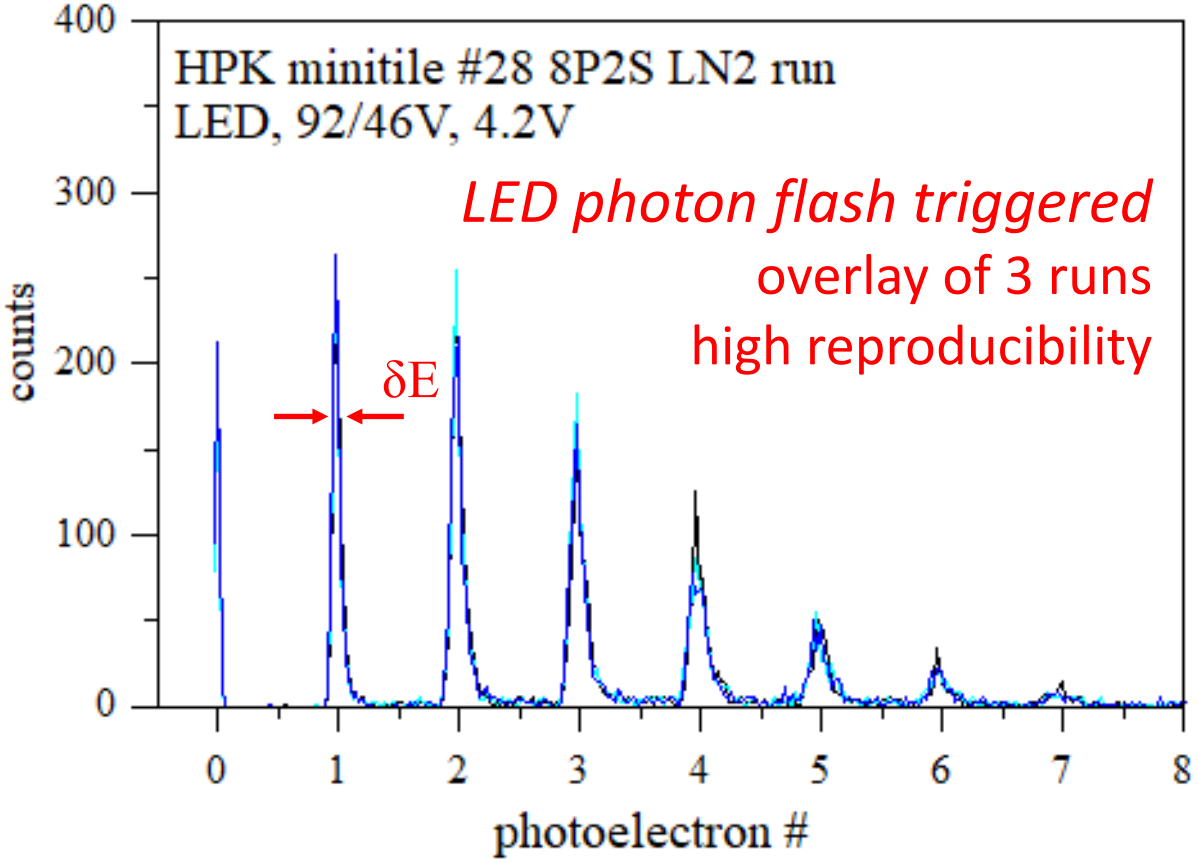
160μm x 100μm=16,000μm^2

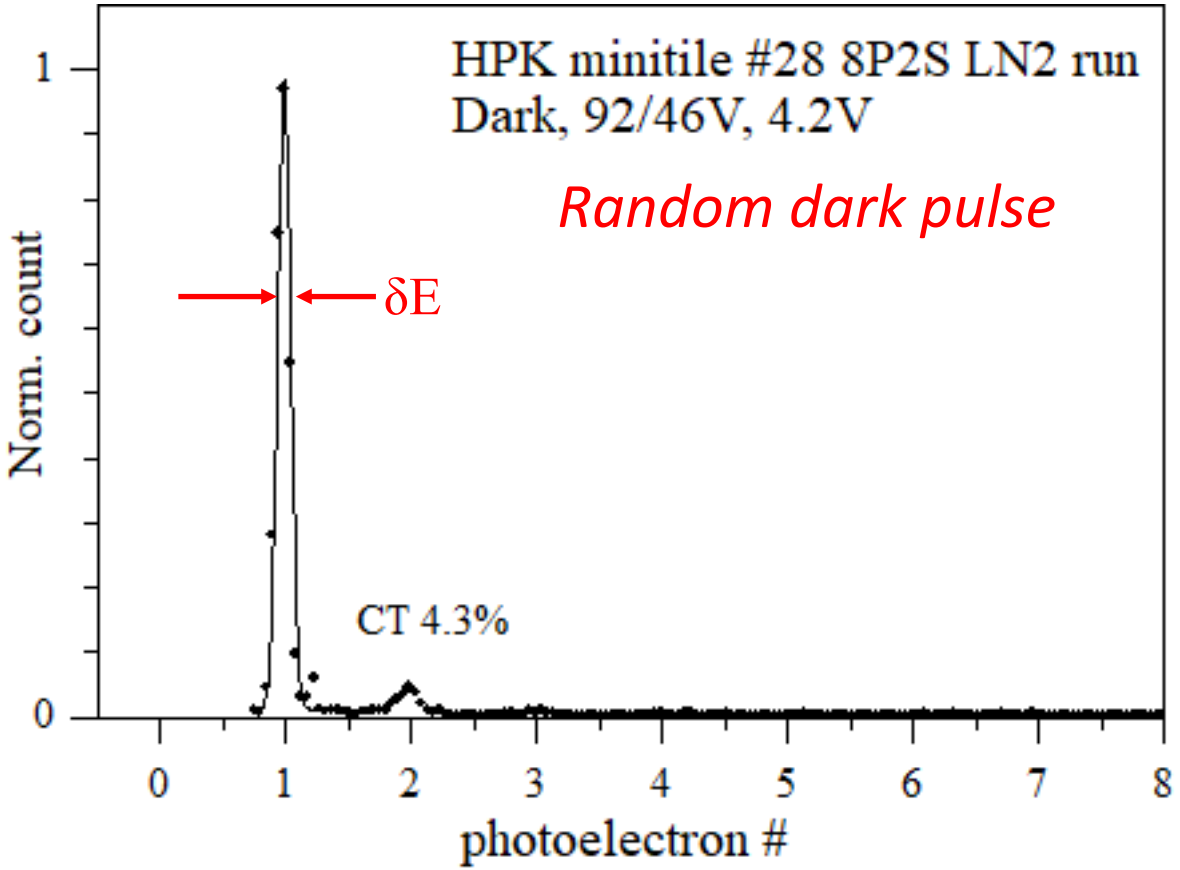
$$W/L = \frac{20\ mm}{270\ nm}$$



For a *very large low noise PMOS transistor* W~20mm, L~270nm, W/L~4x10^4, C_g~20pF ;
The transistor can never match a nanofarad SiPM;
This very large transistor is a small fraction (~1/400) of the SiPM capacitance.

SiPM Minitile (6 cm^2) : Charge Histogram, LN_2

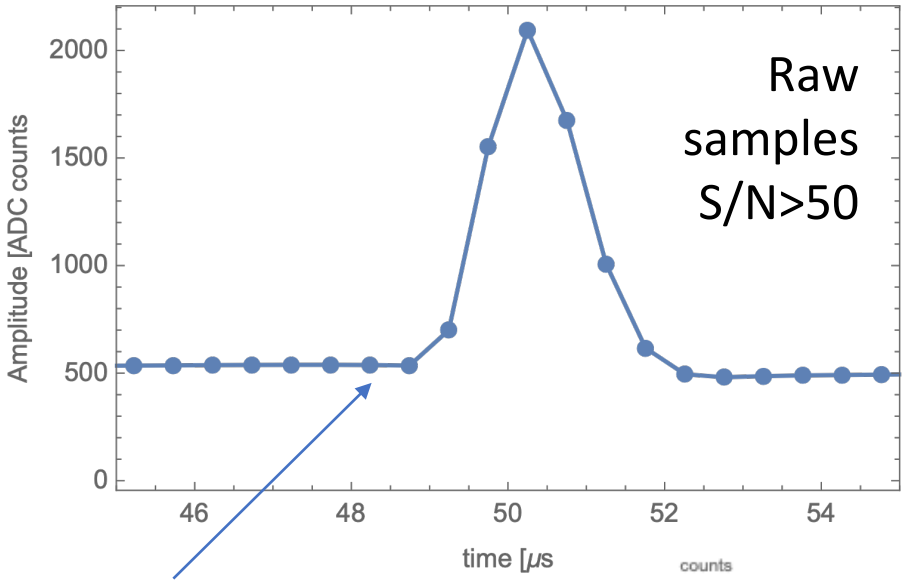




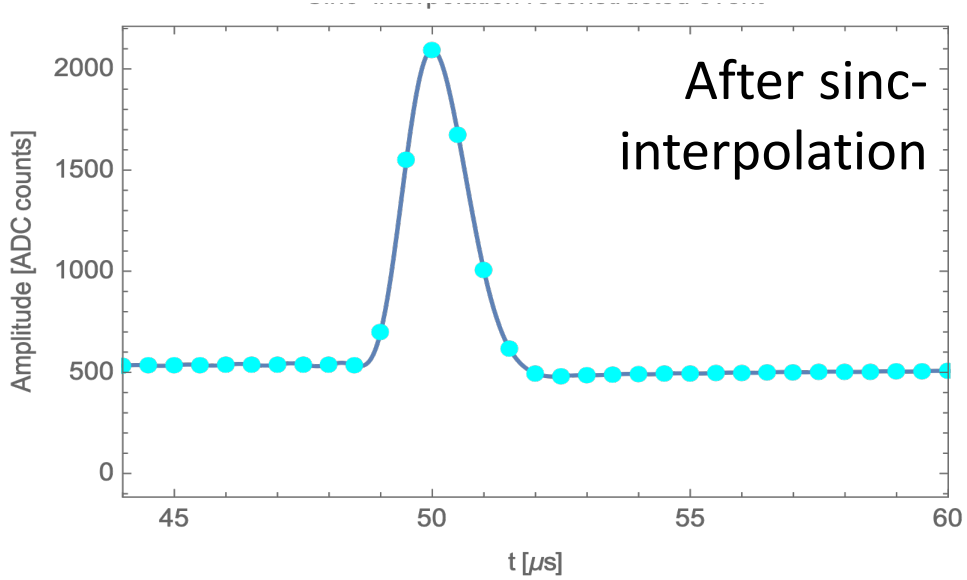
Photon rate: ~80 Hz (trigger rate 100 Hz)
1-pe resolution (δE): 3 to 3.5% rms

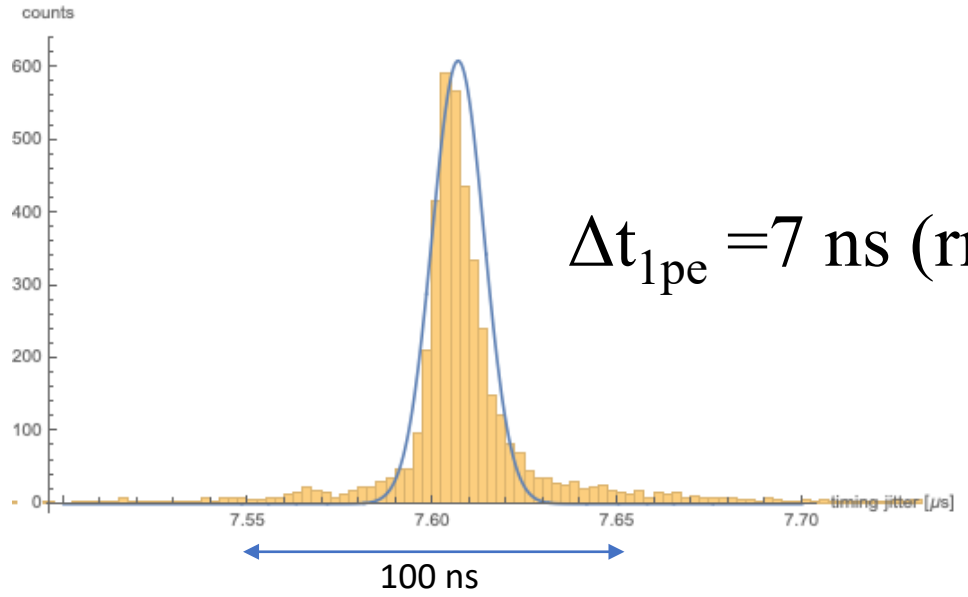
DCR: ~96 Hz (0.17 Hz/mm^2)
1-pe resolution (δE): ~ 5% rms

Waveform reconstruction and single-photon timing resolution (SPTR)



10 μs = 20 samples at 2Msps





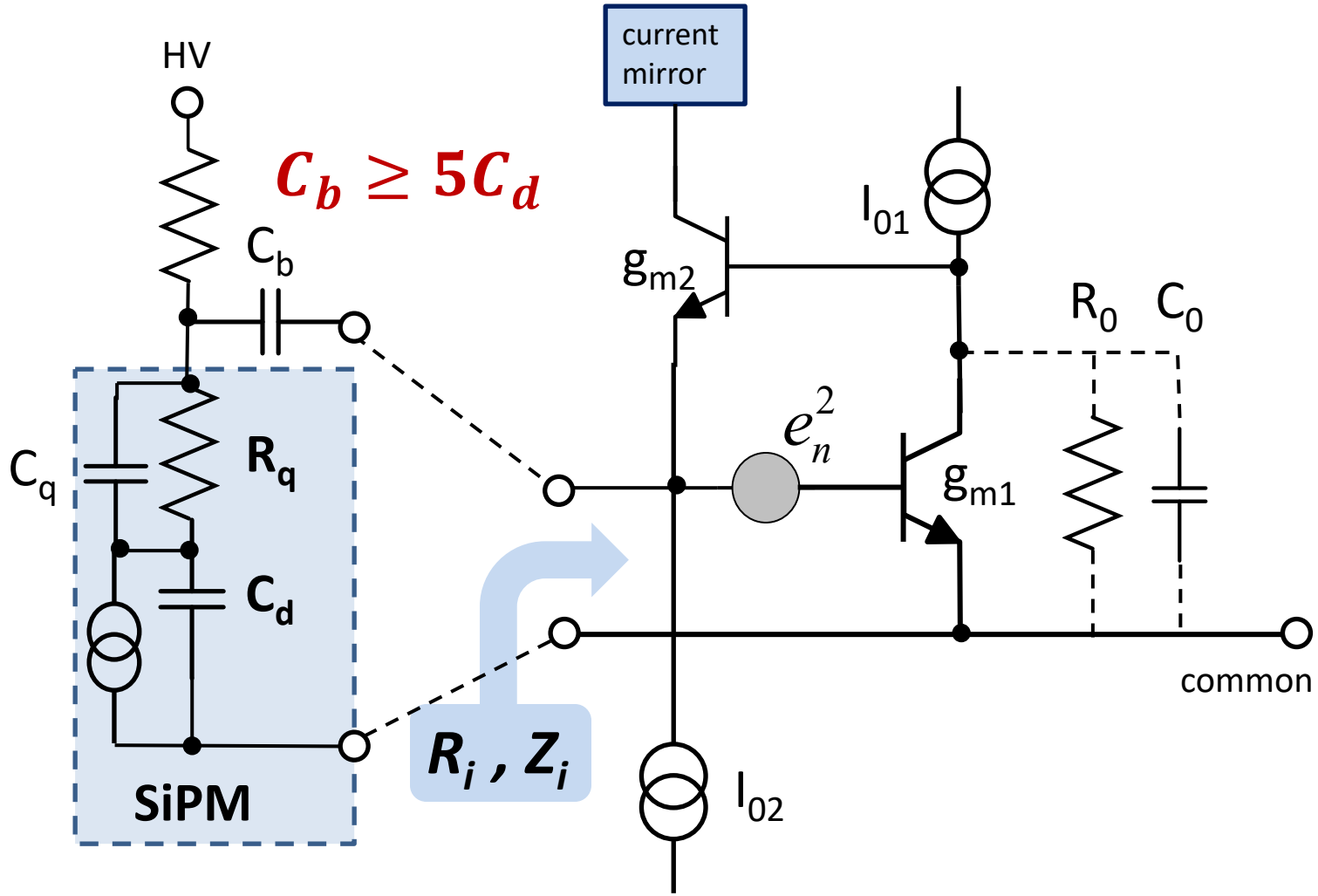
Δt_{1pe} =7 ns (rms)

Using sinc-interpolation + 'digital' constant fraction discriminator, leads to a low timing error (SPTR)

Summary

- In a conventional approach using a “current amplifier”, or any other, both the signal and series noise are affected equally by amplifier feedback, and S/N ratio remains unaffected by feedback.
- With large SiPM capacitance grossly mismatched to even the largest input transistor, transfer of charge from SiPM via a large (de)coupling capacitor ($C_b > C_d$,i.e., strong coupling) does not contribute to S/N.
- Due to a large mismatch, **a *weak coupling*** between the SiPM and the input transistor is sufficient, where $C_d > C_b >> C_g$. Most appropriate configuration for realization of this concept is a charge sensitive amplifier (CSA), coupled to SiPMs by a decoupling capacitor an order of magnitude smaller than SiPM capacitance (C_b~200-500pF for 5-10 nF SiPM subarray)
- The LAr FE ASIC for MicroBooNE, protoDUNE and SBND (“LArASIC”), has the required characteristics, and it has made possible experimental verification of the noise calculation. SiPM response, S/N, and timing resolution have been demonstrated.

SiPM Readout by “Current Feedback Amplifier”?



- A large (de)coupling capacitor C_b is required.
- There are additional noise sources in the “Current Feedback Amplifier” besides the input transistor