Readout Design Concept for Light Detection in Noble Liquid TPCs using Large Capacitance SiPMs


25 May 2021
Outline

• The need for large area SiPM light detectors:
  - nEXO SiPM area ~4.6 m^2 ; DUNE ~ tens of m^2

• There is a large mismatch between the “giant” SiPM capacitance $C_d$ (many nanofarads) and a tiny input transistor gate capacitance $C_g$ (a few picofarads).

• Conventional approach: Transfer all the SiPM avalanche charge onto an (“current”) amplifier – not optimal for $C_d/C_g >> 1$

• A different approach: Transfer only a charge that we can “naturally see”, due to sharing among the capacitances, onto the input transistor gate.

• Advantages: instead of a “giant” (de)coupling capacitor to close the signal circuit, a much smaller capacitor is sufficient; lower power dissipation; SiPM and electronic gain calibration.

• Single and multiple photoelectron response, S/N and timing resolution are demonstrated for 20 nF (6 cm^2) SiPM subarrays operated at low temperature (LN2).
“Giant” SiPM Capacitance

<table>
<thead>
<tr>
<th>Technology</th>
<th>“HPK”</th>
<th>“FBK”</th>
</tr>
</thead>
<tbody>
<tr>
<td>C/A [nF/cm^2]</td>
<td>3.5</td>
<td>8.5</td>
</tr>
<tr>
<td>V_{op} [V]</td>
<td>60</td>
<td>30</td>
</tr>
<tr>
<td>C_{6cm^2} [nF]</td>
<td>21</td>
<td>51</td>
</tr>
<tr>
<td>C_{2s} [nF]</td>
<td>5</td>
<td>12.5</td>
</tr>
<tr>
<td>V_{2s} [V]</td>
<td>120</td>
<td>60</td>
</tr>
</tbody>
</table>

Why “Giant”?
SiPM capacitance $C_d$ (in any practical arrangement) is much higher than in any known detector

- $C_d$ is large, but so is the charge/pe, $Q_s \sim 0.4 \text{ pC} (2.4 \times 10^6 \text{ e}^{-})$
- The charge is bound to that giant capacitance: can we “see” it??
- How to “extract” the charge while applying the bias to SiPMs?
- Does $C_b$, the decoupling (radio pure) HV capacitor have also to be “giant”?

Assumptions (approx.):
- Number of readout channels in nEXO $\sim$8000x6cm² for a SIPM area of $\sim$4.8 m²
SiPM – transistor capacitance mismatch
- how much of the avalanche signal charge do we really “see”?

\[
\frac{Q_g}{Q_s} = \frac{C_g}{C_g + C_d} \approx \frac{C_g}{C_d}
\]

for \(C_d \gg C_g\)

Example:
\(C_d = 10\) nF
\(C_g = 25\) pF (very large transistor)

\(\frac{Q_g}{Q_s} = \frac{C_g}{C_d} = 1/400\)

We “see” only \(1/400\) of the SiPM avalanche charge.

A long way to an ideal capacitance match:

\(\frac{Q_g}{Q_s}\) max = \(\frac{1}{2}\)

for \(C_g/C_d = 1\)
Should we think of something different?

**Weak coupling SiPM to amplifier**

\[
\frac{v_{out}}{Q_{in}} = \frac{1}{C_f} \cdot \frac{1}{1 + \frac{C_d}{C_b}}
\]

\[\text{for } \frac{C_d}{C_b} \gg 1 \rightarrow \frac{v_{out}}{Q_{in}} \approx \frac{1}{C_f} \times \frac{C_b}{C_d}\]

Do we need **feedback**? Not needed but useful; it defines the gain (charge sensitivity) and the response. **Feedback cannot improve S/N** (it “feeds” back both signal and noise).

With feedback this is just a classical Charge Sensitive Amplifier.

The result: **$C_b$ has to be larger than $C_g$, but can be much smaller than $C_d$:**

\[
C_d > C_b >> C_g
\]

$n$= series connection (slide 7, n=2)
Toward matching ... 

\[ ENC = \frac{e_n}{\tau^{1/2}} \left( \frac{C_d}{n} + nC_{gs} \right) \]

\[ n_{opt} = \left( \frac{C_d}{C_{gs}} \right)^{1/2} \]

\[ ENC_{sop} = 2 \frac{e_n}{\tau_p^{1/2}} \left( \frac{C_d C_{gs}}{n^2} \right)^{1/2} \]

\[ n = \text{transformation ratio for EM and ES transformers} = (\text{number of transistors in parallel})^{1/2} \]

\[ \frac{1}{n} \]

EM transformer, the best and proven, but not radio pure

\[ C_d = 10000 \text{ pf} \]

\[ C_g = 25pF \rightarrow n_{opt} = \sqrt{\frac{C_d}{C_g}} \approx 20 \]

ENC is reduced by: \[ \frac{1}{2} \sqrt{\frac{C_d}{C_g}} = 10 \]

ES transformer \( n=4 \) will improve S/N by a factor of \( \sim 3.95 \); \( n=2 \) by a factor of \( \sim 2 \), compared to parallel connection of SiPMs.

It would take 16(4) times as many transistors and power for the same result as with ES transformer.

Cannot connect too many in SiPMs in series: excessive high voltage, need of HV capacitor.
SiPM Readout: Interposer and Electronics Daughterboard

**Two-ASICs approach**

- **SiPM Interposer**
  - one of 16 subarrays/tile shown

- **LAr ASIC** (one of 16 channels)
  - Developed for Dune/Microboone

- **ADC-Digital ASIC**
  - ADC data serializer
  - cable driver (pre-emphasis)

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**Diagram Details**

- **SiPM Interposer**
  - 3 bonds (bump or wire) per subarray
  - 16 subarrays = 48 bonds

- **LAr ASIC**
  - One of 16 sets of R1, R2, Cb is shown

- **ADC-Digital ASIC**
  - Common for all 24 tiles in a stave

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**Equation**

\[
\tau_f = \frac{1}{f_0}
\]

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**Text Notes**

- **Prefix** common for all 24 tiles in a stave
- **Prefix** 320 SiPM subarray (“minitiles”)
LArASIC = Antialiasing Filter

For a very large low noise PMOS transistor $W \approx 20\,\text{mm}$, $L \approx 270\,\text{nm}$, $W/L \approx 4 \times 10^4$, $C_g \approx 20\,\text{pF}$; The transistor can never match a nanofarad SiPM; This very large transistor is a small fraction ($\approx 1/400$) of the SiPM capacitance.

$W/L = \frac{20\,\text{mm}}{270\,\text{nm}}$

$160\,\mu\text{m} \times 100\,\mu\text{m} = 16,000\,\mu\text{m}^2$
SiPM Minitile (6 cm^2) : Charge Histogram, LN₂

 Photon rate: ~80 Hz (trigger rate 100 Hz)
 1-pe resolution (δE): 3 to 3.5% rms

 LED photon flash triggered overlay of 3 runs high reproducibility

 DCR: ~96 Hz (0.17 Hz/mm²)
 1-pe resolution (δE): ~5% rms

Random dark pulse
Waveform reconstruction and single-photon timing resolution (SPTR)

After sinc-interpolation

Raw samples
S/N > 50

\[ \Delta t_{1pe} = 7 \text{ ns (rms)} \]

Using sinc-interpolation + ‘digital’ constant fraction discriminator, leads to a low timing error (SPTR)
Summary

- In a conventional approach using a “current amplifier”, or any other, both the signal and series noise are affected equally by amplifier feedback, and S/N ratio remains unaffected by feedback.

- With large SiPM capacitance grossly mismatched to even the largest input transistor, transfer of charge from SiPM via a large (de)coupling capacitor ($C_b > C_d$, i.e., strong coupling) does not contribute to S/N.

- Due to a large mismatch, a weak coupling between the SiPM and the input transistor is sufficient, where $C_d > C_b >> C_g$. Most appropriate configuration for realization of this concept is a charge sensitive amplifier (CSA), coupled to SiPMs by a decoupling capacitor an order of magnitude smaller than SiPM capacitance ($C_b \sim 200$-$500$ pF for 5-10 nF SiPM subarray).

- The LAr FE ASIC for MicroBooNE, protoDUNE and SBND (“LArASIC”), has the required characteristics, and it has made possible experimental verification of the noise calculation. SiPM response, S/N, and timing resolution have been demonstrated.
SiPM Readout by “Current Feedback Amplifier”? 

- A large (de)coupling capacitor $C_b$ is required.
- There are additional noise sources in the “Current Feedback Amplifier” besides the input transistor.

$C_b \geq 5C_d$