A low-power sparsified readout for the MAPS-based High Energy Particle Detector space tracker

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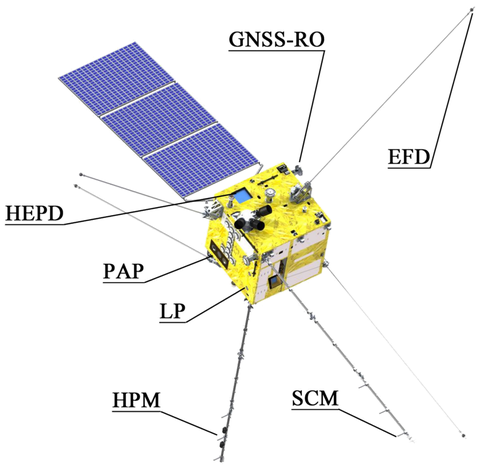
ABSTRACT

The **transfer to satellite-based applications** of the silicon monolithic pixel technology can enable a higher particle detector granularity without increasing the number of bonding interconnections. However, power consumption and heat dissipation are issues to be dealt with for enabling such developments. This contribution will present a **low-power** sparsified **readout architecture** for the **MAPS-based tracker** which will be integrated in the **High-Energy Particle Detector onboard the CSES-02 satellite**. The whole tracker includes 150 ALPIDE sensors organised in three planes and is managed by a custom parallel readout architecture implemented on a single low-power FPGA chip. The adopted solution allows to address both the required performance and the stringent constraints on the power budget. Additionally, this architecture is **scalable** to larger and more complex detectors, thus representing an option for **future space missions**.

HIGH ENERGY PARTICLE DETECTOR

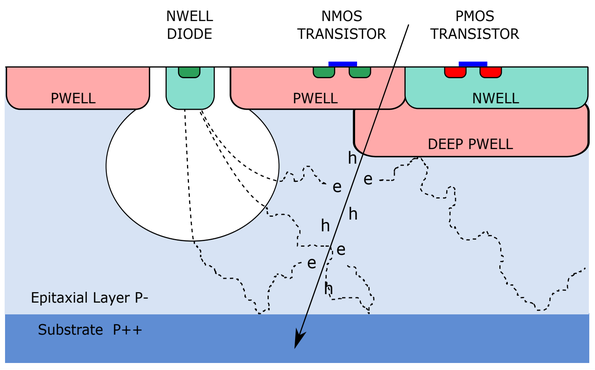
The **High Energy Particle Detector** (**HEPD-02**) is one of the payloads that will equip the **China Seismo Electromagnetic Satellite** (**CSES-02**), and it is aimed at measuring the electromagnetic field and the flux of particles trapped in the Earth's magnetosphere. The detector, through calorimetry and tacking measurements, will reconstruct the energy and direction of **electrons** between **3 and 150 MeV** and **protons** between **30 and 300 MeV**.



The mission goals are to investigate the lithosphere-ionosphere coupling and to study solar physics, space weather and cosmic ray fluxes.

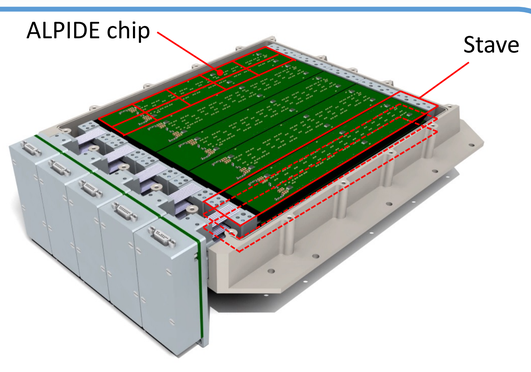
MONOLITHIC ACTIVE PIXEL SENSORS and the ALPIDE

The HEPD-02 includes a **silicon tracker** to reconstruct the particle incidence directions. This tracker is based on silicon **monolithic active pixel sensors** (MAPS), **never used before for a satellite-based experiment**. MAPS enable **higher granularity, low noise, reduced material budget** and much **fewer bonding interconnections** compared to hybrid microstrip sensors. Moreover, they have **lower production costs** than hybrid pixel detectors. The ALPIDE chip, developed by the ALICE collaboration at CERN, was chosen for the HEPD-02 tracker. Each chip is made of 512x1024 pixels with 27 µm x 29 µm pitch. The in-pixel readout circuit, implanted in same substrate as the active area, gives a **binary zero-suppressed output**. The ALPIDE chip has a **sparsified readout**: only the hit pixels output a signal. A fast high-speed LVDS serial readout port, with rate up to 1.2 Gbps, and a **slower readout channel** (3-5 Mbps) from the control port can be alternatively used. The second option was chosen to achieve a **lower power consumption** (18.5 mW cm^{-2}, 71 mW per chip), given the power budget constraints.



THE TRACKER

The **150 ALPIDE** sensors (total **80M pixels**) of the HEPD-02 tracker are organised in **three tracking planes**. The basic tracking and mechanical unit is the **stave**, which includes two columns of 5 ALPIDE chips each (4 **slaves** controlled by 1 **master** via 80 Mbps parallel local buses), glued to a **flex printed circuit** and a **carbon fibre mechanical support**. Three superimposed staves form a **turret**, and five turrets with independent trigger constitute the **tracker**, on top of which two **segmented** layers of crossed plastic scintillator **trigger bars** are placed. The low material budget and the small pixel pitch guarantee high granularity and better angular resolution than the HEPD-01 silicon strip tracker.

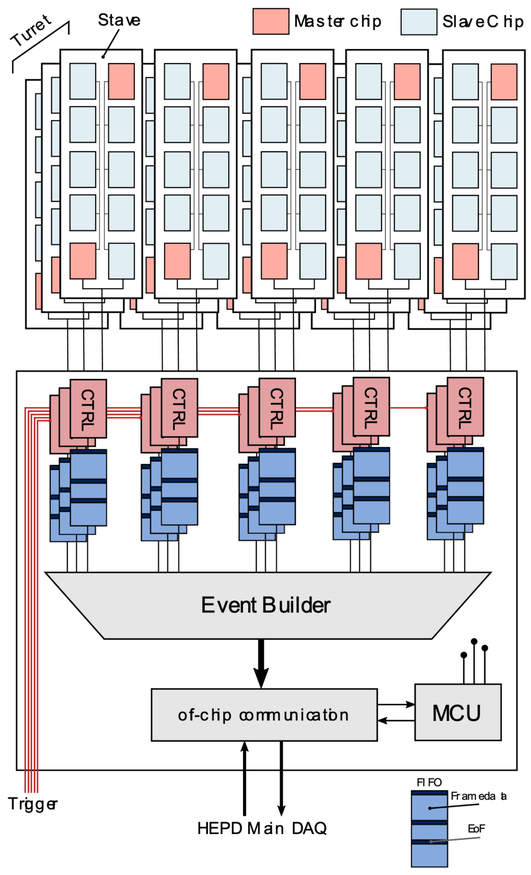


LOW-POWER PARALLEL READOUT

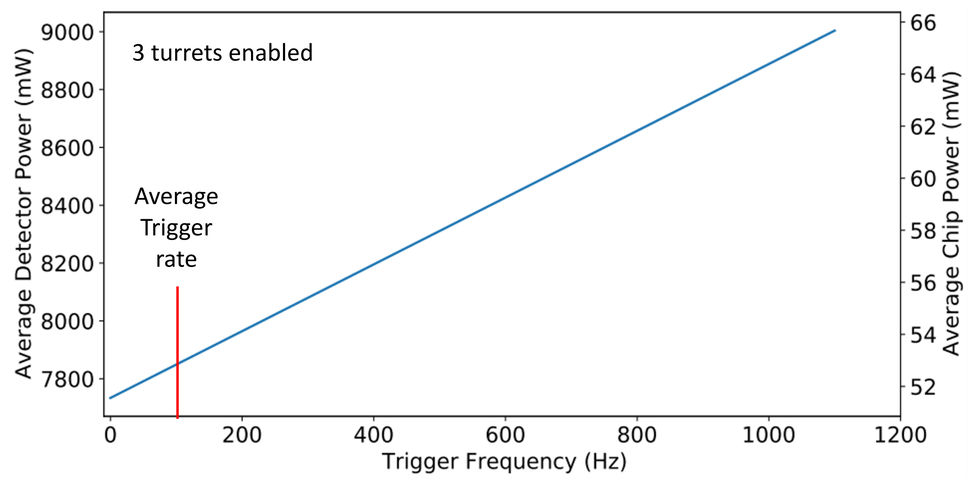
A **low-power parallel sparsified readout architecture** has been implemented to manage the tracker with a **single low-power FPGA** (~1W). The following bus lines are implemented:

- a dedicated differential LVDS **control line** per each stave, plus **clock**
- a **trigger line** per each turret plus busy output
- a spacewire connection to the HEPD main DAQ (100 MHz data rate)

In a single stave, the two masters are connected to the same control bus for clock distribution, triggering and readout. The slow control line readout is acceptable given the **expected average event size** of 100-200 bytes for the entire tracker at **typical trigger rate of 100 Hz** (1 kHz peak). With this trigger rate, the detector is functionally "off" for most of the time. To improve the readout speed, **each stave** is managed **in parallel**.



A further strategy to reduce the power consumption is the **clock gating**. The segmentation of the trigger planes allows to switch on and distribute the clock **only to the turret below the activated trigger sector and to the two adjacent turrets**. Each stave is clocked **only for the time necessary for the event readout**. The event rate is dependent on the local coordinates of the satellite. Hence, the **clock frequency** can be **dynamically scaled** in regions where a lower trigger rate is sufficient and fewer data need to be read out. This reduces the detector power.



CONCLUSIONS

The production of the **engineering models** of stave and turret and the first **calibration, acquisition and tracking tests** have been completed. The mass production for the **qualification and flight models** of the HEPD-02 tracker have started.