Contribution ID: **633** Type: **Poster**

A low-power sparsified readout for the MAPS-based High Energy Particle Detector space tracker

Wednesday, May 26, 2021 5:12 AM (18 minutes)

The transfer to satellite-based applications of the silicon monolithic pixel technology can enable a higher particle detector granularity without increasing the number of bonding interconnections. However, power consumption and heat dissipation are issues to be dealt with for enabling such developments. This contribution will present a low-power sparsified readout architecture for the MAPS-based tracker which will be integrated in the High-Energy Particle Detector onboard the CSES-02 satellite. The whole tracker includes 150 ALPIDE sensors organised in three planes and is managed by a custom parallel readout architecture implemented on a single low-power FPGA chip. The adopted solution allows to address both the required performance and the stringent constraints on the power budget. Additionally, this architecture is scalable to larger and more complex detectors, thus representing an option for future space missions.

TIPP2020 abstract resubmission?

Funding information

Primary authors: BEOLE, Stefania (Universita e INFN Torino (IT)); DE CILLADI, Lorenzo (Universita e INFN Torino (IT)); GEBBIA, Giuseppe (Università di Trento); IUPPA, Roberto (Universita degli Studi di Trento and INFN (IT)); RICCI, Ester (Universita degli Studi di Trento and INFN (IT)); RICCIARINI, Sergio Bruno (Universita e INFN, Firenze (IT)); ZUCCON, Paolo (Universita degli Studi di Trento and INFN (IT))

Presenter: DE CILLADI, Lorenzo (Universita e INFN Torino (IT))

Session Classification: Posters: Particle Astrophysics and Space

Track Classification: Experiments: Experiments: Space and particle astrophysics