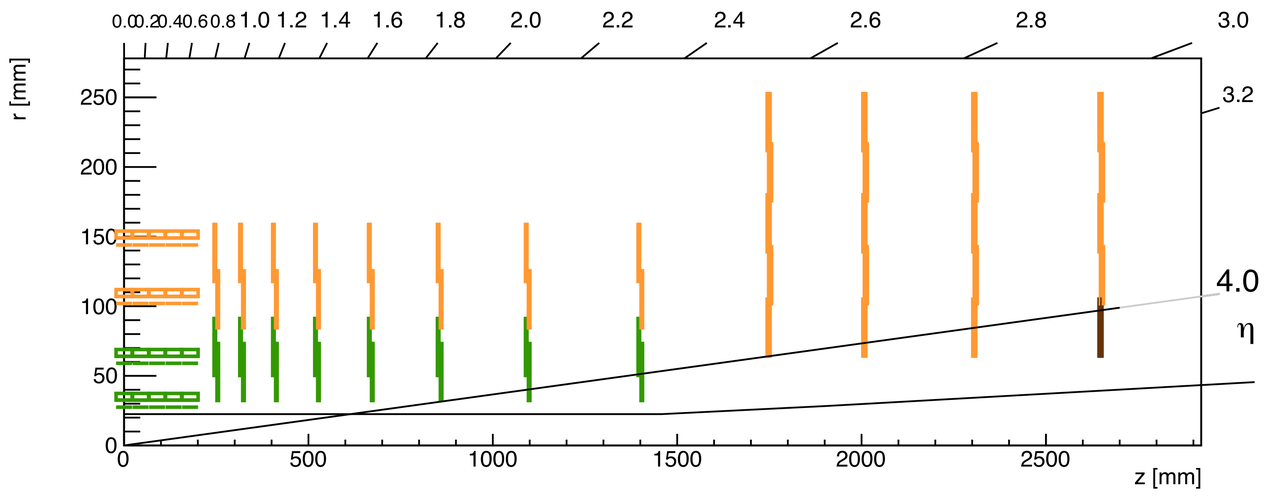
Luminosity and beam-induced background measurement with the CMS tracker endcap pixel detector at HL-LHC

Mykyta Haranko on behalf of the CMS collaboration - **TIPP 2021**

Tracker endcap pixel detector (TEPX)



TEPX:

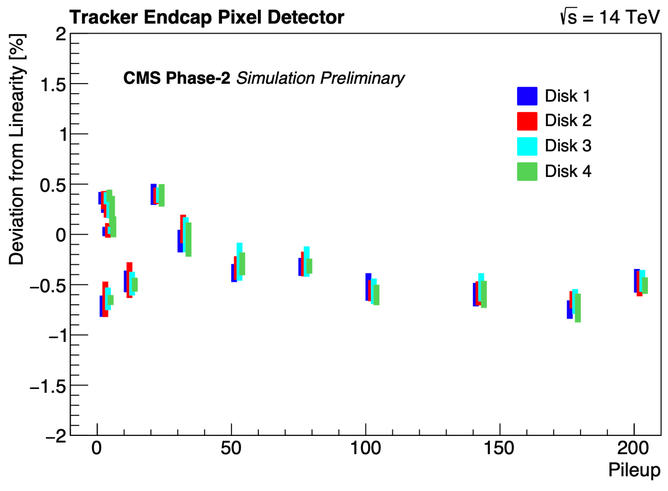
- One z-side consists of 4 double disks 5 rings each
- Is positioned at 175 cm < |z| < 265 cm, 6.3 cm < r < 25.5 cm from the IP
- L1A trigger at 750 kHz is expected (for physics)
- **Additional 75 kHz trigger rate for luminosity**

TEPX D4R1:

- Disk 4 Ring 1 (D4R1) is beyond η = 4 and therefore not useful for tracking
- Gets 17 ns separation between incoming bunch and collision products
- **Full bandwidth (825 kHz or more) for luminosity and beam-induced background measurement**

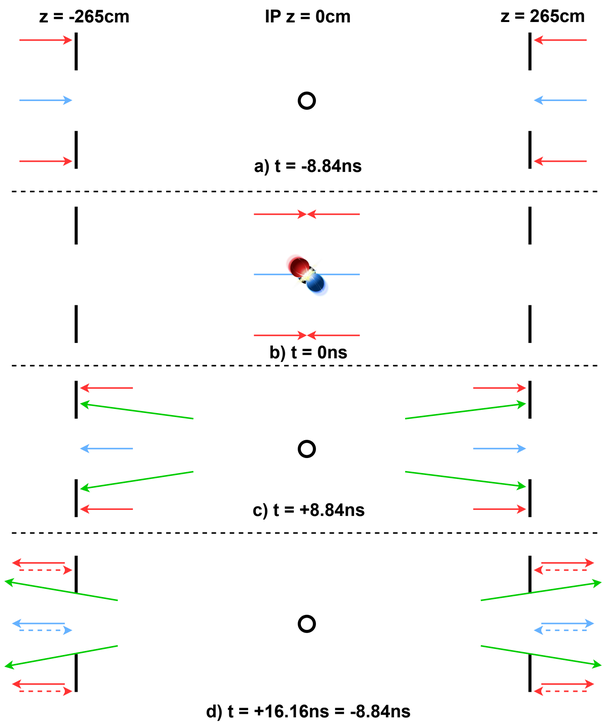
Luminosity perspective

- **TEPX incl. D4R1** : (4 quartes x 5 rings x x 4 disks x 2 ends) - **160 luminosity channels**
- **Sampling rate (TEPX excl. D4R1)**
  - 21 samples per BX per second (physics, 75 kHz)
  - 281 samples per BX per second (VdM, 1 MHz)



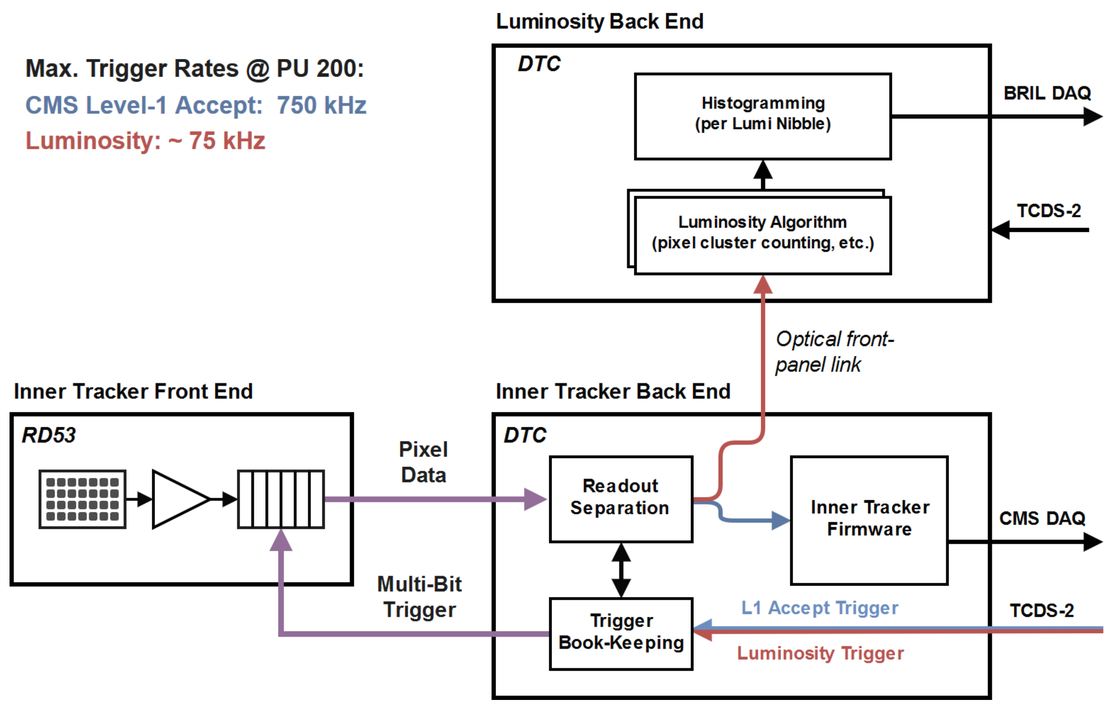
Beam-induced background perspective

- Measure before the first colliding bunch in a train (to exclude collision products and albedo)
- Appropriate time tuning to measure both luminosity and BiB

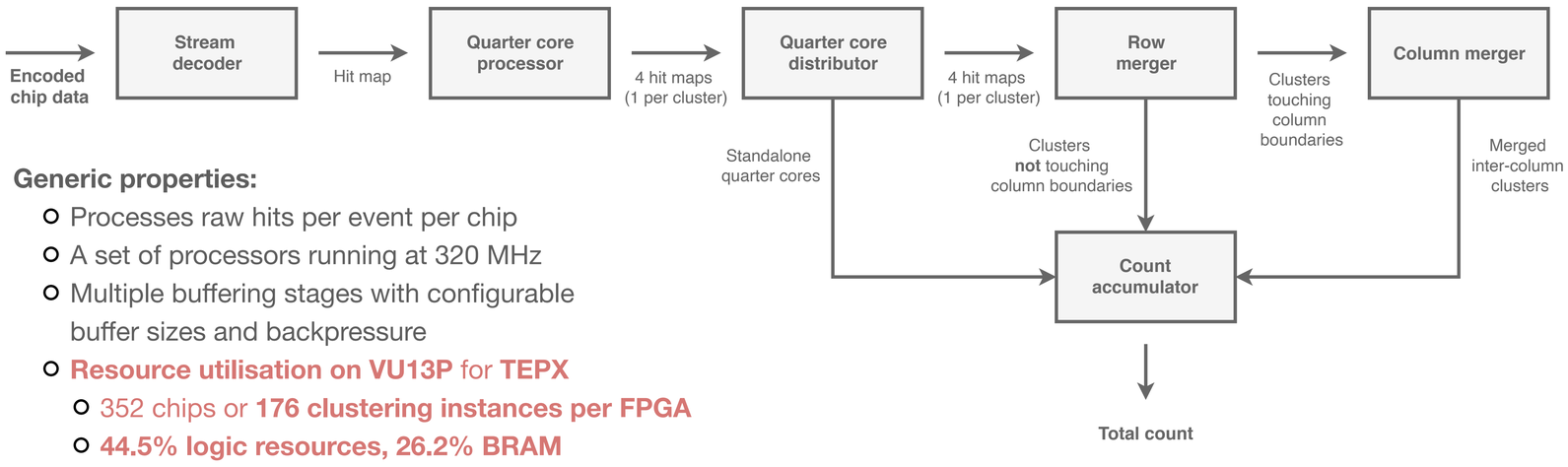


Data flow diagram

- **Apollo ATCA platform** will serve as both the data acquisition card and the luminosity processor
- One luminosity processor will receive data from one DAQ card
- Required bandwidth in range **from 24 Gb/s (TEPX) to 80 Gb/s (TEPX D4R1)**



Real time pixel cluster counting on FPGA - proof of concept



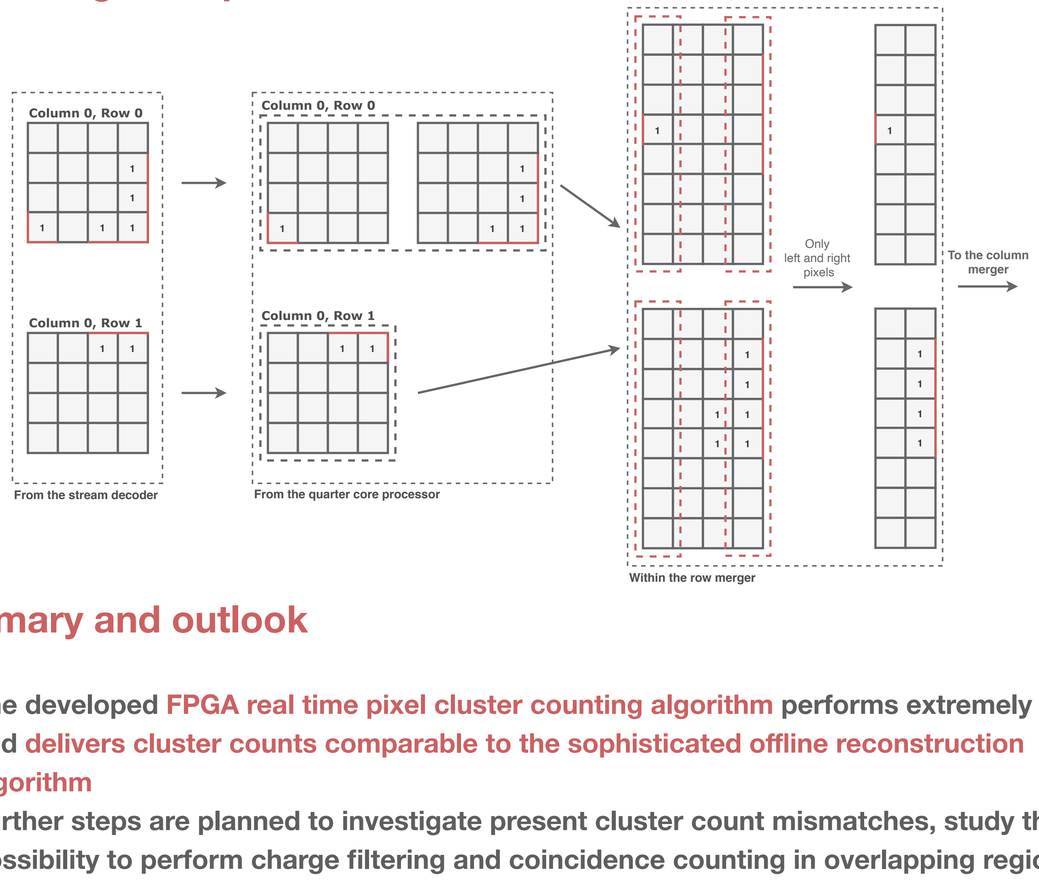
Generic properties:

- Processes raw hits per event per chip
- A set of processors running at 320 MHz
- Multiple buffering stages with configurable buffer sizes and backpressure
- **Resource utilisation on VU13P** for **TEPX**
  - 352 chips or **176 clustering instances per FPGA**
  - **44.5% logic resources, 26.2% BRAM**

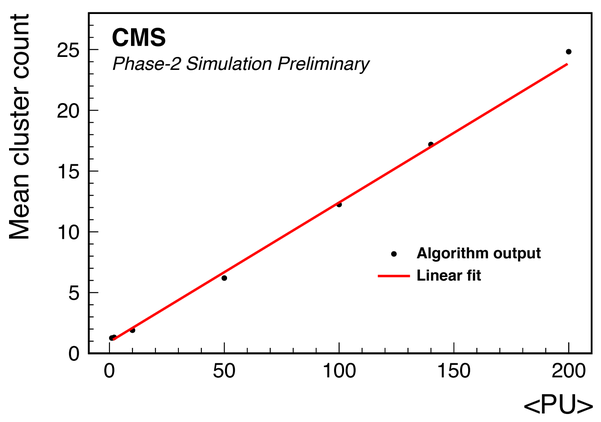
Processor functionality:

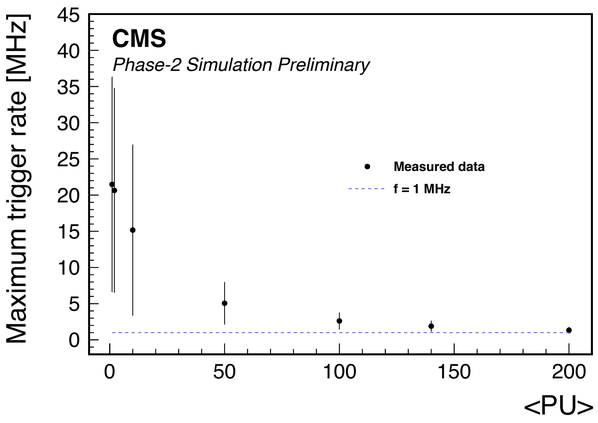
- **Stream decoder** recovers 4x4 hit maps (quarter cores) from the encoded data stream
- **Quarter core processor** splits 4x4 hit maps into clusters, analyses boundaries (touch information)
- **Quarter core distributor** filters isolated quarter cores
- **Row merger** performs vertical cluster merging
- **Column merger** performs horizontal cluster merging
- **Count accumulator** combines counts and performs status monitoring (error and warnings flags)

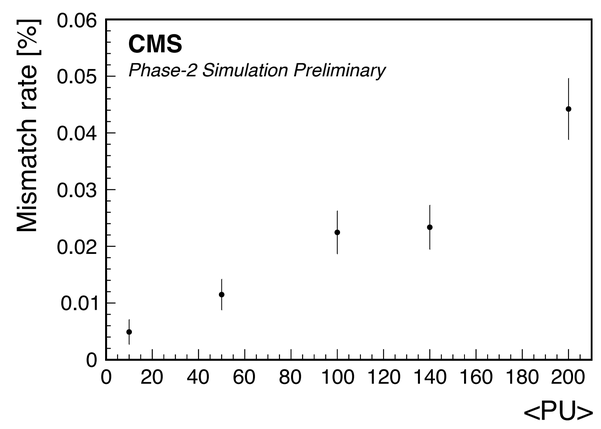
Processing example



Performance







- Performance tested by injecting CMSSW simulated events and comparing to the offline reconstruction algorithm output
- Most of the mismatches are due to charge filtering in the offline algorithm (not available yet on FPGA)
- **Safe margin in processing rate (1.33 MHz at PU200)**

Summary and outlook

- **The developed FPGA real time pixel cluster counting algorithm performs extremely well and delivers cluster counts comparable to the sophisticated offline reconstruction algorithm**
- **Further steps are planned to investigate present cluster count mismatches, study the possibility to perform charge filtering and coincidence counting in overlapping regions**