Abstract

The LHC will be upgraded in several phases that will allow significant expansion of its physics program. The luminosity of the accelerator is expected to exceed 5×10^{34} cm^{-2}s^{-1}. In order to sustain the harsh conditions and to help maintain good trigger efficiency and performance the Resistive Plate Chambers (RPC) system of the CMS experiment will be upgraded. The present RPC system would continue to operate, and it would be upgraded with new Link Boards system. In addition, the coverage of the RPC system will be increased up to pseudo-rapidity of 2.4 by installing a new generation of improved RPCs (iRPCs). Their design and configuration are optimized to sustain higher rates and hence to survive the harsh background condition during HL-LHC operation. The iRPC are equipped with newly developed electronics designed to read-out the detectors from both sides, allowing in this way a good spatial resolution along the strips. The status of the upgrade project is presented.

CMS RPC Upgrade

The CMS RPC upgrade for Phase-2 [1] comprehends (1) the replacement of a the current Link System, which connects the Front-End Boards (FEBs) to the trigger processors, by a new one, redesigned from scratch and (2) the extension of the pseudorapidity coverage of the RPC system by adding new chambers from η = 1.9 up to 2.4. These new chamber will be assembled with a Improved Resistive Plate Chambers (iRPC) technology, which does the readout of signals in both ends of the strip, allowing a 2-dimensional hit reconstruction.

These upgrades would, in the expected high rate of the HL-LHC environment:

- enhance the redundancy of the CMS Muon System;
- resolve ambiguities in the Endcap triggering;
- allow improvements of the RPC system to Trigger and reconstruction.

Figure 1 presents a quadrant of the CMS Muon system for the Phase-2 Upgrade. The locations of new forward muon detectors for the HL-LHC project are indicated in red for Gas Electron Multiplier (GEM) stations (ME0, GE1/1, and GE2/1) and violet for improved RPC stations (RE3/1 and RE4/1).

iRPC FEB

The iRPC chambers will demand changes, in comparison with the current system, in terms of design and electronics [4]. In terms of electronics, a complete new FEB is being developed. This one should (1) ensure the chamber efficiency in a high rate environment (up to 2 kHz/cm²) and (2) provide information for a 2-dimensional readout. To achieve the requirements, the iRPC FEB will use PETIROC ASICs [2], with 32-channels each, for pre-amplification and discrimination of strip signals, providing low-jitter trigger with accurate charge and time measurements.

Each strip end will be connected to one channel of the PETIROC. The digitized signal is sent to a FPGA (Field Programmable Gate Array), where a high resolution Time-to-Digital Converter (TDC) is implemented, allowing 2D measurement of the muon hit by measuring the arrival time difference of the two strip ends.

Figure 2: Muon Efficiency versus High Voltage Effective (HVeff) and Total Current for the second version of FEB with PETIROC2B (FEBv3) and the mean value of multiplicity for each side. ‘AND’ efficiency showing without crosstalk impact. Scintillators placed in the HR of the chamber and covered about 28m. This setup includes three protected with lead scintillators inside GIF++ (ORINo Gamma Irradiation Facility - September-November 2019 - w/o outside scintillators). FEB thresholds: 50 ± 10 MeV.

New Link System

In the CMS experiment, the RPC chambers are readout, controlled and monitored through the Link System, which consists of 1592 electronics boards, divided in two kinds, known as the Link boards (Libs) and Control Boards (Cibs). Libs can work as Master Lib or Slave Lib.

The new link system is being developed around the use of modern components and FPGAs (Field Programmable Gate Array), following a radiation hard design.

The data transmission rate between the new Link system and RPC back-end electronics increases to 10.24 Gbps and resolution of the Muon hit time improves to 1.5 ns.

This is achieved by (1) the use GTX transceivers of the FPGA, pre-processing of data and (2) implementing a high resolution 96-channel TDC in the link board FPGA. Each TDC-channel consists of 36 bins with a time scale of 25/16 ns. Figure 3 shows the emulated channel width, in agreement with the expected 1.56 ns.

Readout and Control Electronics

An extensive Phase-2 upgrade program is also scheduled for CMS Level-1 Trigger [3]. Since RPC is the only Muon detector present in both CMS Barrel and Endcap region, its contribution to CMS Level-1 Trigger upgrade program is important.

The readout and control system (also called back-end) of the RPC (Figure 4) system will be redesigned in order to:

- include readout and control of new hardware;
- cope with the requirements of the CMS Level-1 Trigger Phase-2 design;
- sustain maintainability of the system by replacing obsolete hardware.

The new readout, control and monitoring hardware will be installed in the CMS Services Area, away from CMS radiation, and will follow the CMS specification of common hardware platforms for Phase-2, specifically, Twenty boards [4] with ATCA form factor.

Barrel RPC hits are expected to be distributed to a common CMS Barrel (RPC 4 DT) hardware, while Endcap and iRPC hits will go to dedicated RPC boards. These hits will later be distributed to CMS Muon Task Finders and DAQ.

Conclusion

For the next CMS data-taking period (Run-1 starting in 2022), it is assumed that prototypes of the upgrade activities described above will be installed in CMS to take data concurrently with CMS, for validation propose. In preparation for Phase-2 upgrade, a thorough commissioning of prototypes is expected for the next years. Irradiation tests are also planned.

References


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