New Approach for Achieving High Granularity Low Gain Avalanche Detector

The Deep-Junction Low Gain Avalanche Detector (DJ-LGAD)

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Motivation: Grainsity Limitation on Low Gain Avalanche Detectors (LGADs)

- Conventional Low-Gain-Avalanche-Detectors (LGADs) with spatially segmented readouts uses a surface structure, so called the Junction-termination extension (JTE), to prevent early breakdown due to high electric fields generated by a highly-doped p-type multiplication layer. (as shown in figure)
- The JTE structure introduces “dead region” between readouts, thus limiting the granularity to 1mm scale.
- To make use of LGADs technology in future experiments (i.e., 4D tracking) would require granularity of better than 100um.

- we propose a new approach to resolve this limitation: the Deep-Junction LGADs.

The Deep Junction LGAD (DJ-LGAD) Concept

- The p-n junction formed by highly-doped p+ and n+ gain layers is buried several microns below the surface of the device.
- The high-resistivity n-type isolation layer is used to lower the electric field down from the n+ layer to preserves electrostatic stability for the segmented surface of the device.
- The electric field in the gain layer, or multiplication region, will be large enough to create impact ionization gain.
- Regions outside of the multiplication region will have significantly less electric field, but large enough to saturate the carrier drift velocity.
- Device operates at full depletion, and it’s DC-coupled to a readout electrode.

Demonstrating the DJ-LGAD Idea with TCAD Simulation

- Sentaurus (TCAD) is used to simulate a baseline setup of DJ-LGAD model.
- Electrical properties, such as electric field profile, 1-V curve, and gain-voltage curve were explored in simulation.
- Injection of minimum-ionization particle (mip) is performed to simulate transient signal responses.

1. Deposition of energy track is simulated to represent a mip injection. The dynamic responses (or transient signals) from the readout electrodes are extracted.
2. Signal from the channel for which the mip is injected experiences a non-zero integral response with rise time of order 100ps.

- Simulation of pixel array with 20um pitch.
- Total sum of gain from all channels in terms of transverse position of incidence of a mip.
- Uniformity across channels is within 5%.

Realistic Design for Phase-1 Fabrication

Techniques for achieving deep junction:
- Epitaxial growth (BNL)
  1. Deep junctions created on conventional wafers used for LGADs
  2. A Sum thick p-type HR epitaxial layer has been grown
  3. n+ electrodes (strip and pixels) are then implemented and DC-contacted by aluminum.
- Wafer-Wafer bonding (CACTUS Material)
  1. First using ion implantation to create n+ and p+ gain layers on separate wafers.
  2. The P-N junction development of the gain layers using wafer-to-wafer bonding approach.

Layout of a single diode

1. Enabling of new forms of self-supporting structures.
2. Highly-packed in-situ processing (on focal plane), bringing together hetero-material device interfaces.
3. Fine pitch 3D integration. Phase-1 design has pitch in order of ~10 um.

Conclusion & Plans

- The concept of Deep Junction LGAD (DJ-LGAD) is introduced and simulated with TCAD software.
- Part of designs for the Phase-1 fabrication was shown.
- Prototype of the Phase-1 design were produced by BNL & Cactus Material. Samples are ready for laboratory testing and measurements.
- Design refinement and parameter optimization with TCAD simulation. Working toward Phase-2 fabrication.

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