New Approach for Achieving High Granularity Low Gain Avalanche Detector
The Deep-Junction Low Gain Avalanche Detector (DJ-LGAD)

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Motivation: Granularity Limitation on Low Gain Avalanche Detectors (LGADs)

- Conventional Low-Gain-Avalanche-Detectors (LGADs) with spatially segmented readouts uses a surface structure, so called the Junction-termination extension (JTE), to prevent early breakdown due to high electric fields generated by a highly-doped p-type multiplication layer. (as shown in figure)
- The JTE structure introduces "dead region" between readouts, thus limiting the granularity to 1mm scale.
- To make use of LGADs technology in future experiments (i.e., 4D tracking) would requires granularity of better than 100um.
- we propose a new approach to resolve this limitation : the Deep-Junction LGADs.

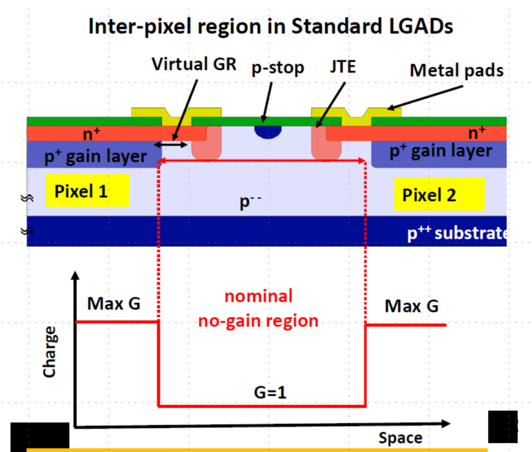
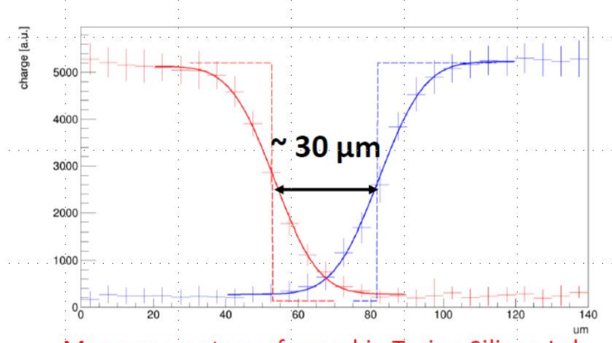


Diagram credit: FBK, Trento, Italy

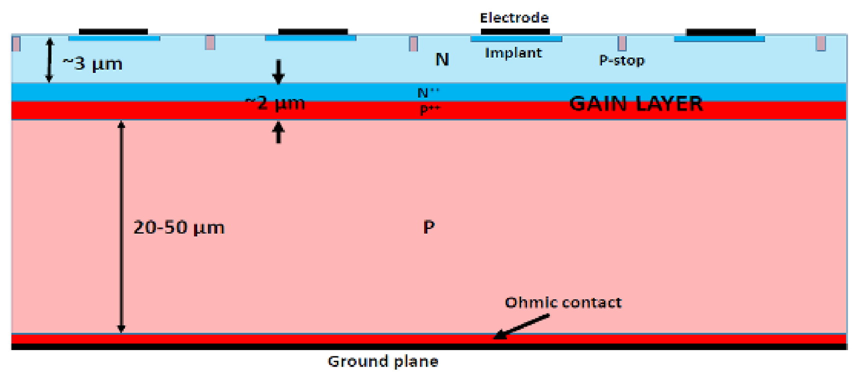
Measurement (laser scan)



Measurements performed in Torino Silicon Lab (University of Torino - INFN)

The Deep Junction LGAD (DJ-LGAD) Concept

- The p-n junction formed by highly-doped p+ and n+ gain layers is buried several microns below the surface of the device.
- The high-resistivity n-type isolation layer is used to lower the electric field down from the n+ layer to preserves electrostatic stability for the segmented surface of the detector.
- The electric field in the gain layer, or multiplication region, will be large enough to create impact ionization gain.
- Regions outside of the multiplication region will have significantly less electric field, but large enough to saturate the carrier drift velocity
- Device operates at full depletion, and it's DC-coupled to a readout electrode.

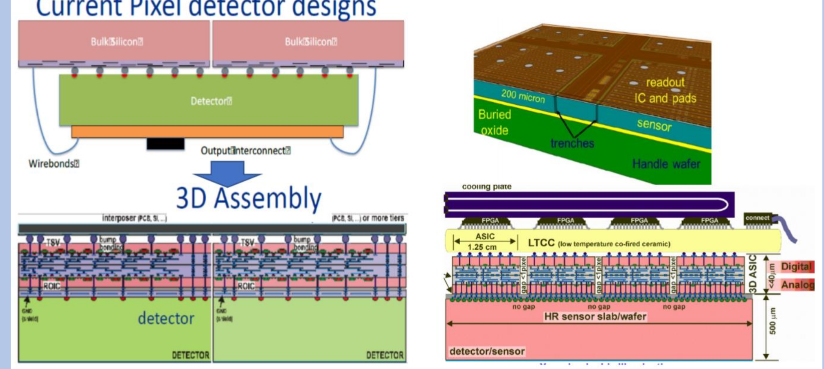


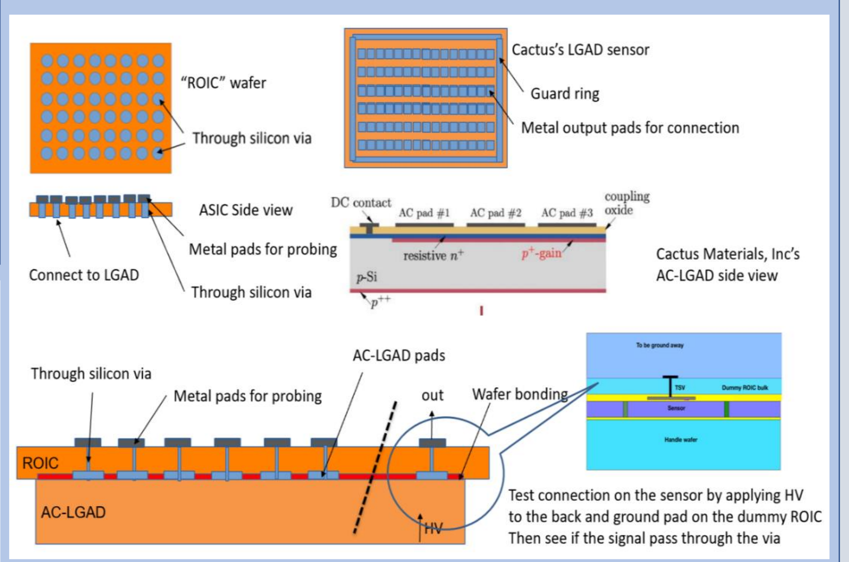
Element	Doping Level (N/cm^3)	Extent In Depth
N isolation layer (N bulk)	constant doping of 3×10^{12}	From 0 µm to beginning of N+ "gain plate" layer
N+ gain plate (upper half of gain layer)	Gaussian, peak doping 3×10^{16}	peak at 4 µm, Gaussian width of 0.17 µm
P+ gain plate(lower half of gain layer)	Gaussian, peak doping 3×10^{16}	Peak at 5.5 µm, Gaussian width of 0.17 µm
P drift region (P bulk)	constant doping of 3×10^{12}	End of P+ "gain plate" layer to 50 µm
P stop	constant doping of 1×10^{13}	1 µm deep at surface, 1 µm wide
N++ implant (under electrode)	constant doping 1×10^{19}	at surface
Gain layer doping tolerance (N+ and P+ varied together)	effective operation peak doping between 2.9×10^{16} and 3.5×10^{16}	

High Density Interconnect ("3D Integration")

1. Enabling of new forms of self-supporting structures.
2. Highly-packed in-situ processing (on focal plane), bringing together hetero-material device interfaces.
3. Fine pitch 3D integration. Phase-1 design has pitch in order of ~10 um.

Current Pixel detector designs

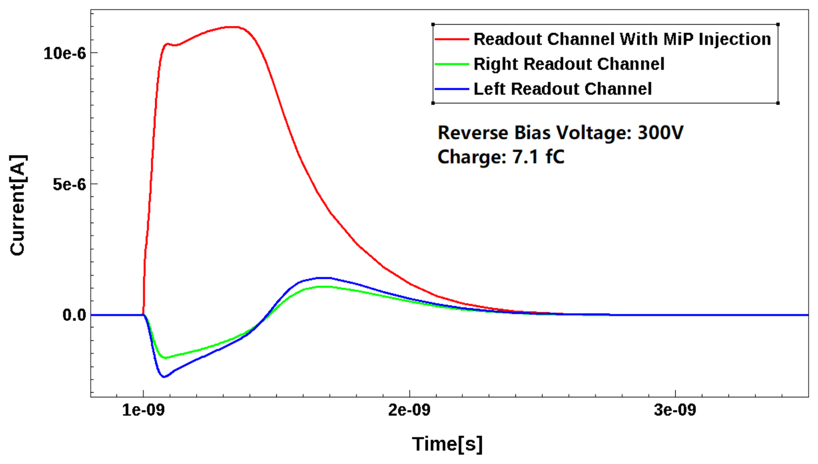




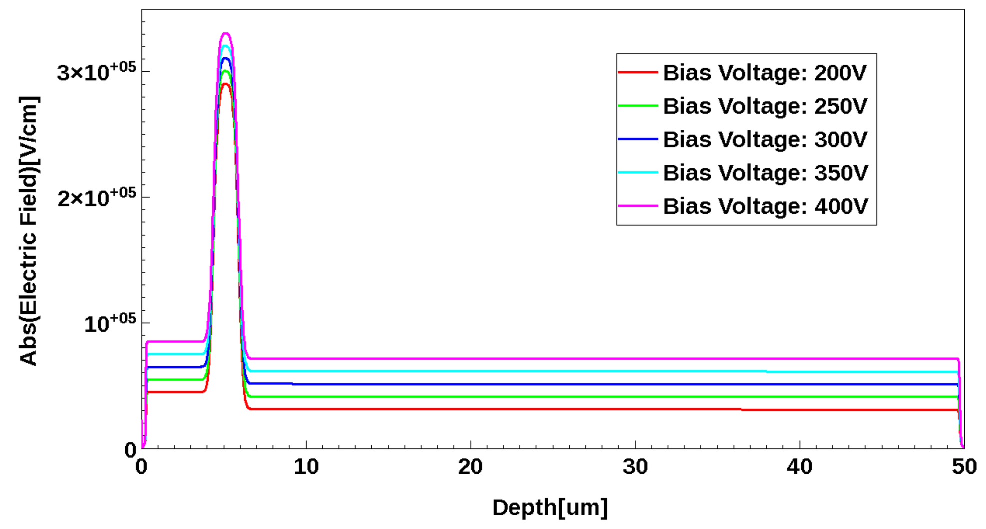
Demonstrating the DJ-LGAD Idea with TCAD Simulation

- Sentaurus (TCAD) is used to simulate a baseline setup of DJ-LGAD model.
- Electrical properties, such as electric field profile, I-V curve, and gain-voltage curve were explored in simulation.
- Injection of minimum-ionization particle (mip) is performed to simulate transient signal responses.

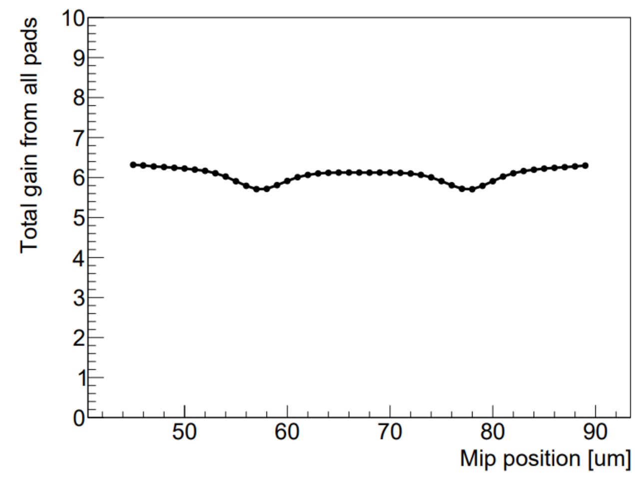
1. Deposition of energy track is simulated to represent a mip injection. The dynamic responses (or transient signals) from the readout electrodes are extracted.
2. Signal from the channel for which the mip is injected experiences a non-zero integral response with rise time of order 100ps.



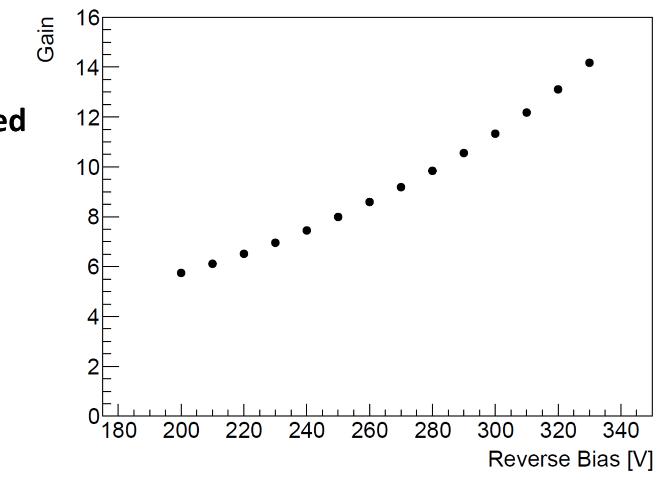
1. Electric field strengths along the surface to the back of the device at the center of a channel are shown for various bias voltages.
2. The peak region is generated by the highly-doped n+ and p+ gain layers, and the regions with relatively lower field comes from the n-type diffusion region and p-bulk.
3. The simulation shows that field within the peak region is high enough to trigger an impact ionization process.
4. The diffusion region maintains a relatively lower field but large enough to reach carries drift velocity saturation.



- Simulation of pixel array with 20um pitch.
- Total sum of gain from all channels in terms of transverse position of incidence of a mip.
- Uniformity across channels is within 5%.



- Gain as function of reversed bias voltage.
- Gain > 10 is achievable for bias voltage ~280V.



Realistic Design for Phase-1 Fabrication

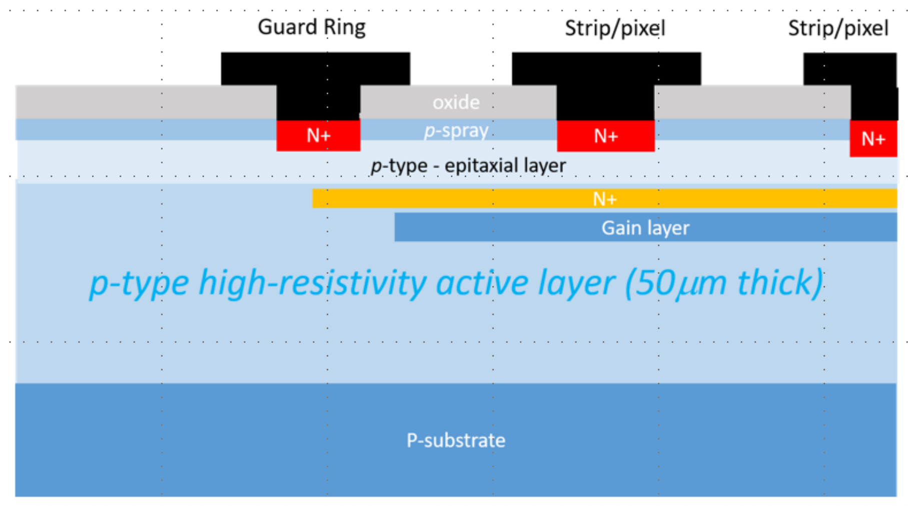
Techniques for achieving deep Junction:

Epitaxial growth (BNL)

1. Deep junction created on conventional wafers used for LGADs
2. A 5um thick p-type HR epitaxial layer has been grown
3. n+ electrodes (strip and pixels) are then implemented and DC-contacted by aluminum.

Wafer-Wafer bonding (Cactus Material)

1. First using ion implantation to create n+ and p+ gain layers on separate wafers.
2. The P-N junction development of the gain layers using wafer-to-wafer bonding approach.

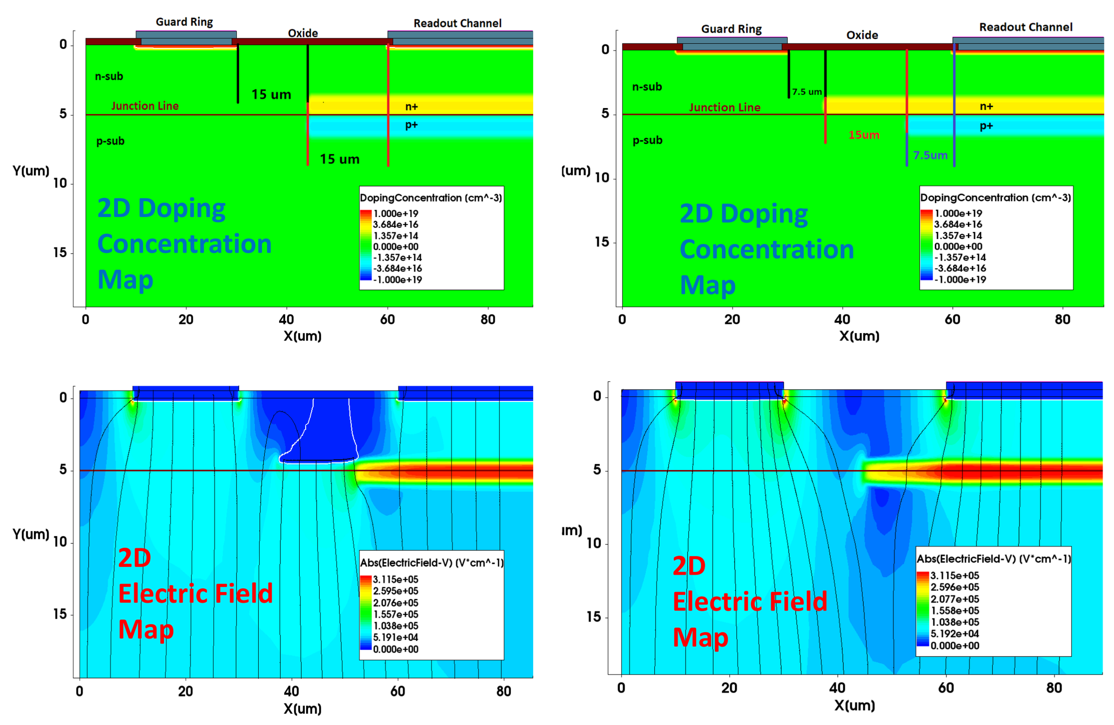


Edge Termination Strategies

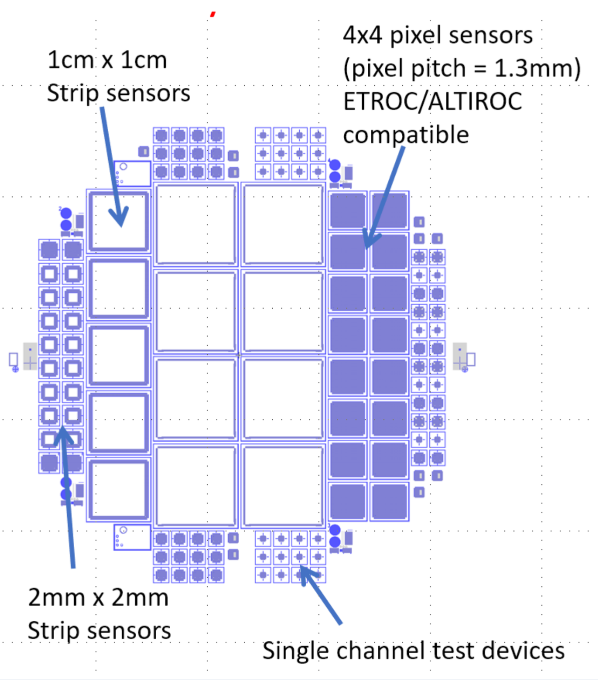
The gain layer needs to be terminated from the physical edge of the device. Two edge termination strategies are proposed:

Symmetric: the lateral extended range is the same for both n+ and p+ layers.

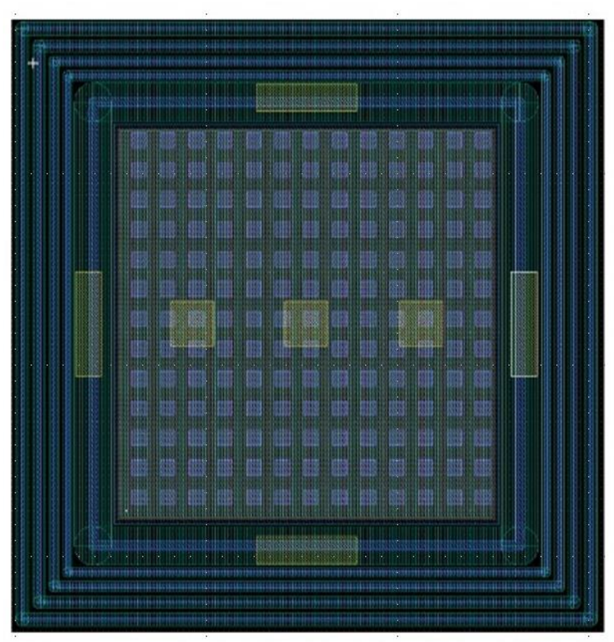
Antisymmetric: the n+ extends longer than the p+ layer.



Wafer Mask Design/Layout



Layout of a single diode



Conclusion & Plans

- The concept of Deep Junction LGAD (DJ-LGAD) is introduced and simulated with TCAD software.
- Part of designs for the Phase-1 fabrication was shown.

- Prototype of the Phase-1 design were produced by BNL & Cactus Material. Samples are ready for laboratory testing and measurements.
- Design refinement and parameter optimization with TCAD simulation. Working toward Phase-2 fabrication.

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