RD53B Wafer Testing for the ATLAS ITk Pixel Detector
Mark Standke on behalf of the ATLAS ITk Collaboration

**LHC & ATLAS**

ATLAS (A Toroidal LHC ApparatuS) is one of two general purpose particle detectors at the Large Hadron Collider (LHC). With the High Luminosity (HL-LHC) upgrade, the objective is to increase the LHC’s luminosity by a factor of 10 beyond its original design value.

For this purpose ATLAS (ITk) will have to be upgraded to cope with the increased radiation, speed and vertex resolution.

**ITKPIX—WAFER PROBING SETUP**

**ITKPIX WAFER**

ITkPix is manufactured in 65nm CMOS TSMC technology. Despite the age of the technology, production of complex chips still involves statistical production uncertainties. Therefore each chip needs to be tested after manufacturing before being assembled as modules. The chips get delivered in wafers of 134 chips.

**ITKPIX NEEDLE CARD**

To enable scalable testing each chip is connected to the testing system via a needle card, which in contrast to wire bonding, is a non-permanent connection and allows the probe station to hop from chip to chip.

**PROBE STATION**

The probe station is responsible for the microscopic alignment of the needle card to the chip pads on the wafer.

It features a microscope, a micrometer motor stage and dust cover to contact and hop from chip to chip.

**BDAQ53 TEST SYSTEM**

The heart of the ITkPix wafer probing system is the bdaq53 test system developed in Bonn. It consists of driver Software for power supplies, SMUs, the probe station and needle card. In addition to that it features a custom designed FPGA board for ITkPix Data acquisition.

**PIXEL MATRIX**

The Pixel Matrix of a single ITkPix consists of 400 x 384 pixels with a pixel size of 50 x 50 μm. This makes up 96% of the chips surface area. Each Pixel consists of an analog front end surrounded by digital pixel logic.

**CHIP BOTTOM**

The Digital Chip Bottom is responsible for communication, analog to digital and digital to analog conversion of chip internal signals, debug muxes and temperature and radiation sensors, as well as supply voltage regulators.

**ANALOG PIXEL FRONT END**

The charge received by each pixel is in the order of hundreds to thousands of electrons. Each signal has to be amplified, its charge amount has to be measured and prepared for digitalization after application of a detection threshold.

**DIGITAL COMMUNICATION**

Digital communication is established via a single differential 160 Mbit Rx line for command receipt and data is sent by up to four differential 1.28Gbit Tx Lines.

**ANALOG CHIP BOTTOM**

The chip bottom also houses a mux to check many internal chip potentials and currents, as well as supply voltage/current generators for other chip modules and supply voltage regulators for serial powering.

**ACKNOWLEDGEMENTS**

ATLAS INNER TRACKER (ITK)

The ATLAS Inner tracker (ITk) will consist of five layers of Hybrid Pixel Detector modules. Each module consists of a charge collecting Sensor chip, collecting the deposited charge of traversing ionizing particles and guides this charge via a bump bond to the Hybrid Pixel Readout Chip.

**ITKCHARACTERISTICS**

- Five layers of Pixel Modules
  - Active area 12.7 m²
  - Pixel size: 50x50 (and 25x100) μm²
  - ~10000 Hybrid modules
  - ~33000 electronic readout chips
- Four Layers of Silicon Strip Detectors

**RD53B/ITKPIX—HYBRID PIXEL READOUTCHIP**

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**DIGITAL PIXEL LOGIC**

Each analog pixel signal needs to be digitized and stored for up to 500 LHC bunch crossings.

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