

# Passive CMOS Strip Sensors with Multiple Stitching

Technology and Instrumentation in Particle Physics conference TIPP 2021

Marta Baselga<sup>1</sup>, Leena Diehl<sup>2</sup>, Ingrid-Maria Gregor<sup>1</sup>, Marc Hauser<sup>2</sup>, Tomasz Hemperek<sup>3</sup>, Jan-Cedric Hönig<sup>2</sup>, Sven Mädgefessel<sup>2</sup>, Ulrich Parzefall<sup>2</sup>, **Arturo Rodriguez<sup>2\*</sup>**, Surabhi Sharma<sup>1</sup>, Dennis Sperlich<sup>2</sup>, Tianyang Wang<sup>2</sup>, Liv Wiik-Fuchs<sup>2</sup>

1) Deutsches Elektronen-Synchrotron DESY, Notkestraße 85, 22607 Hamburg

2) Physics Institute University of Freiburg, Hermann-Herder-Straße 3a, 79104 Freiburg im Breisgau

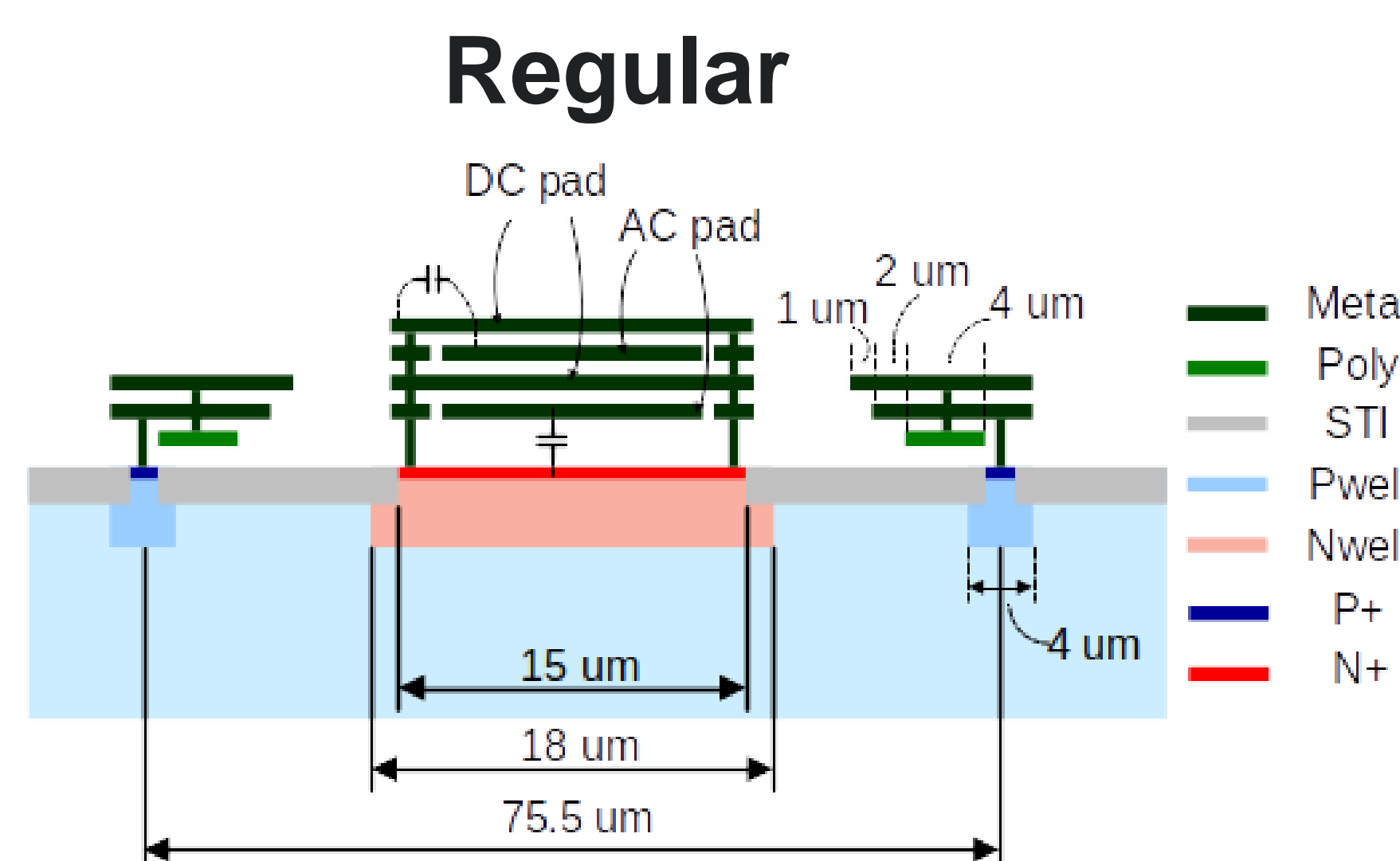
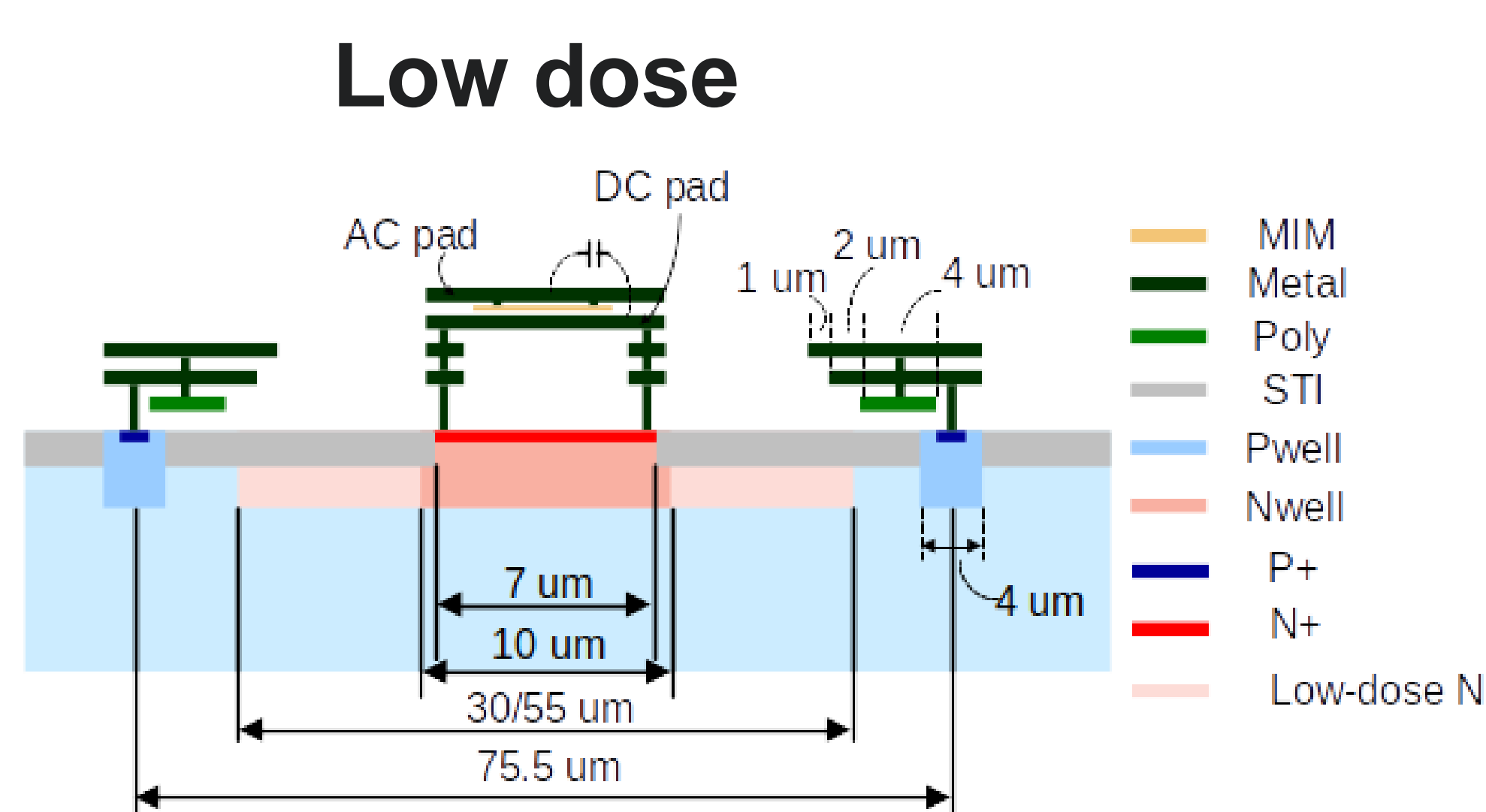
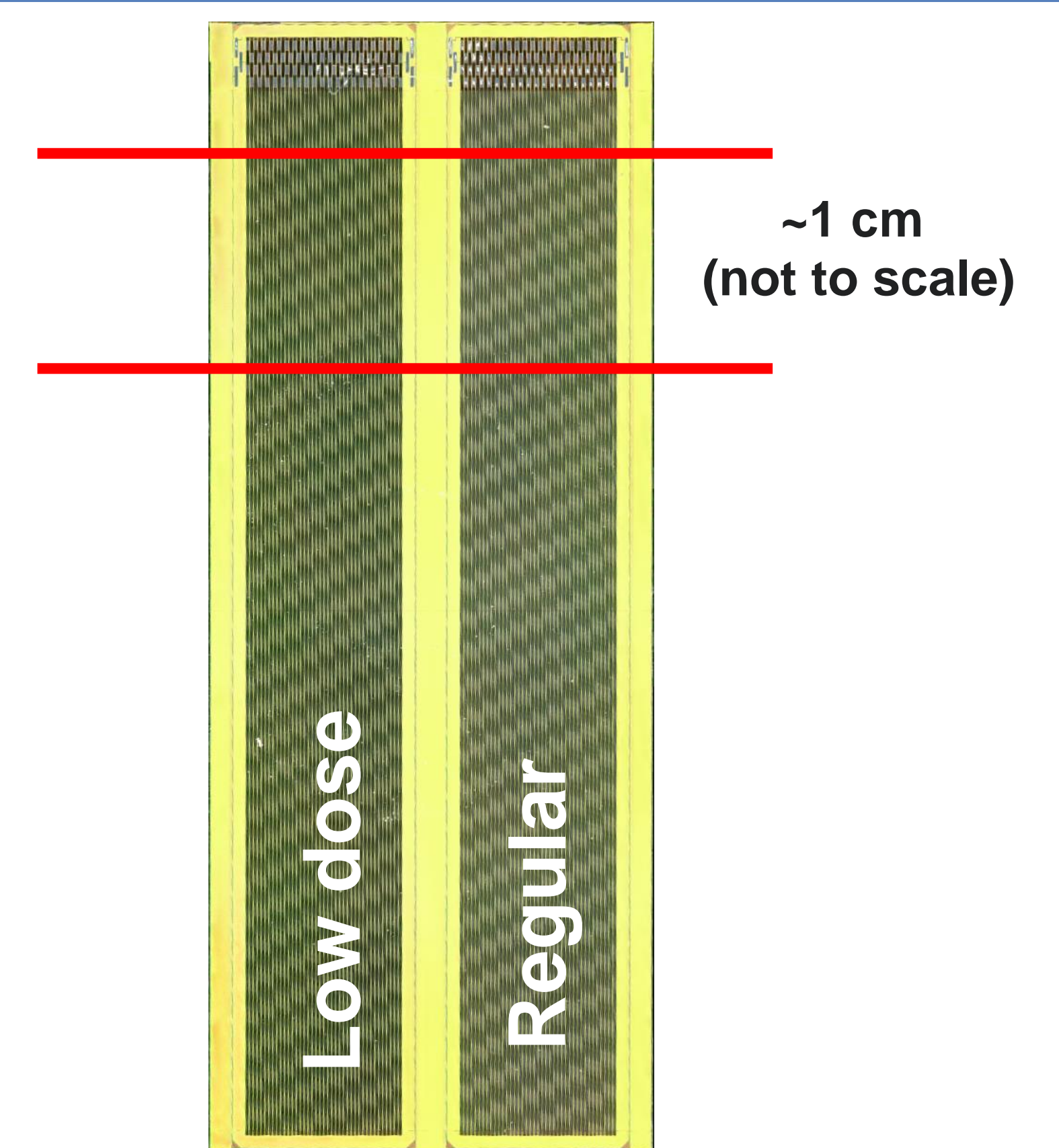
3) Physics Institute University of Bonn, Nußallee 12, 53115 Bonn

**Abstract:** Two current issues with Silicon particle sensors are the high cost, making them a cost driver, and the limited availability from only a few manufacturers. Most CMOS foundries are equipped for producing small chips only. To obtain larger sensors as required in strip trackers, reticles have to be connected by stitching. In our study, passive strip sensors were developed in p-CMOS 150 nm technology on a 150  $\mu\text{m}$  thick wafer and produced by a European manufacturer. Stitching of up to 5 different reticles was used. Sensors were characterized on probe stations and then tested in the lab with Sr-90 sources and IR-lasers. We will present position-resolved signal measurements to evaluate the sensor performance. Results from 2 batches of sensors are shown in this study, with an improved backside processing on the 2nd batch of sensors to enhance the HV performance of the initial batch. We are able demonstrate that the sensors perform well, and stitching does not show negative effects

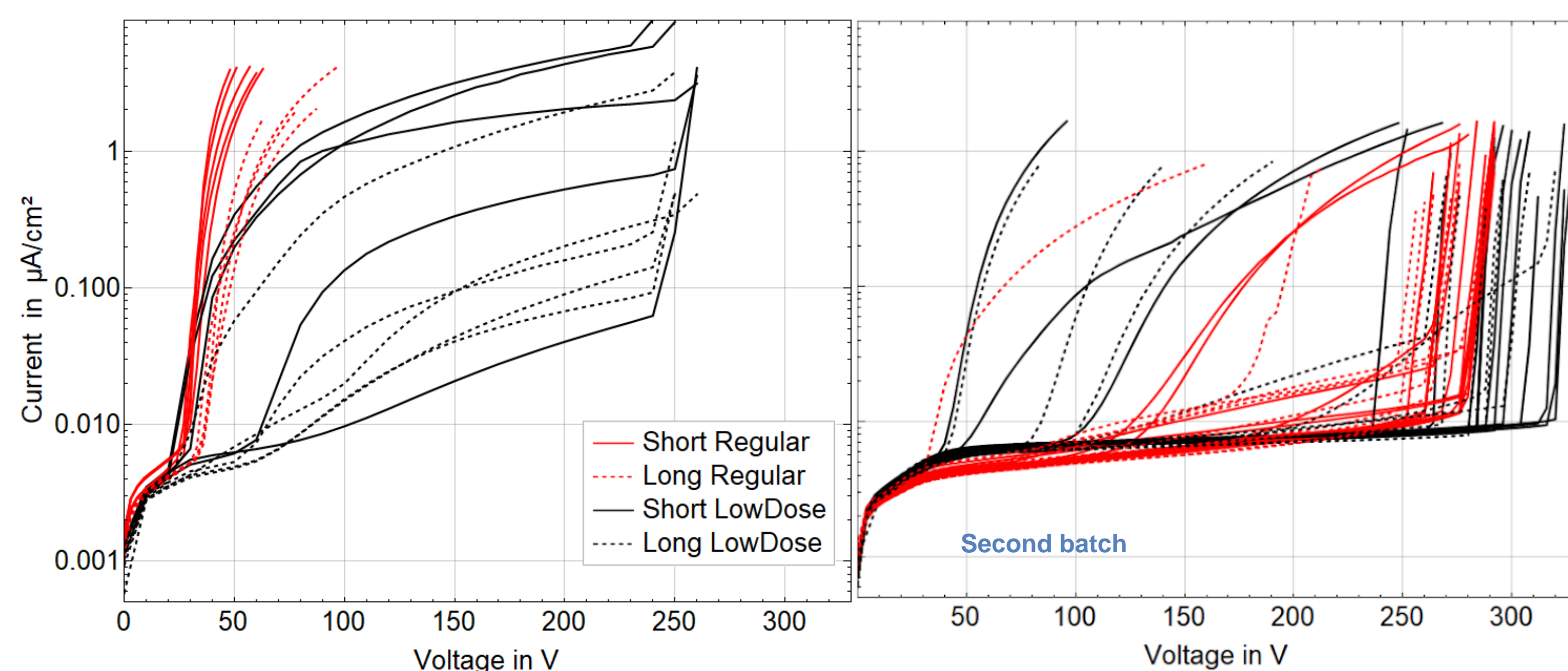
## Sensor Design

- First stitched strip sensors produced on 8" wafer by a commercial high-volume foundry.
- L-Foundry 150 nm process (deep N-well/P-well)
- Up to 7 metal layers
- Wafer Resistivity: > 2 k $\Omega\cdot\text{cm}$
- Float-Zone silicon

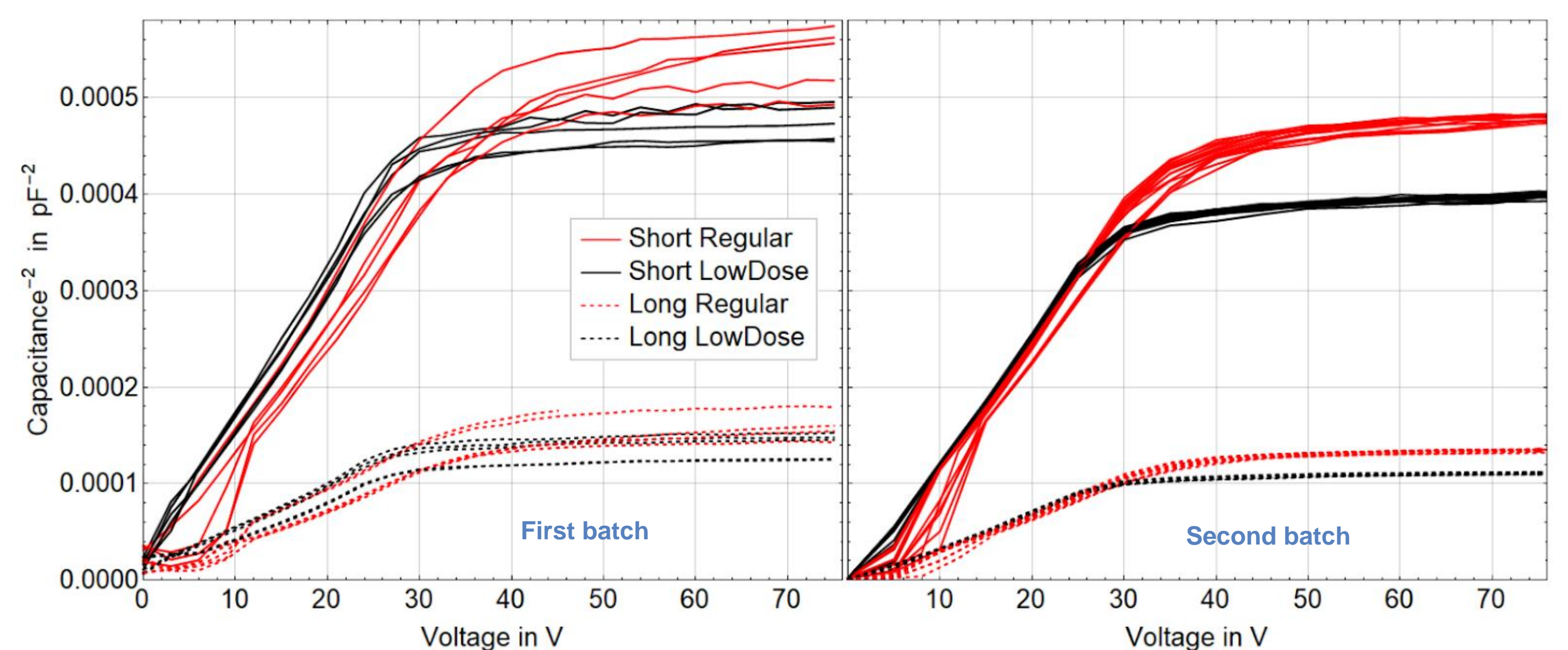
- Frontside process: Reticle stitching  $\Rightarrow$  larger sensors
- Two sensor lengths (2 and 4 cm)
- Three types of implants per sensor
- 40 strips for each design



## IV and CV Measurements

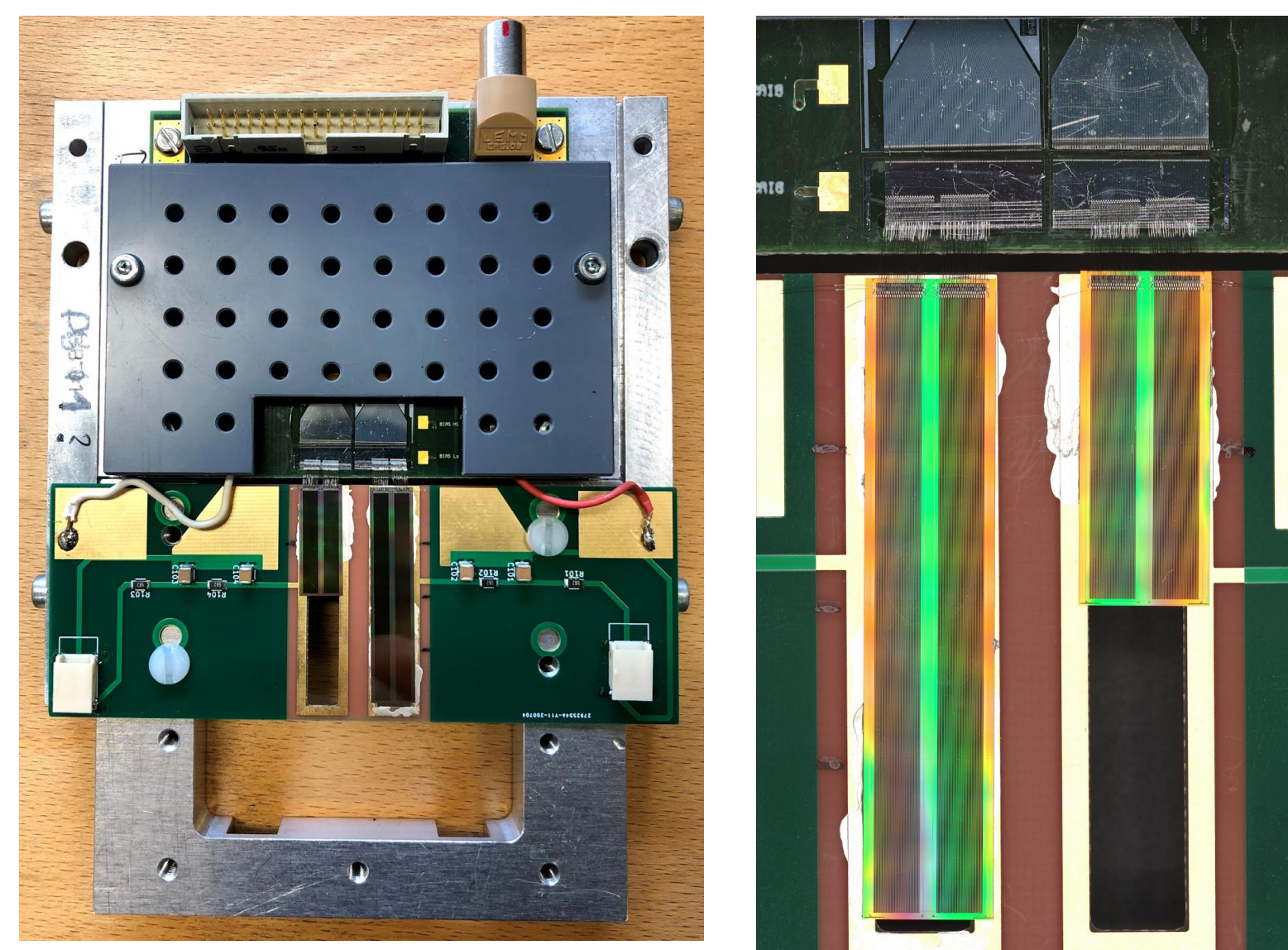
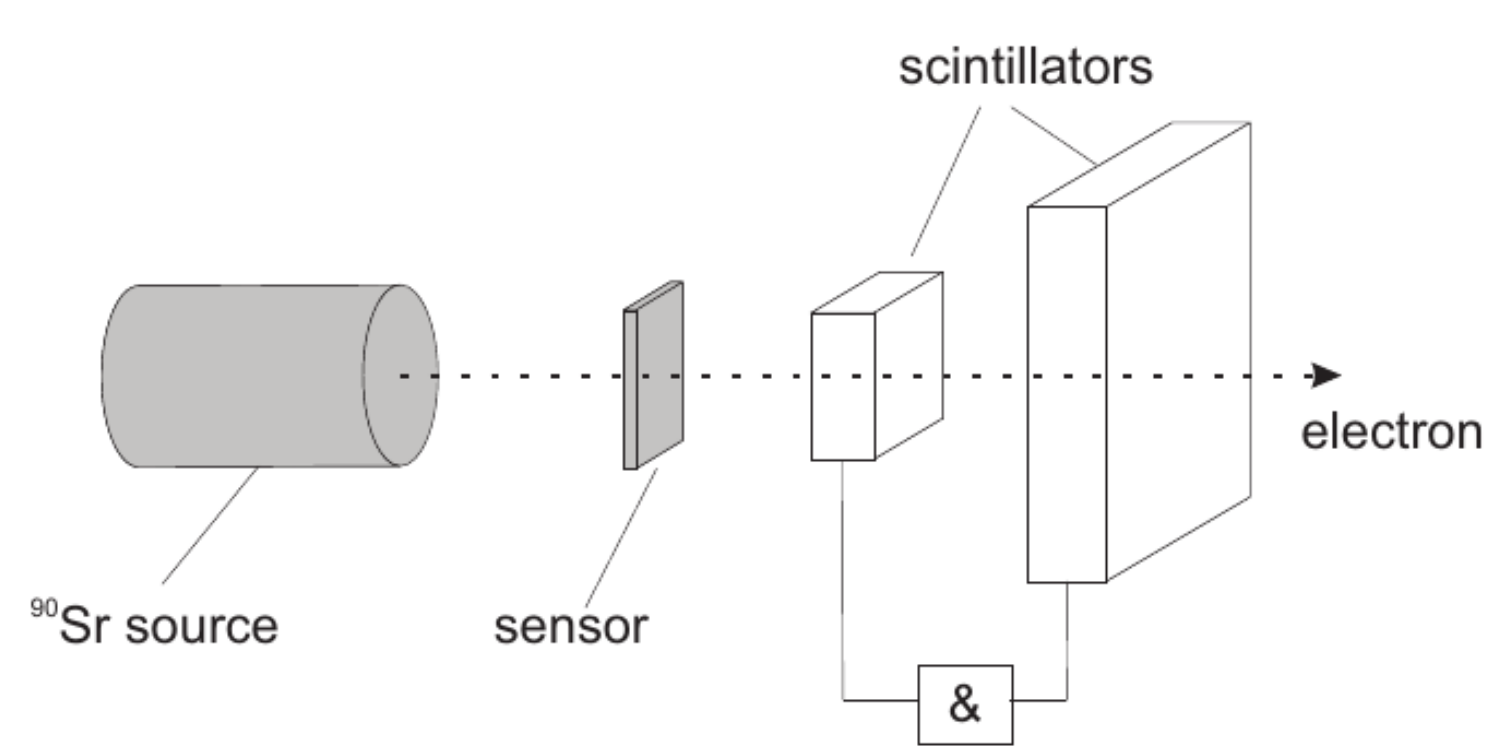


- First batch: low concentration backside implant and not metallization  
Second batch: higher concentration backside implant and metallization
- Breakdown above 220 V
  - Low dose design more stable along the range of voltages

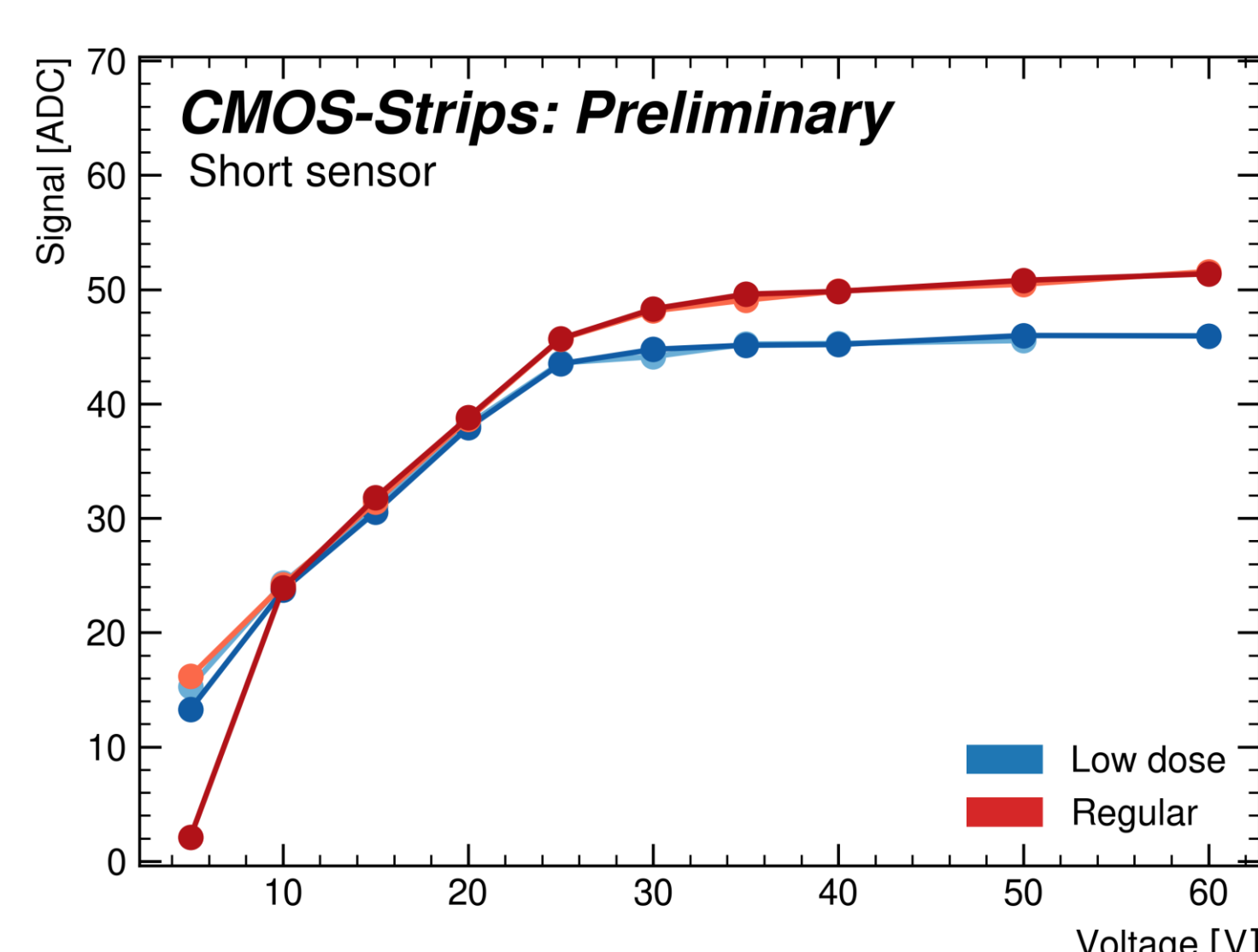
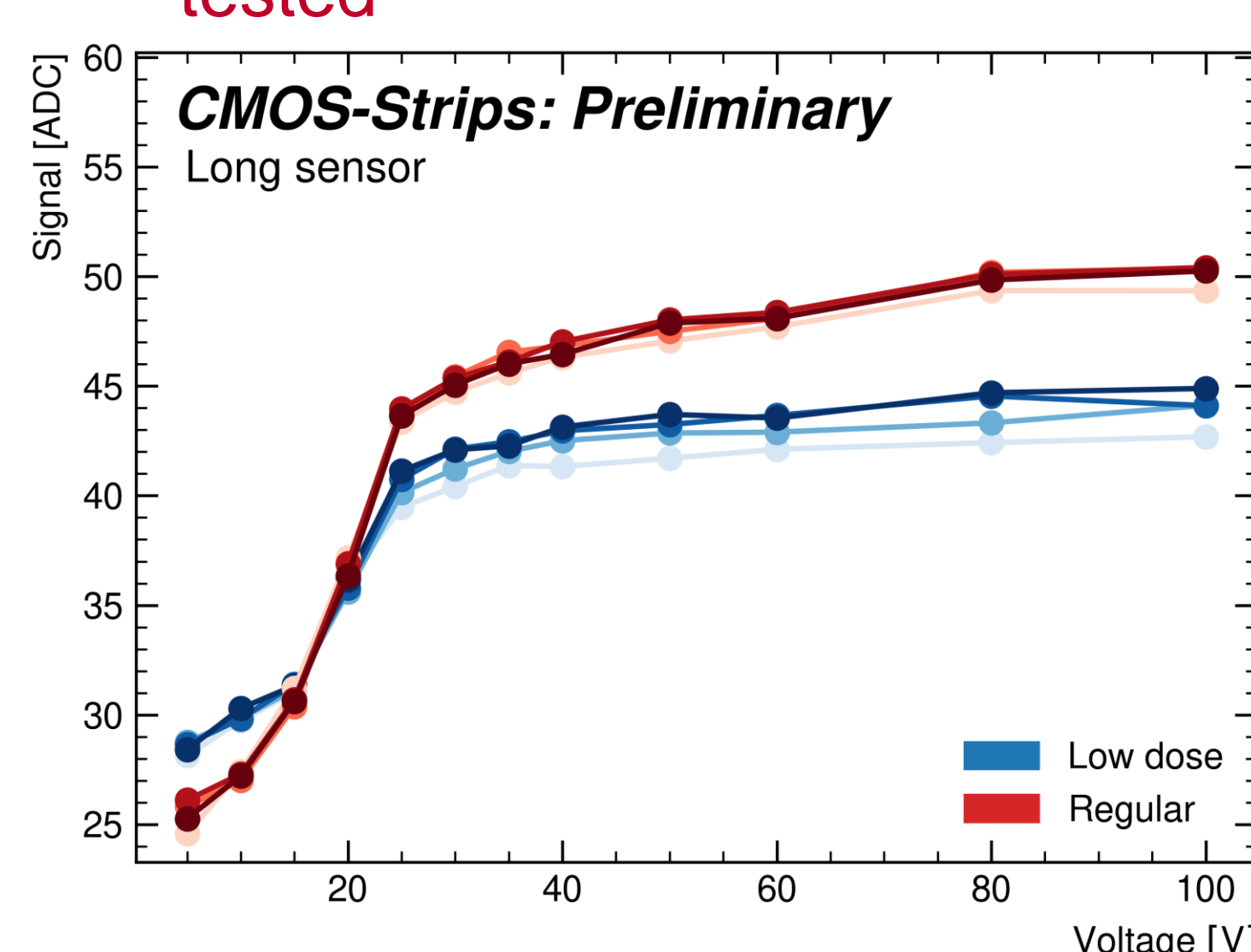


- Full depletion voltage around 25-40 V for both designs
- Strong strip impact on capacitance for regular design at low voltages up to 10 V
- No negative effect from stitching visible

## Beta Source Charge Collection Measurement



- Move source to scan each stitched area
- Only sensors from first batch tested



No negative effect from stitching visible

## Summary and Outlook

- Successful design, production and measurements of first passive CMOS strip sensors
- Low dose sensor design is better suited to withstand high voltages
- Breakdown voltage for good sensors is larger than 250 V

### Stitching works

No negative effect from the stitching could be observed in the measurements conducted

- Charge collection measurements for the second batch are currently being performed
- Irradiation studies are ongoing
- Sensors were measured at the DESY test beam facility and analysis is ongoing

