ARCADIA: sensor development and chip design for low-power, large area FD-MAPS

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ARCADIA project overview

ARCADIA (INFN CSNV Call Project)
Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

Ongoing activity towards a CMOS sensor design and fabrication platform allowing for:

- **Active sensor thickness** in the range **50 µm to 500 µm** or more;
- Operation in **full depletion with fast charge collection** only by drift, small charge collecting electrode for optimal signal-to-noise ratio;
- Scalable readout architecture with **ultra-low power** capability (O(10 mW/cm2));
- Compatibility with **standard CMOS** fabrication processes: concept study with small-scale test structure (SEED), technology demonstration with large area sensors (ARCADIA)

Target **applications**:

- Medical scanners (proton CT)
- Future lepton colliders
- Space experiments
- Possibly x-ray applications with thick substrates

Monolithic Sensor Technology

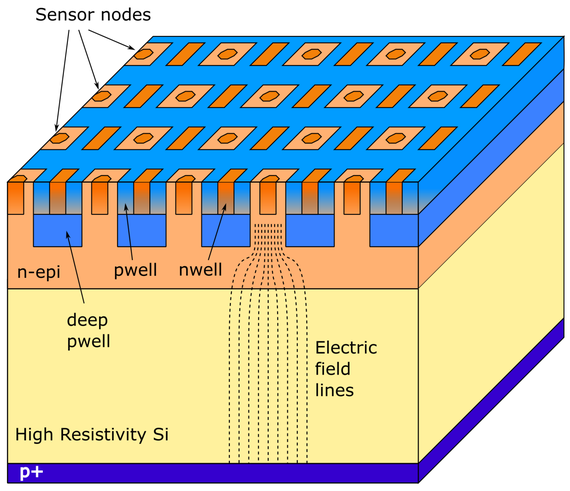


Figure 1. Monolithic pixel sensor schematic view

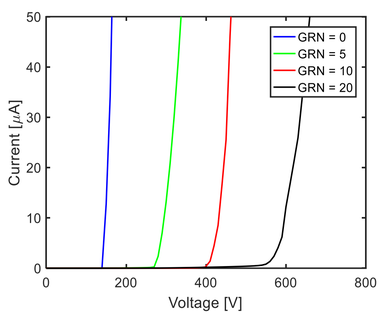
- Modified 110nm CMOS process
- 1.2V thin-oxide transistors for high radiation resistance
- In-pixel CMOS electronics: transistor nwells shielded by deep pwell implantations
- Fully-depleted **n-type High Resistivity substrate**
- Low-resistivity epi-layer for delayed onset of punch-through current
- Backside processing: p+ implantation, metal and passivation
- Depletion region extending from the backside junction

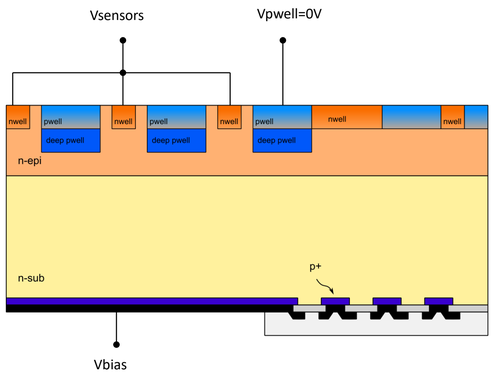
Patented process developed in collaboration with LFoundry

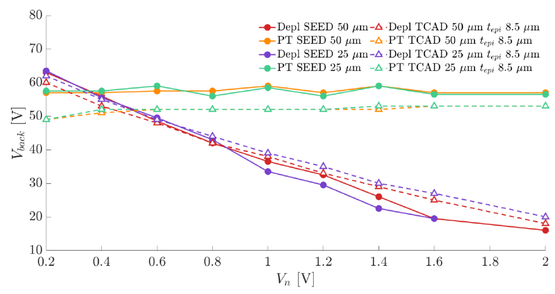
SEED project: concept validation

Test structures:

- Passive pixel arrays with **50µm and 25µm pixels pitch**, read out as a single sensor (all the sensor nodes are connected in parallel). Full depletion and punch-through voltage are extracted and compared with TCAD simulations.
- Backside diodes with different number of guard rings



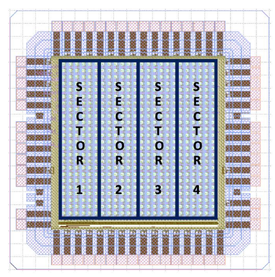


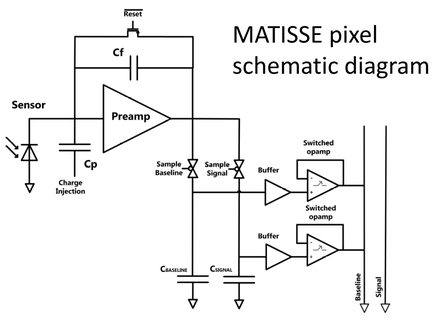


T. Corradino, UniTN

Active pixel array MATISSE:

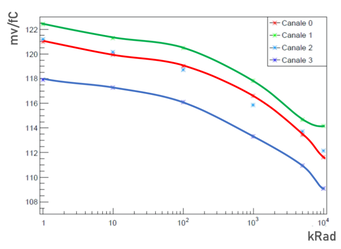
- Designed for charged particle tracking (typ. ~22.5 ke-/event in 300µm substrate)
- 24 x 24 pixel array, divided into 4 sectors with different sensor geometry
- Pixel size: 50µm x 50µm
- In-pixel charge integrating amplifier, S/H and buffer amplifiers
- Operation voltage: 1.2V
- Analog gain: 130mV/fC (2.1mV/100e-)
- Sensor capacitance: 20fF
- Integration capacitance: 70 fF
- Linear output range: 400mV – 950mV
- 4 analog outputs, 5 MHz readout rate
- Frame rate: up to 34 kfps



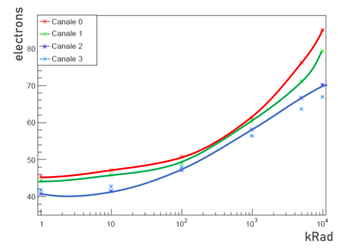


MATISSE pixel schematic diagram

Gain vs total dose



Noise vs total dose



S. Mattiazzo, UniBG

Gain was calibrated with ^{55}Fe source [Left, signal and noise for the SEED 4 quadrants, featuring different CE geometries]. The gain is only slightly affected up to about 1 kGray (100 kRad). TID is done using x-rays (Seifert machine) .

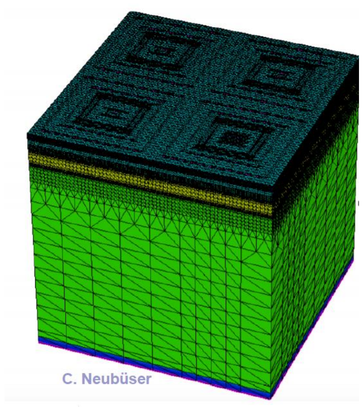
ARCADIA project: new design

Sensor optimization: design

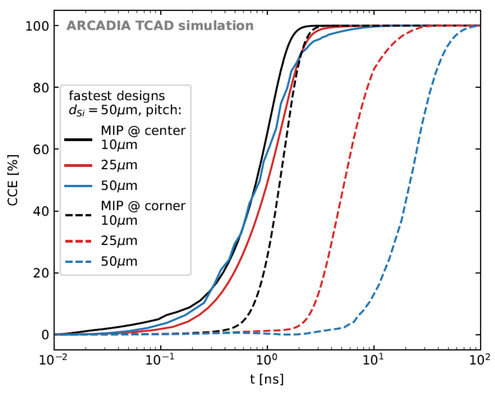
TCAD simulations:

- Operation voltage range
- Sensor capacitance
- Charge collection dynamics
- Charge sharing
- Radiation damage (surface and bulk)

All simulations are repeated for pixels with different pitch, substrate thickness and sensor geometries



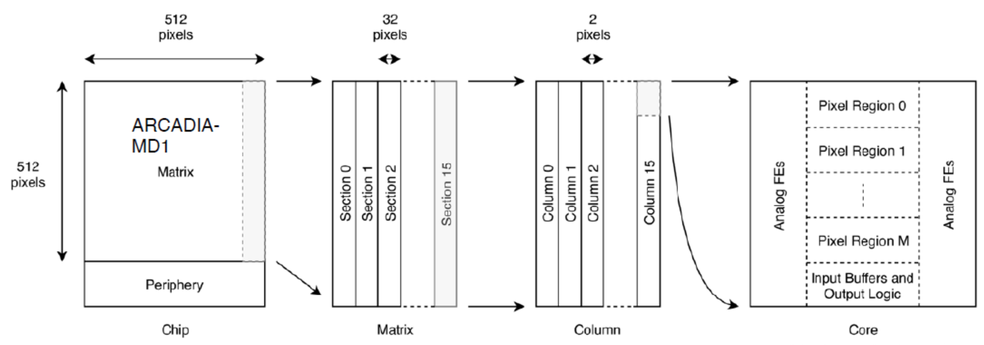
C. Neubüser



C. Neubüser, TIFPA

ARCADIA-MD1 Demonstrator Chip

- Pixel size 25 µm x 25 µm
- Matrix core 512 x 512, "side-abuttable" to accomodate a 1024 x 512 silicon active area (2.56 x 1.28 cm^2).
- Matrix and EoC architecture, data links and payload ID: scalable to 2048 x 2048
- Triggerless binary data readout, event rate up to 10-100 MHz/cm2
- Clock-less matrix integrated on a power-oriented flow, optimizing both static and dynamic power



M. Rolo, INFN Torino

- Pixels are roughly 50% analog, 50% digital; sensor diode about 20% of total area
- Each 2x512 Column is composed of 2x32-pixel cores (the minimum synthesizable entity)
- Cores are sub-divided into 2x4 pixel Regions, which optimize the area by sharing some resources (addressing, data muxing, bus arbitration logic...)

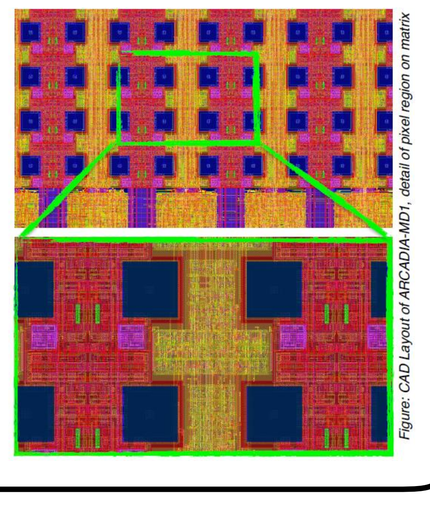


Figure: CAD Layout of ARCADIA-MD1, detail of pixel region on matrix

Project timeline: next steps

Three dedicated SPW runs have been scheduled:

1. 2020-Q4 (wafers have been produced, and are currently being cut),
2. 2021-Q3 (currently in advanced design phase)
3. 2022-Q1

- Runs 2 and 3 allow for the test of new architectures and R&D on new sensor technology (fast timing)
- First triggerless binary data readout full-chip demonstrator samples available in the next weeks
- Multi-plane telescope sensor and DAQ ready for beam tests by Fall/Winter 2021

Acknowledgements

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