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A radiation tolerant 16 Gbps 1:16 Deserializer for High-Energy Physics Experiments

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The paper would present the design and test results of a 16Gbps 1:16 deserializer chip fabricated in 55 nm CMOS technology,which is a part of the optical link ASICs in the Nuclotron-based Ion Collider fAcility (NICA) front-end readout electronics.The input equalizer stage is used to compensate for the high frequency loss caused by the transmission line on PCB and the bonding wire.The strength of equalizer can be configured via SPI module with TMR structure.In order to improve the bandwidth of the high-speed 1:2 DEMUX and high-frequency divider,and save voltage margin,their latches adopt a CML structure without tail current source.We designed duty cycle correction circuit and clock alignment circuit to recover duty cycle and align clock edges. The whole chip consumes 305mW with 1.2V supply when working at 16Gbps.The total jitter of post-layout simulation is 28.2ps.This chip has been taped out and the test results will be reported in the meeting.

TIPP2020 abstract resubmission?

No, this is an entirely new submission.

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