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A 4.5GHz to 5.6GHz PLL in 55 nm CMOS for High-Energy Physics Experiments

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This paper presents the design and test results of a radiation tolerant PLL ASIC as part of the optical link ASICs in the Nuclotron-based Ion Collider Facility (NICA) front-end readout electronics. To obtain low DC leakage current and reduce dynamic mismatch, the charge pump uses two unity-gain feedback operational amplifiers to keep the output common mode voltage constant. The LCVCO employs a novel capacitor array structure to improve the Q degradation due to the source/ drain leakage current from the binary controlled MOS transistor. All adjustable bits can be controlled by the SPI module, which is also strengthened with the Triple Modular Redundancy (TMR) structure. The PLL covers a wide-frequency range from 4.5GHz to 5.6GHz, consuming a total power of 25 mW from the post layout simulation. At 5.12GHz, the phase noise is -115 dBc/Hz @ 1MHz offset. The chip has been taped out and the tests are planned to be conducted in this March. The test results will be reported in the meeting.

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Primary author: ZHAO, Cong (Central China Normal University)

Co-authors: Mr CHEN, Qiangjun (Central China Normal University); Prof. GUO, Di (Central China Normal University); Mrs GUO, Zengtao (Central China Normal University); Mrs GAN, Yujing (Central China Normal University)

Presenters: ZHAO, Cong (Central China Normal University); Prof. GUO, Di (Central China Normal University)

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