A possible design of the readout electronics for large area SiPM detectors of the TAO experiment

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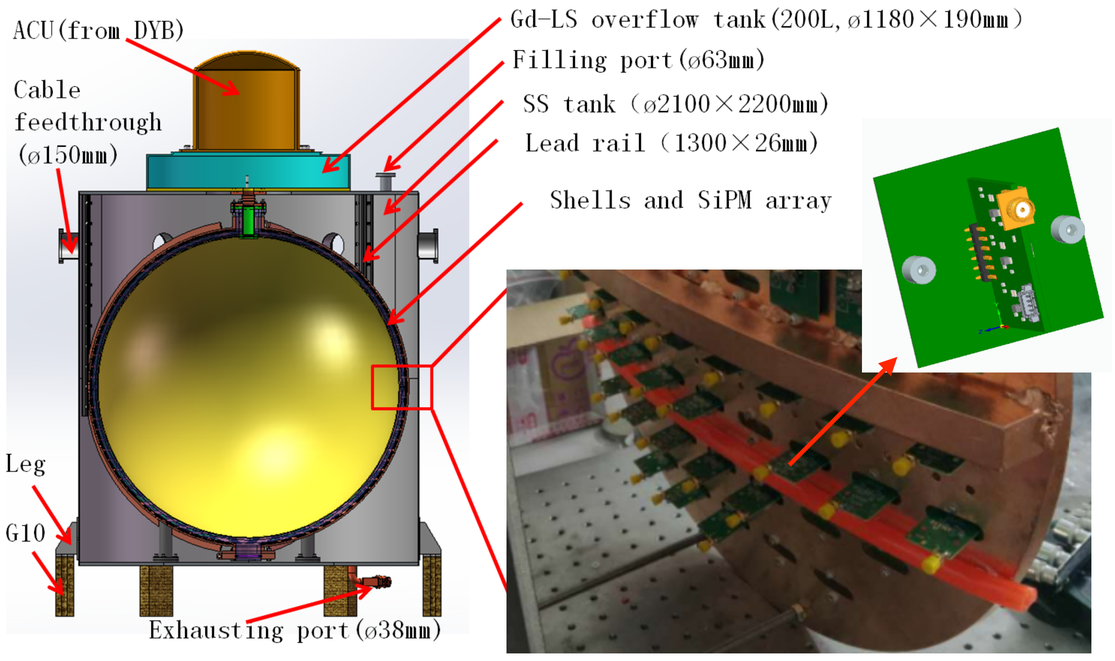
The Taishan Antineutrino Observatory

Motivation

- Precisely measure the reactor antineutrino spectrum with energy resolution at the level of ~2% at 1 MeV.
- Provide a model independent reference spectrum for JUNO
- Reactor monitoring and safeguard
- Search for sterile neutrino

General properties

- Gd-doped liquid scintillator
- Very close (~30 m) to Taishan reactor core 1 (4.6 GW_{th})
  - Expected rate ~4000 antineutrinos per day
- ~10 m^2 SiPM Readout
- Detector operated @ -50 °C



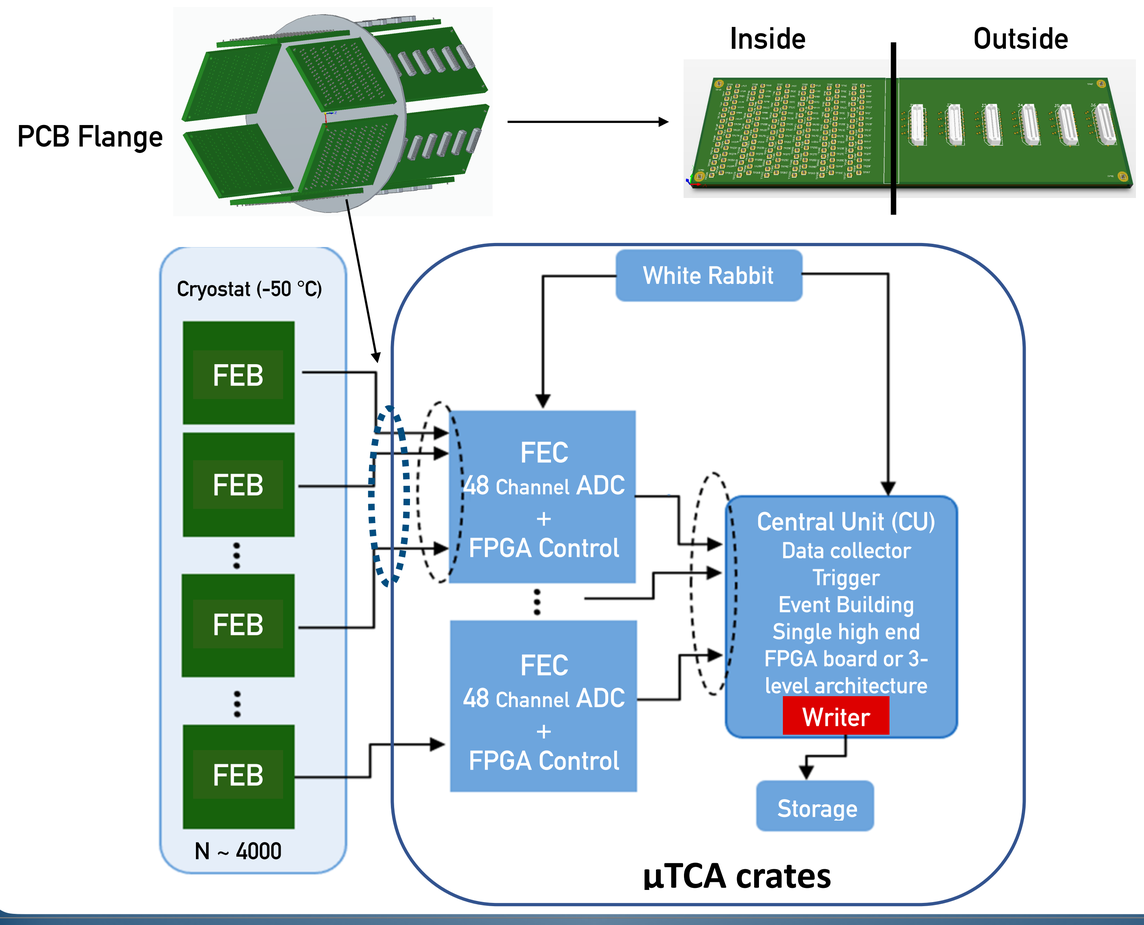
TAO Readout Electronics

Front-End board

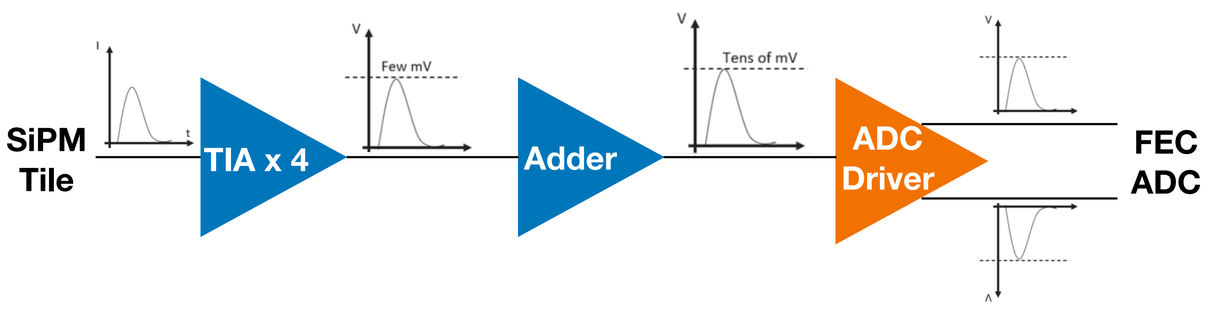
- 1 channel = 1 tile
- Total ~4000 channels
- Analog signals from FEB will be transferred to FEC via differential pairs, 3-4 m inside the SS tank, ~10 m outside the tank
- Custom made pcb flanges to bring signals outside the tank

Front-End Controller

- Host the ADCs
- 1 FEC = 32 or 48 channels
- Real time waveform analysis on FEC FPGA to extract (Q,t) pairs
- White Rabbit for clock distribution

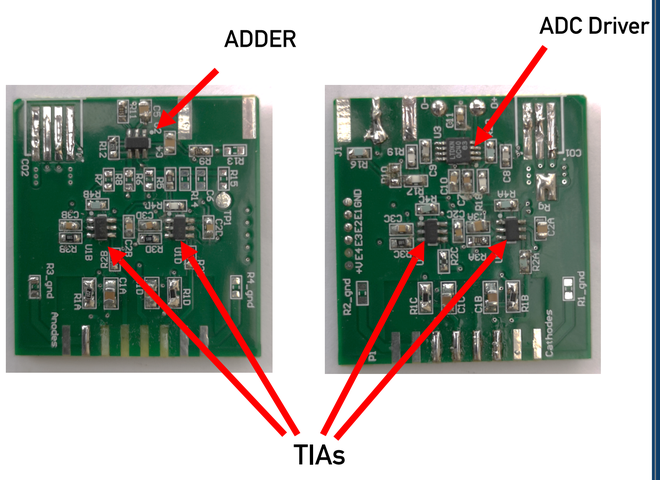


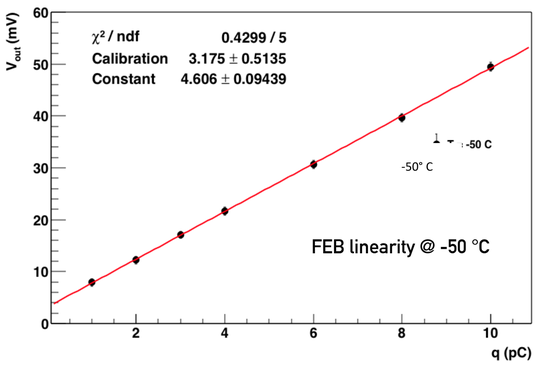
Front-End Board

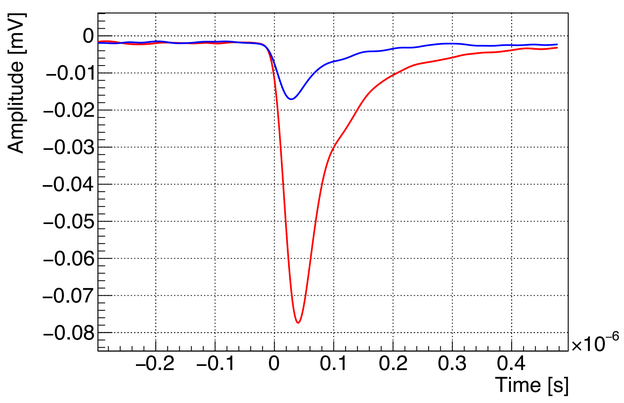


FEB Features

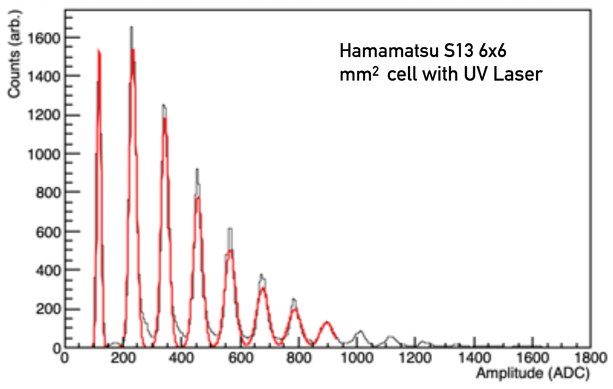
- SiPM elements of each tile are splitter in 4 Transimpedance amplifier
- More TIAs can be added in order to reduce input capacitance
- ADC driver for differential output allows having ~10 meters cable between FEB and ADC
  Single PE amplitude ~8 mV
- 0V-2V output range: matches the input range of the ADC
- Dynamic range 1-250 PE







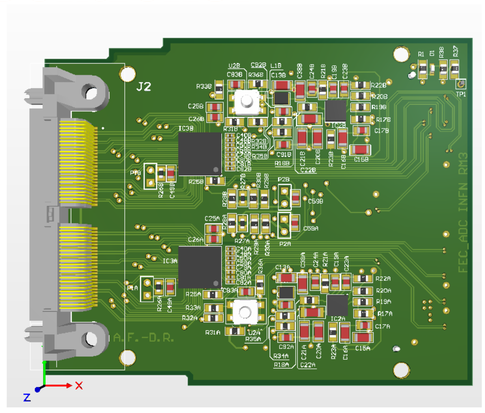
- Good stability @ -50 °C
- Extensively tested @ -70 °C without any failures
- Low background PCB materials under test (Pyralux, Aramid)



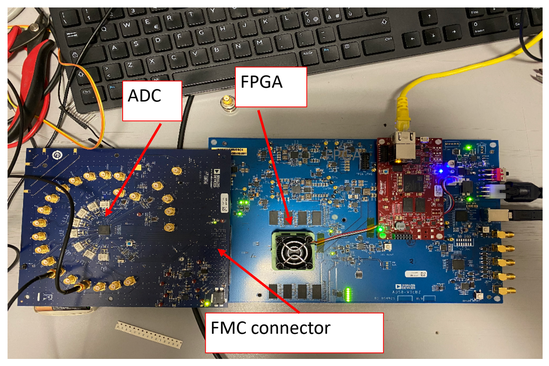
Front-End Controller

FEC Prototype

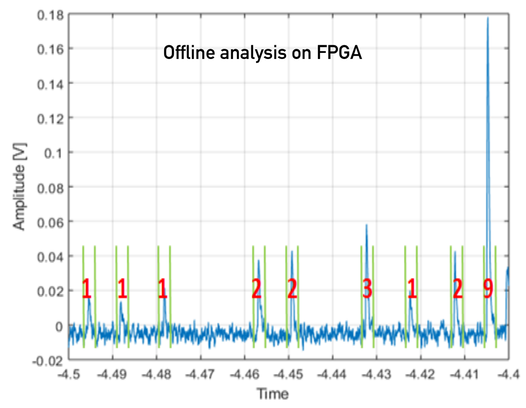
- AD9083 ADC board
- FPGA Control (Kintex 7)
- Ethernet connection with PC
- 250 MS/s, 125 MHz Bandwith
- 16 Channels
- Differential 2Vpp input

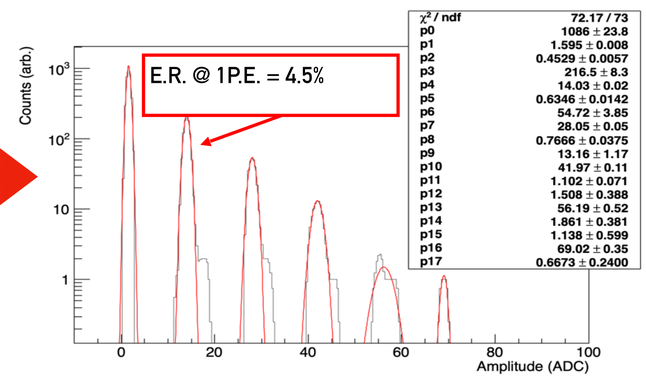


FEC Designed to be hosted in µTCA Crate



- FPGA compute Q,T in real time for each ADC input
- Q,T can be sent in form of number of PE or raw area value
- Full waveform can be transferred during calibration or commissioning





Conclusions

- FEB prototypes extensively tested: match the TAO requirements
  - High reliability
  - Very flexible in terms of gain, shaping time, dynamic range, granularity
- FEC first prototype shows design feasibility
  - Protoype shows the possibility of real time waveform analysis on FPGA

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