CMS ECAL upgrade for precision timing and energy measurements at the High Luminosity LHC

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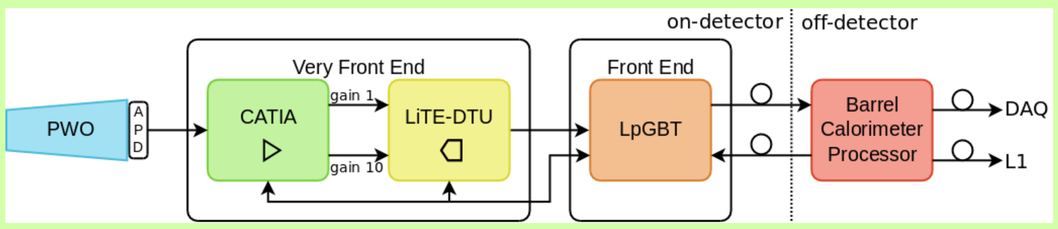
The CMS ECAL Phase 2 upgrade

The **High Luminosity upgrade of the LHC (HL-LHC)** at CERN will provide an unprecedented instantaneous luminosity of $5x10^{34}$ $cm^{-2}s^{-1}$, leading to an average of 150-200 simultaneous collisions. The current CMS electromagnetic calorimeter (ECAL) [1], consisting of 75848 lead tungstate (PbWO4) crystals arranged in a barrel section and two endcaps, will need to be upgraded to handle the HL-LHC conditions. During the long shutdown 3 of the LHC the endcap part of the ECAL will be replaced with a new detector. The 61200 crystals of the ECAL barrel [2] and their avalanche photodiodes (APDs) will be kept for the HL-LHC runs.

The **crystal temperature will be lowered from 18°C to 9°C** to keep the APD noise below 250 MeV. The **front end and the back end electronics will be replaced** to cope with the 7.5 fold increased Level 1 (L1) trigger and readout rate and to achieve a timing resolution of 30 ps.

Data compression in combination with high bandwidth optical connections allow to send **single crystal information from the on-detector electronics to the off-detector processor boards**. The processor boards feature powerful field programmable gate arrays (FPGAs) to generate **trigger primitive (TP) information with crystal level granularity** and send it to the L1 trigger for more selective trigger algorithms.

The **30 ps time resolution** allows to determine the vertex position with 1 cm precision and is achieved with a shorter pulse shape and a four times higher sampling rate of 160 MHz. The shorter pulse shape allows to **distinguish scintillation signals from APD direct ionisation signals** (spikes). The spike signals need to be suppressed since they would otherwise dominate the trigger rate.



Block diagram of the ECAL barrel Phase 2 upgrade electronics

Front end ASICs

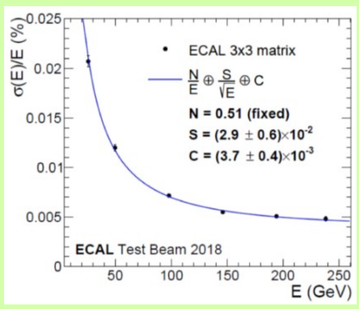
Two custom radiation tolerant application specific integrated circuits (ASICs) are designed for the ECAL upgrade. A pre-amplifier ASIC and an ADC that also prepares the digitized samples for transmission to the back end.

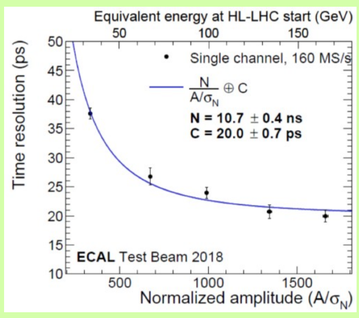
CATIA (Calorimeter Trans-Impedance Amplifier)

Fabricated in 130 nm CMOS technology, the dual gain CATIA outputs signals with gain 1 and gain 10. The **two gains cover the range from tens of MeV up to 2 TeV.** The TIA circuit allows for a reduced shaping time of the signal. This is required for the desired timing performance and to reduce the APD leakage current contribution to the noise term. The CATIA also presents trimable voltage levels for ADC calibration.

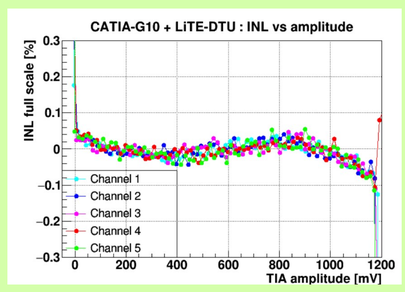
LiTE-DTU (Lisbon-Torino ECAL Data Transmission Unit)

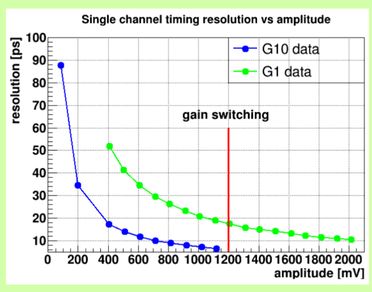
Fabricated in 65 nm CMOS technology, the LiTE-DTU achieves the 160 MHz sampling rate using **two interleaved 80 MHz 12 bit ADC** IP blocks from the commercial company Dialog Semiconductor. The effective number of bits of the ADC is specified to 10.2 bit at 50 MHz. The LiTE-DTU also houses custom **logic for the gain selection and data transmission**, including a lossless data compression scheme and a 80 MHz fallback mode that can be used for noisy channels.





Energy (top) and time (bottom) resolution of the CATIA from 2018 beam tests





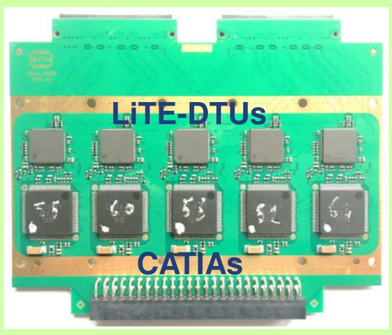
Amplitude linearities (left) and single channel time resolution (right) of CATIAs with LiTE-DTUs

Front end electronics boards

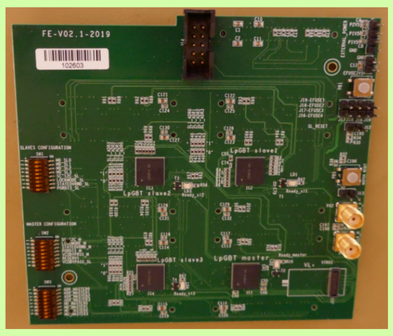
The **Very Front End (VFE)** (12240 cards) is connected to the crystal APDs via the passive motherboard, which will be kept from the current ECAL. Each VFE houses five CATIA and LiTE-DTU ASICs to read out and digitize five crystal signals.

The **Front End (FE)** (2448 cards) collects the signals of five VFE cards and sends the data to the off-detector back end board via 10 Gb/s optical links. The required data rate for data readout and the receiving of clock and control signals from the back end is achieved using four Low-power Gigabit Tranceiver (LpGBT) chips. Versatile Link plus (VL+) technology is used for the connection to the back end.

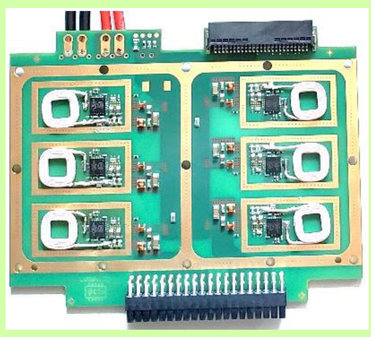
Power is distributed to the VFEs and FE via the **Low Voltage Regulator (LVR)** card (2448 cards). It houses radiation hard DC-DC converters of the FEAST or bPOL type to step down the low voltage fed into an ECAL supermodule to the voltage required by the ASICs. The power consumption of the front end electronics could be reduced by 50% compared to the current ECAL. This and the higher voltage level delivered to the LVR allowed to significantly reduce the low voltage cable diameter.



Prototype VFE card v2 with five CATIA and five LiTE-DTU chips



Prototype FE card v2.1 with four LpGPTs and VL+ optical link

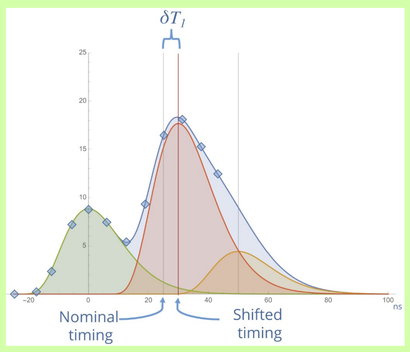


Prototype LVR card v2 with six DC-DC converters

Trigger primitive algorithms

The algorithms running on the BCP reconstruct two sets of TPs that are then sent to the L1 trigger. A 16 bit **single crystal TP** consisting of the transverse energy, time information, and APD spike flag bit. The **crystal cluster TP** is generated from a 3x3 or 3x5 cluster of crystals and consists of 40 bits to encode the transverse energy, position, time, and spike flag of the cluster. The algorithms are implemented using the Xilinx Vivado High Level Synthesis (HLS) tools.

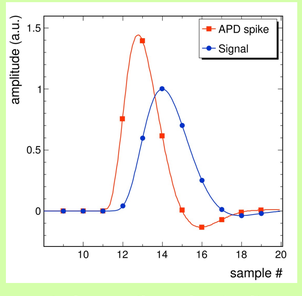
A **linearised multifit-timing algorithm** [3] is used for the reconstruction of the transverse energy and the time information. An **in-time pulse amplitude** is calculated from 12 consecutive samples using a least squares **linear algebra technique** in the presence of two out-of-time pulse shapes. Allowing for small shifts of the pulses from their nominal arrival time, in combination with a first order Taylor expansion of the sample values, is used to calculate the **timing of the pulse** with respect to the nominal arrival time.



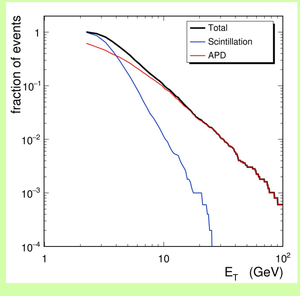
A linear combination of the central in-time pulse shape with two out-of-time pulses before and after result in the sample values (Blue diamonds)

Two algorithms are used to calculate the APD spike flag. The **linear discriminant (LD) algorithm** exploits the difference in shape between a spike signal and a scintillation signal. The spike signal has a faster rise time and is shorter than a scintillation signal. Three consecutive samples are used to calculate an LD variable that is used for the **discrimination between spike signals and scintillation signals**.

The **swiss-cross algorithm** calculates a spike flag using ratios between the energy in the central crystal and the adjacent neighbouring crystals. For spikes the central crystal contains almost all the energy while for signals from showers the adjacent crystals contain a significant fraction of the total energy.



A short spike pulse (red) compared to a longer scintillation pulse (blue)



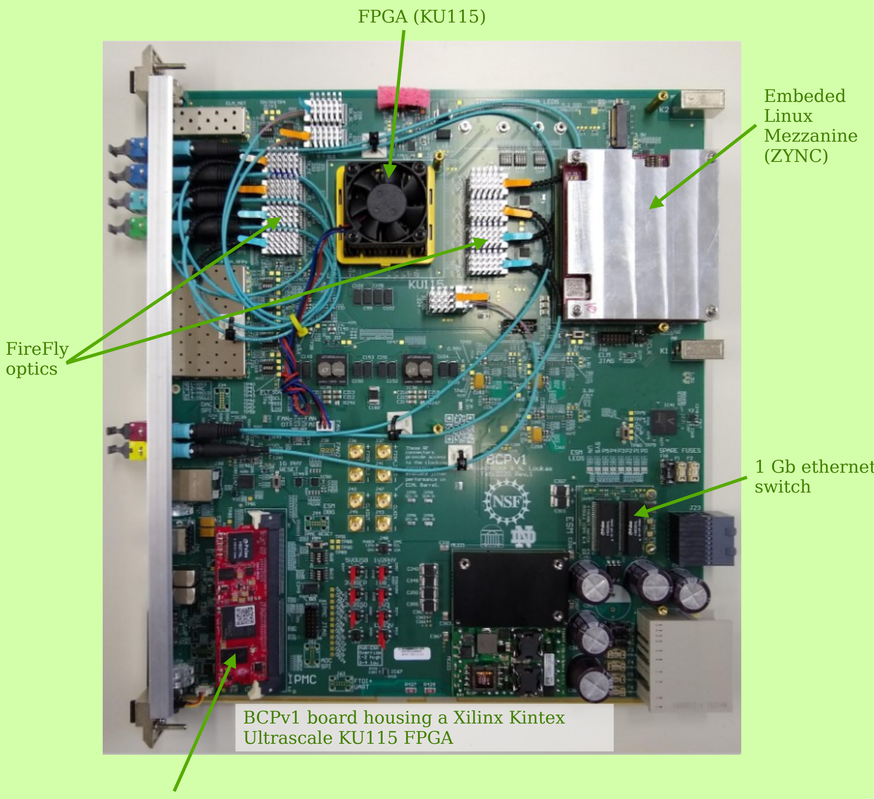
Contribution of spike and scintillation pulses to the total number of events as a function of transverse energy

Back end electronics

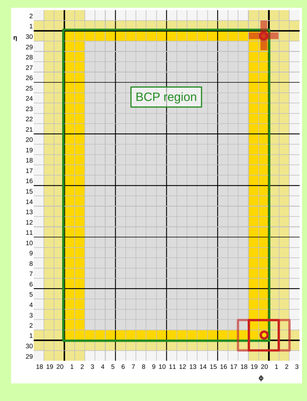
The back end electronics is housed in the CMS service cavern and does not require a radiation tolerant design. It receives the signal samples for each crystal via optical fibres and **provides the samples to the data acquisition system** (DAQ) when a trigger signal is received. In addition, it **generates trigger primitives for the L1 trigger**, including the flagging of anomalous APD signals and provides the clock and control signals for the on-detector electronics.

The **Barrel Calorimeter Processor (BCP)** is a custom designed Advanced Telecommunications Computing Architecture (ATCA) board that houses a large Xilinx **Virtex Ultrascale Plus VU13P FPGA**. Each card serves up to 600 channels and 108 cards are required to cover the whole ECAL upgrade. The connection to the DAQ and the FE electronics is made with **SAMTEC FireFly optics capable of transmitting up to 25 Gb/s**. A mezzanine board housing a Xilinx **ZYNC FPGA, running a Linux operating system is used to control the board**. The BCP is also going to be used in the CMS barrel hadronic calorimeter readout.

The BCPv1 is a prototype board with a Xilinx Kintex Ultrascale KU115 FPGA and is used to develop the firmware and test the interface with the FE and with the DAQ.



The generation of 3x3 or 3x5 crystal cluster energy TPs and the swiss-cross anomalous signal identification method requires the **sharing of crystal information between BCP boards**. A passive **optical fibre router** is developed to make the required connections to BCPs serving the adjacent regions.



30x20 channel BCP region with shared crystals in yellow and crystal cluster and swiss cross examples in red

References

[1] CMS Collaboration, *The CMS electromagnetic calorimeter project: Technical Design Report*, CERN-LHCC-97-033 (1997)
[2] CMS Collaboration, *The Phase-2 Upgrade of the CMS Barrel Calorimeters*, CERN-LHCC-2017-011 (2017)
[3] CMS Collaboration, *Reconstruction of signal amplitudes in the CMS electromagnetic calorimeter in the presence of overlapping proton-proton interactions*, JINST 15 (2020) 10, P10002