The QPIx pixilated readout concept for future Liquid Argon Time Projection Chambers: status and prospects.

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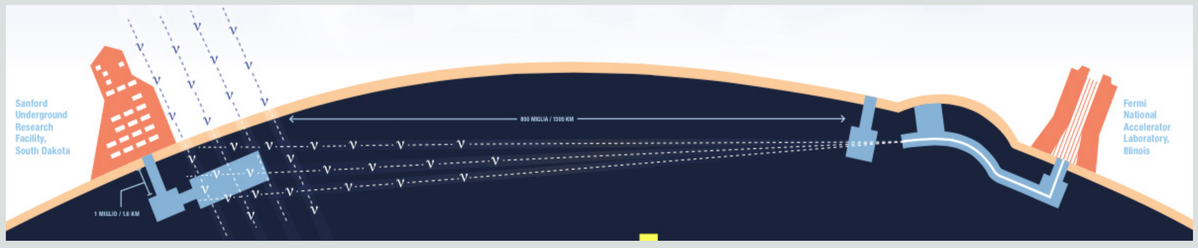
ABSTRACT

Future long baseline neutrino experiments such as the Deep Underground Neutrino Experiment (DUNE) pose challenges for development of readout techniques for multi-kiloton LAr Time Projection Chambers (TPC). In contrast to wire/strip anode readout, a pixilated readout eliminates disadvantages such as disambiguation in 2D track reconstruction. The Q-Pix Consortium, established in 2019, is developing a pixilated readout technique for LAr TPCs based on charge-integrate/reset (CIR) circuits. The CIR blocks generate a sequence of reset pulses with time intervals corresponding to fixed charge integrals, allowing signal reconstruction without continuous digitization. The Q-Pix ASIC, intended for reading out pixel arrays, comprises CIR blocks along with digital components responsible for communication and reconfigurable data routing. This work is devoted to give an overview of the Q-Pix project, its status, and prospects, with emphasis on the development and prototyping of the Q-Pix readout ASICs.

INTRODUCTION

DUNE: the next big thing in ν physics



Burning questions in ν physics

- $\theta_{12}, \theta_{13}, \theta_{23}$
- $\Delta m^2, \delta m^2$
- N_ν
- δ_{CP}
- $sign(\Delta m^2)$
- α_1, α_2
- m_x
- $P \infty ?$

International flagship project in the HEP panorama.

Far Detector: **4 gigantic LArTPCs (10kTon, 18x19x66 m³ each)**

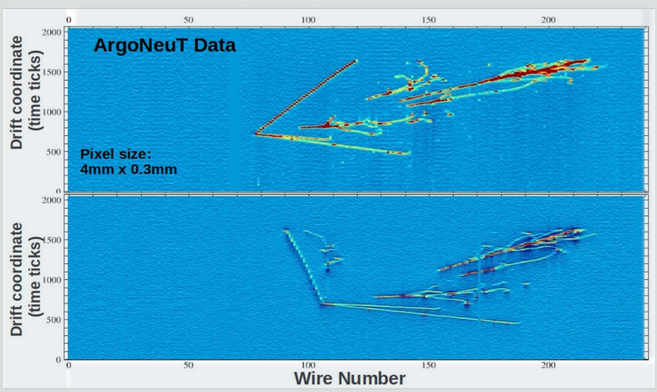
1 mile underground

→ Explore CP violation in neutrino sector
→ Precision Measurements of Neutrino Mixing
→ Neutrino Mass Hierarchy
→ Rare BSM processes (proton decay, nnbar oscillation) & SN
→ < Your new idea here!!! >

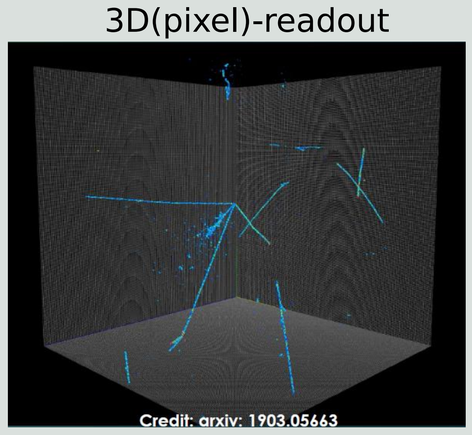
Set to run for 10+ years

LAR TPC WITH PIXILATED READOUT

2D(wire)-readout



3D(pixel)-readout

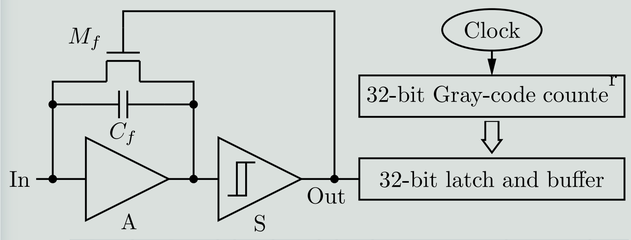


Conventional Liquid Argon Time Projection Chambers (LArTPCs) utilize sets of wire planes to detect and collect charge. This strategy, adopted as the baseline design for the DUNE experiment compromises the inherent precision of TPC.

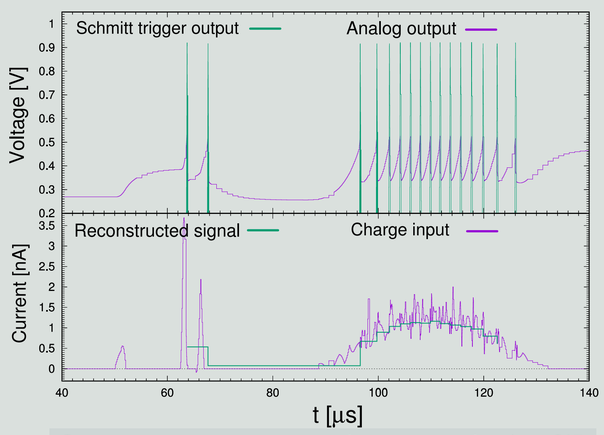
Pixilated readout allows to avoid ambiguities in the track reconstruction. It requires unconventional design to meet power, data rate and other requirements. The Q-Pix concept is a novel readout technique aimed for large scale TPCs with relatively low event rates.

Q-PIX CONCEPT

The Q-Pix readout scheme allows for a low data rate measurement of integrated charge using pixel-scale self-triggering charge integrate-reset (CIR) blocks. Time difference between reset pulses allows for reconstruction of the integrated charge being collected.

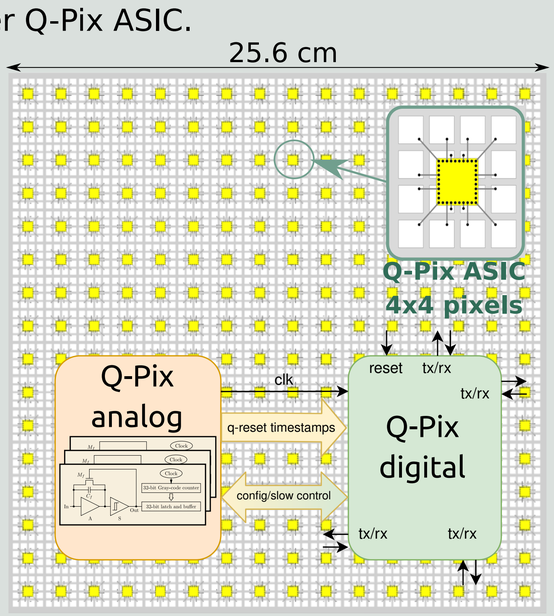


Q-Pix CIR block with timestamping unit connected to it



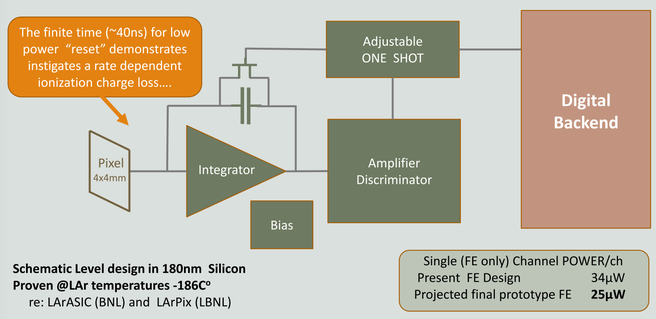
Charge integration simulation results for CIR block with ΔQ of 1 fC

In order to reduce power consumption and minimize possible crosstalks the baseline design uses individual oscilator per Q-Pix ASIC.



A "tile" as a basic unit of 16x16 ASICS (4096 4mmx4mm pixels)

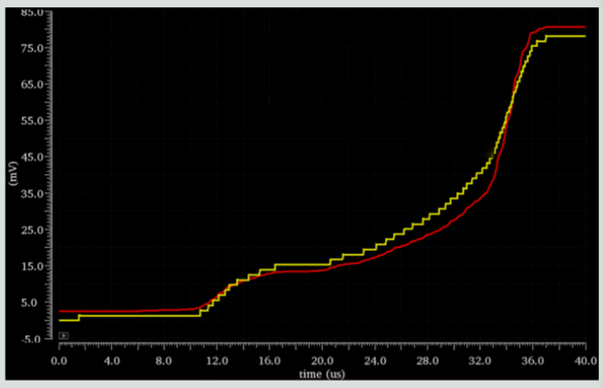
ANALOG CHIP COMPONENT



Schematic Level design in 180nm Silicon
Proven @LAr temperatures -186C°
re: LArASIC (BNL) and LArPix (LBNL)

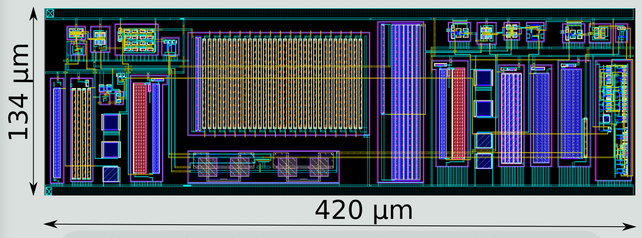
Single (FE only) Channel POWER/ch	
Present FE Design	34μW
Projected final prototype FE	**25μW**

Q-Pix analog frontend diagram



An example physics event simulated for the Q-Pix circuit. It shows reconstruction of the total integrated charge (reconstructed signal in yelow and original signal is red). Each reset pulse corresponds to approximately 1fC of charge.

A baseline design has been completed at the schematic and layout levels in 180 nm technology, with total power requirement of less than 40 uW per channel.



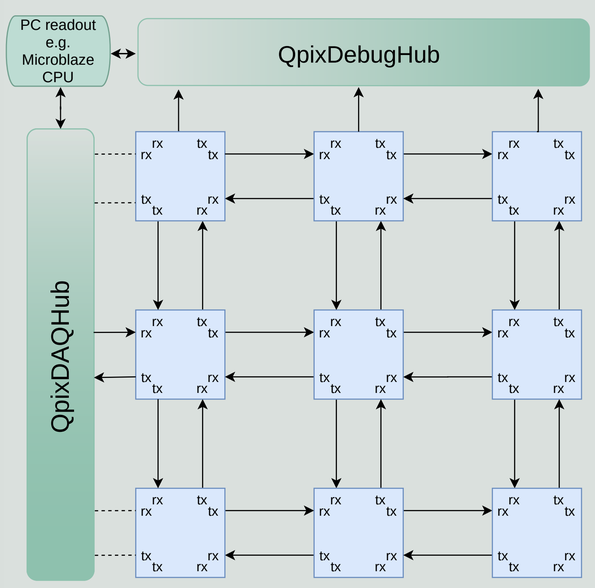
Full replenishment channel layout.

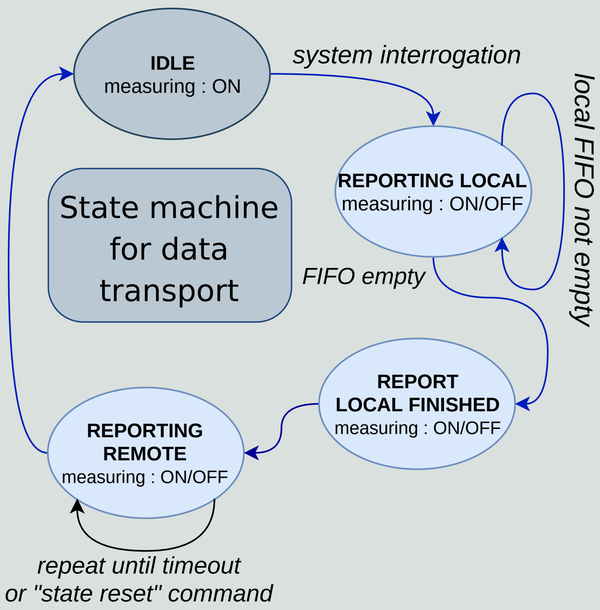
A number of different design options are being explored which include: break-before-make switches for continuous charge integration and full replenishment circuitry.

Q-PIX DIGITAL

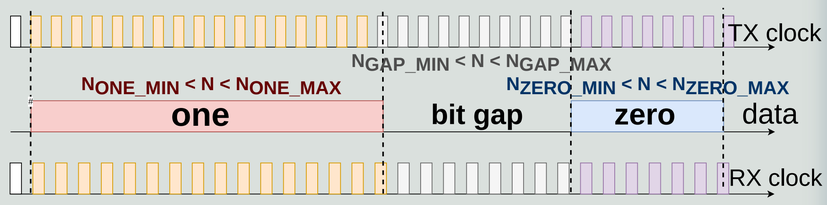
The digital aspect of the Q-Pix will utilize synthesized logic in order to implement inter-ASIC communications, readout state machines, and slow control pathways. ASICs generally pass data through one another to a given DAQ node, where data can be extracted and transmitted to the backend system.

A full design of the Q-Pix difital component has been implemented in a Xilinx Zynq-7 FPGA including multiple ASIC blocks arranged in an array to emulate ASIC-to-ASIC functinality

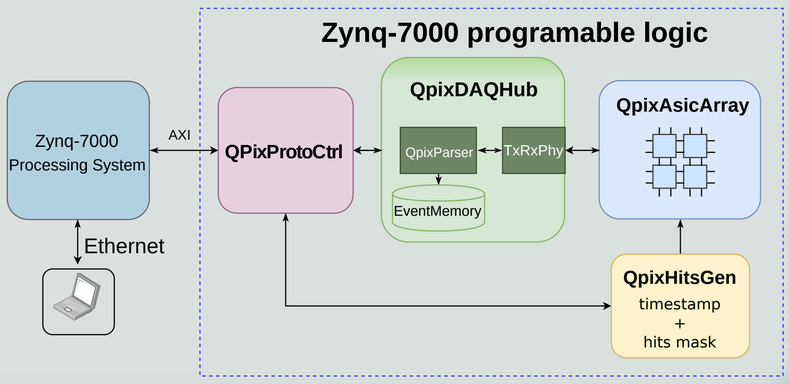




The baseline for inter-ASIC communication is the Penn "Endeavor" Morse-like protocol originally developed for AMAC ASICs.



The FPGA prototype of Q-Pix digital component includes the ASIC array, prototype of the DAQ readout and the block for injecting hits into the array. This allows for testing the full readout chain with realistic MC hits for different particle types.



CURRENT STATUS

First versions of the Q-Pix analog and digital designs are planned for submission for fabrication later this year. The analog and digital components will be pursued as separate ASIC submissions in order to mitigate risk and allow maximum flexibility for testing.

REFERENCES

D.A. Dwyer et al., "LArPix: Demonstration of low-power 3D pixilated charge readout for liquid argon time projection chambers" JINST 13 P10007 (2018).

D. Nygren and Y. Mei, "Q-Pix: Pixel-scale Signal Capture for KilotonLiquid Argon TPC Detectors: Time-to-Charge Waveform Capture, LocalClocks, Dynamic Networks" arXiv:1809.10213 (2018).