The Monitoring of Pixel System (MOPS) chip for the Detector Control System of the ATLAS ITk Pixel Detector

Technology and Instrumentation in Particle Physics (TIPP 2021)

The ATLAS experiment will get a new inner tracker (ITk) during the phase II upgrade. The innermost part is called the Pixel Detector. A new Detector Control System (DCS) is being developed to provide control and monitoring of the ITk pixel detector. The Monitoring of Pixel System (MOPS) chip is an Application Specific Integrated Circuit(ASIC) foreseen in the DCS to independently monitor the voltage and the temperature across the modules which constitute the front end electronics responsible for tracking and data readout. The modules which need to be monitored are powered serially in a chain. The MOPS chip has a 12-bit ADC which can read up to 34 channels. Controller Area Network (CAN) and CANopen protocols are used for communication. The final chip is required to be radiation hard up to an ionizing dose of 500 Mrad.

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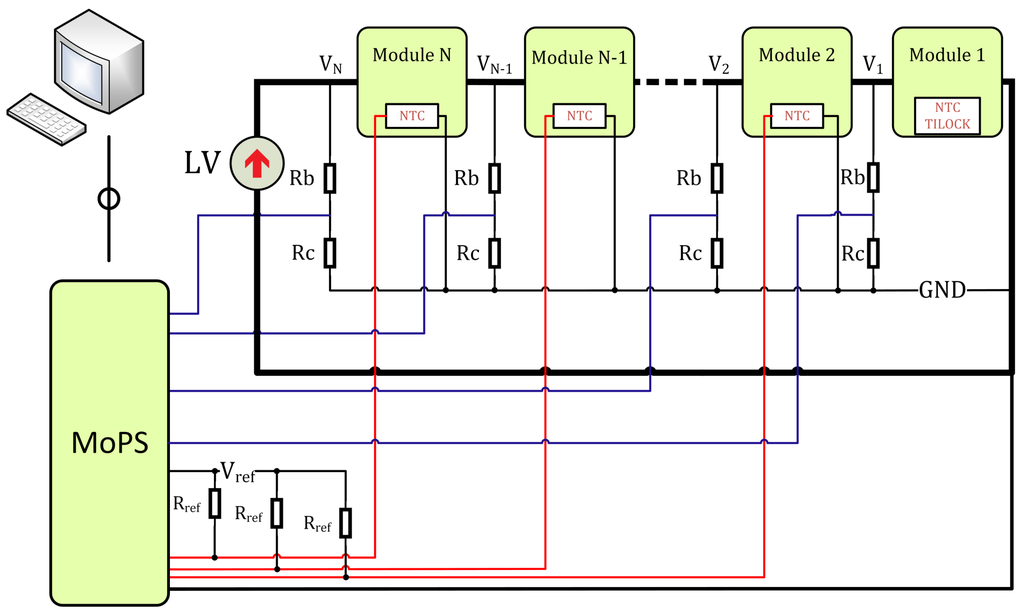
Detector Control System (DCS) of the ATLAS ITk Pixel Detector

The MoPS is an Application specific Integrated Circuit (ASIC) planned to be used in the control & feedback path of the ITk pixel DCS. The blue lines shown in the figure below are for voltage monitoring and red lines represent temperature monitoring. A voltage divider network is used to translate voltages up to 32 V to the input range of the ADC. The chip is located on the EoS/PPO board/services as shown in Fig.

- 2N+1 lines to monitor N modules
  - N+1 voltage
  - N-1 temperature
  - 1 return line
- Communicates over CAN bus to the main DCS computer
- Concept of CANopen standard is used at the application layer
- Reference voltage for the NTCs is provided by the chip
- Radiation tolerance requirements are the same as for the front-end (FE) chips

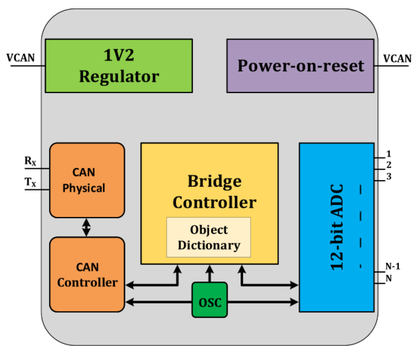


MOPS requirements

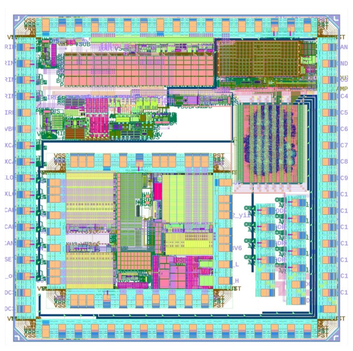
- Measure temperatures and voltages for individual modules in a serial power chain
  - Expected: 15 Temperatures
  - 16 Voltages
- Independent monitoring from DAQ system
- CAN bus speed of 125 Kbps
- CANopen based application layer protocol for data exchange with the DCS computer
- Radiation hard design up to an ionizing dose of 500 Mrad & SEE tolerant
- Working temperature Range -40 °C to +60 °C (no active cooling)
- Supports communication over cable length of at least 70m
- Packaged in a 9 mm X 9 mm case
- TSMC 65nm technology

MOPSv1

The proposed ADC is an SAR-type ADC with a resolution of 12 Bits. Using an analog multiplexer up to 40 Channels can be read. The ADC and accompanying analog multiplexer is a design which has been developed by the RD53 collaboration. This is the same ADC which will be used for the front-end (FE) chip of the ATLAS ITk Pixel Detector. Since the input voltage range of the ADC is 0-850mV the input voltages are divided by an external individual resistor divider network for each channel.



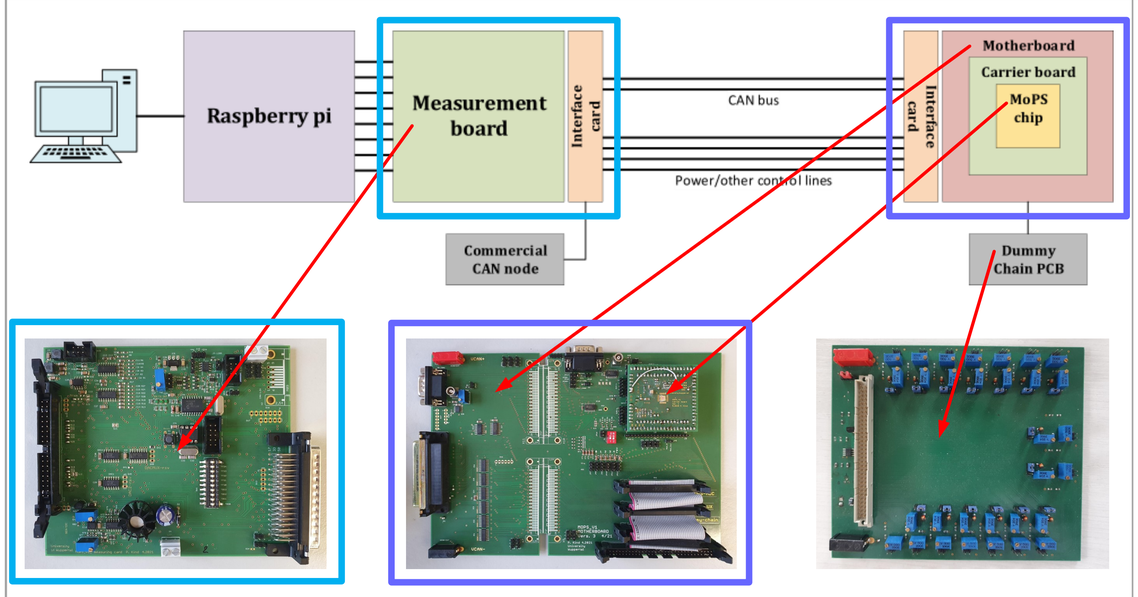
MOPSv1



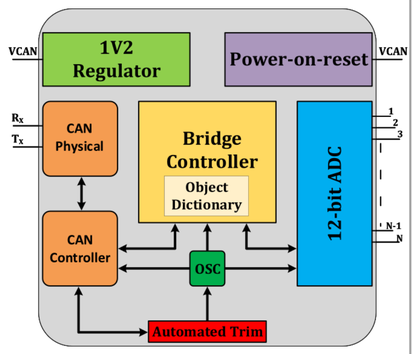
Layout

Complete digital logic of the MOPS chip has been implemented using Triple Modular Redundancy (TMR) to mitigate SEUs effects

Test setup and Planned MOPSv2



- Raspberry pi to allow flexibility of linux and remote operation during radiation campaigns
- Measurement board hosts commercial ADCs / DACs to provide & compare dummy monitoring values for the MOPS chip as well as power supplies / controllers
- Dummy chain PCB mimics an actual serial power chain using simple potentiometers

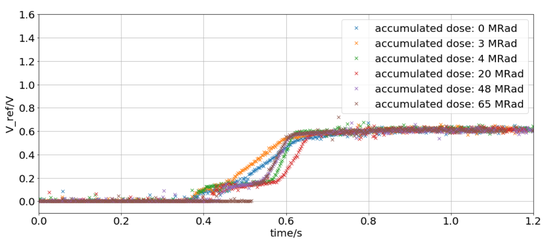


MOPSv2

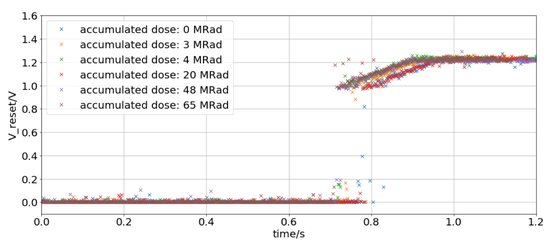
- Automated trimming for the oscillator to compensate for the process variation
- Enhanced tolerance for frequency mismatch on the bus
- Design improvements and fixed bugs

MOPSv1 functionality, irradiation and climate chamber test results

- Overall performance of the MOPSv1 is promising. All building blocks of the chip are working fine
- MOPSv1 survived Total Ionizing Dose (TID) of 500 Mrad with a dose rate of 200 Krad/h for upto 4 Mrad total dose and then 2 Mrad /h
- The chip has also been tested for temperatures between -15°C to +60 °C



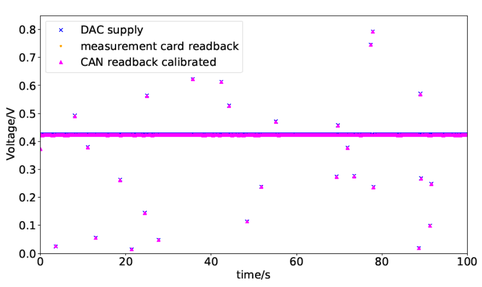
Bandgap refernce at different dose levels



Power on reset at different dose levels

Bandgap output voltage slope during ramp up of the power supply is different for different levels of the accumulated dose. The slope is less steep due to the fact that radiation dose rate is much slower. Because of this threshold of the NMOS transistor changes for this particular CMOS process.

Read out figure shows precision of the MOPS chip after accumulating radiation dose of 500 Mrad.



Readout using commercial ADC vs MOPS

The two figures on the right side shows Controller Area Network (CAN) physical layer signals on the CAN bus and different Analog voltages on the chip during power supply ramp-up after accumulating radiation dose of more than 500 Mrad.

The three plots shown below are for the temperature dependence of the MOPS chip. Starting from left, the first plot shows the maximum possible rise time of the power supply at different temperature values for which the MOPS starts up correctly. MOPSv1 has problems starting up for rise time larger than 30 ms at -15 degree Celsius. The problem is still not clear if this is due to the Bandgap on-chip or the test setup. At 10 °C and onwards the chip has no problem to startup even with a rise time of 6500 ms

The other two plots show variation of the oscillator frequency and output of the bandgap circuit wrt to temperature.