Upgrade of the ATLAS Level-0 Endcap Muon Trigger for HL-LHC

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Abstract

High Luminosity LHC (HL-LHC) is an upgrade of LHC that aims to achieve higher luminosity, enabling experiments to reach better physics sensitivity. Operation of HL-LHC is scheduled to start in 2027 with an instantaneous luminositiy of 7.5 x 10^{34} $cm^{-2}s^{-1}$. To cope with the high luminosity at HL-LHC, the trigger and readout system of the ATLAS detector will be replaced. The design for the level-0 endcap muon trigger of the ATLAS experiment at HL-LHC and the status of the development are presented.

Introduction

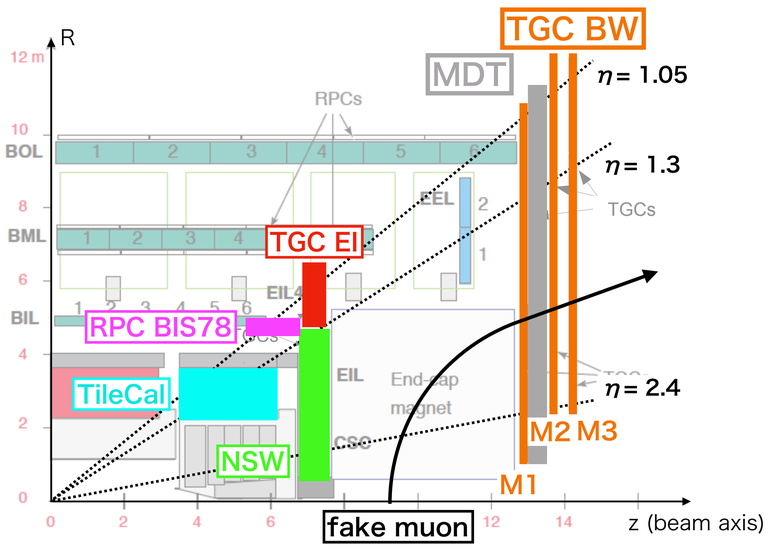
- Main detector of endcap muon trigger
  - Thin Gap Chamber on Big Wheel (TGC BW)
    - Multi wire-proportional chamber
    - Two-dimensional position measurement using signals from wires and strips orthogonal to wires
    - Consisting of three stations, M1 (wire: 3 layers, strip: 2 layers), M2 (2 layers) and M3 (2 layers)
- Inner detectors
  - TGC in Endcap Inner station (TGC EI)
  - Resistive Plate Chambers (RPC BIS78)
  - Tile hadronic calorimeter (TileCal)

  Covering complementary phi regions in $1.05 < |\eta| < 1.3$
  - New Small Wheel (NSW) : Tracking in $1.3 < |\eta| < 2.4$ by small-strip TGC and Micromegas

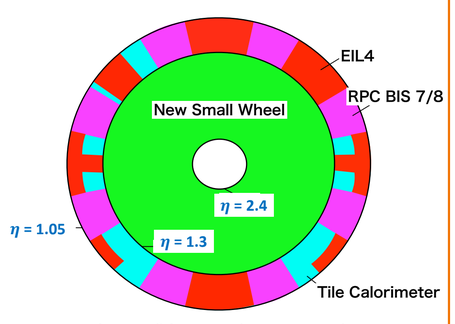
◆Original algorithm of level-1 endcap muon trigger in Run 1-3
- Muon track candidates identification by simple coincidence logic in on-detector boards on TGC BW
- Transverse momentum (p_T) evaluation by look-up tables in off-detector trigger logic boards
- Signals from inner detectors used to take coincidence with TGC BW to suppress backgrounds such as low-p_T "fake" muons from out of interaction point

◆New algorithm for level-0 endcap muon trigger for HL-LHC
- All hit information from TGC BW transferred to off-detector boards used to reconstruct track segments
- Complex coincidence logic of combination of TGC BW track segment with signals from inner detectors → Improved p_T resolution
- Monitored Drift Tube (MDT) is used to improve p_T resolution succeeding the decision by TGC and inner detectors

◆Trigger logic of TGC BW and inner detectors implemented in an FPGA on Sector Logic boards (SL)



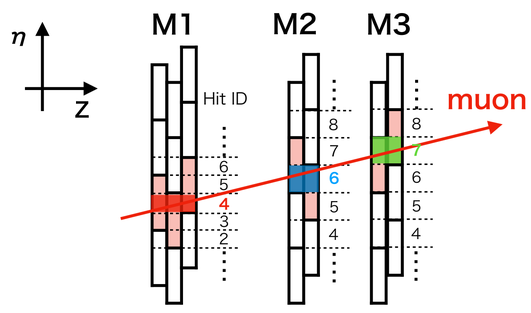
R-Z view of ATLAS muon detectors layout [1]



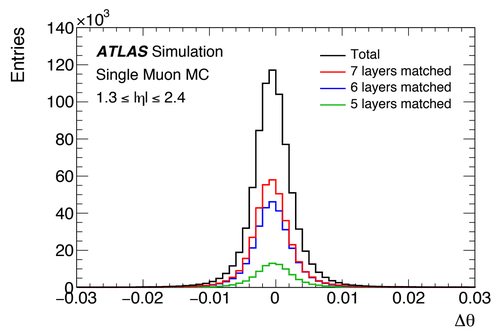
x-y view of inner detectors layout

TGC track segment reconstruction

- **"Pattern Matching"**
  1. Compare TGC hits with pre-defined hit lists for high p_T muons
  2. Each pre-defined hit pattern returns position and angle information



input: Hit ID → output: Position, Angle

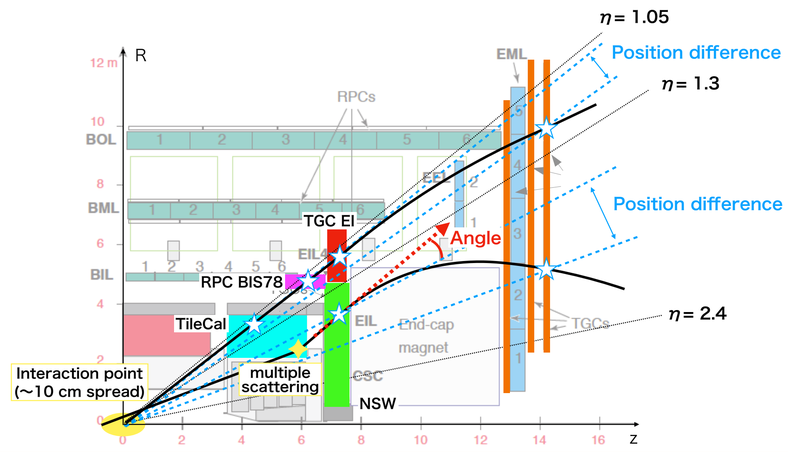


Distributions of polar angle difference ($\Delta\theta$) between track segment reconstructed by pattern matching and track segment reconstructed by ATLAS full offline analysis [2]

- Requirement for hits
  - Run2 : At least two (one) hits in inner three (two) layers and at least three hits in outer four layers for wires (strips)
  - HL-LHC : A looser coincidence with at least five (four) hits in seven (six) layers for wires (strips) to improve efficiency
- Angular resolution of reconstructed track segment evaluated to be **4 mrad** (Total) by a software-based simulation [2]
- p_T pre-determined by angle of reconstructed track segment

Trigger scheme using inner detectors

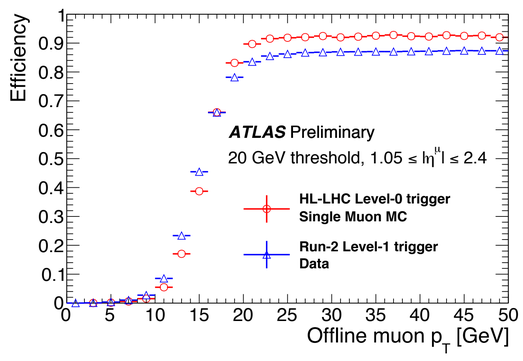
- TGC EI, RPC BIS78 : Two dimensional position measurement
  NSW : Track segment reconstructed with high accuracy
- p_T determined by combination of TGC BW with :
  - TGC EI, RPC BIS78 and TileCal
    - Position difference between TGC BW track segment and hits in TGC EI, RPC BIS78 or TileCal
  - NSW
    - Angle of the tracks reconstructed in NSW
    - Position difference between TGC BW track segment and tracks reconstructed in NSW



Improvement of trigger performance

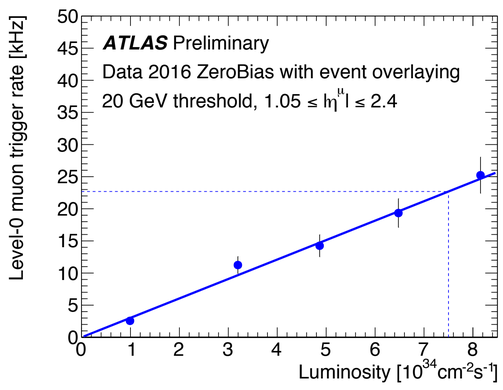
- Performance of level-0 endcap muon trigger (not including more precise p_T measurement in MDT) evaluated by software-based simulation :

- Efficiency [3]



- Higher than **90%** in plateau region thanks to looser coincidence than that in Run 2
- Better rejection for low p_T muons thanks to the good angular resolution

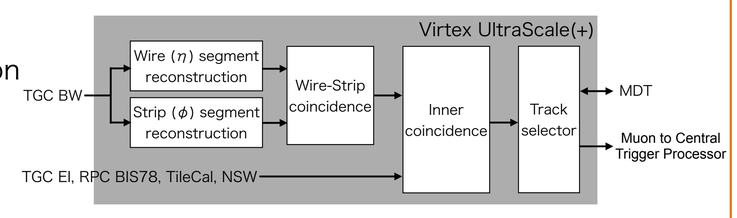
- Trigger rate [3]



- Improved from 60 kHz (in Run 2 configuration) to **23 kHz** for 20 GeV threshold at the luminosity in HL-LHC (7.5×10^{34} $cm^{-2}s^{-1}$)

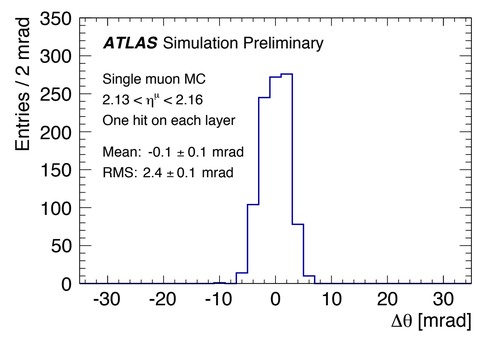
Development of trigger firmware

- Virtex UltraScale(+) FPGA by Xilinx on SL board for implementation of trigger algorithm [2]
- Trigger firmware
  - Wire/Strip segment reconstruction
  - Wire-Strip coincidence
  - Inner coincidence
  - Track selector



- Each part of trigger firmware being developed in parallel.

- TGC wire segment reconstruction for a specific region ($2.13 < |\eta| < 2.16$) implemented on FPGA on an evaluation kit VCU118 and good angular resolution obtained [3]



- Development for whole trigger chain in limited region and expansion to full region ongoing
- Slice test of trigger firmware planned in summer

Reference : [1] The ATLAS Collaboration, Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System, CERN -LHCC-2017-020.
[2] The ATLAS Collaboration, Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer, CERN -LHCC-2017-017.
[3] https://twiki.cern.ch/twiki/bin/view/AtlasPublic/L0MuonTriggerPublicResults