ATLAS Towards the High Luminosity Era: Challenges on Electronic Systems

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On behalf of the ATLAS Collaboration

Physics @ HL-LHC (3-4 ab⁻¹ expected)

- Motivation
  - Precision measurements of Higgs Boson & SM (couplings, top mass/BR)
  - Searches for rare BSM signatures (electroweak SUSY, new resonances, dark matter)
- Difficulties:
  - High pile-up (up to 200 events/BC) & radiation
  - Short time for data processing/transmission (LHC bunch crossing = 25ns)
  - High granularity detector = more channels, larger output data size

High Granularity Timing Detector

- Silicon LGD detector modules located on disks between barrel & endcap calorimeters
- Help identify pile up tracks & maintain electron isolation efficiency in forward region
- Target resolution: 30–50 ps/track up to 4000 fb⁻¹
- Custom large die ASIC ATLRIOC, TMCOS 130nm technology
  - 25 ps jitter at 4IC input change

Inner Tracker

- Entire Inner Detector replaced with all-silicon Inner Tracker (ITk) pixels + strips
  - Key task: read out full calor @ full precision, 16-bit dynamic range @ 40 MHz = data rate of > 250 Tbps to TDAQ system
  - Solution: board next gen readout systems
    - LAr: full custom ASICs = pyramphipper, ADC, ipGBT serializer (200K channels)
    - Tile: new PMTs for pulse + shaped by FENCIS cards + digitized on Mainboard (10k channels)
  - Status: functionalities fully tested, FDR soon
  - Data successfully decoded by L0MDT emulator
  - Test boards ready, sites available early July

Calorimeters

- Tile & LAr readouts replaced for high trigger rates + radiation
  - Key task: transmitting all data of detector for trigger and readout logic processing in custom ATCA blades with powerful FPGAs (SDT IPE and FCATV Sector logic)
  - Solution:
    - New readout for MDT/RPC/TGC: new concentrator boards based on FPGAs that collect data from several FE boards and send it at high speed to the data acquisition system (L0MDT)
    - New MMboards for LAr + TGC
  - Status:
    - MDT: cosmic ray testing, radiation testing of prototypes ASICs for the Inner Detector (R&D & testing)
    - Trigger: FSB design & based testing

Muon System

- Improving trigger chamber performance
  - Key task: streaming all data of detector for trigger and readout logic processing in custom ATCA blade with powerful FPGAs (SDT IPE and FCATV Sector logic)
  - Solution:
    - New FE readout for MDT/RPC/TGC: new concentrator boards based on FPGAs that collect data from several FE boards and send it at high speed to the data acquisition system (L0MDT)
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    - EDET: cosmic ray testing, radiation testing of prototypes ASICs for the Inner Detector (R&D & testing)
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Trigger/Data Acquisition

- Hardware LO → 1 MHz
  - Data from LAr, Tile, RPC, NSI, TGC to Central Trigger Processor (CTP)
- Software/algorithm Event Filter: perform HLT selection in massively parallelized way → 10 kHz
- Key aspects:
  - Extensive use of large FGAs
  - Multi-Gb transceiver links beyond 10 Gb/s
  - Extensive use of ATCA rates/challenging cooling

Dataflow

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Expected muon reco efficiency μp=200