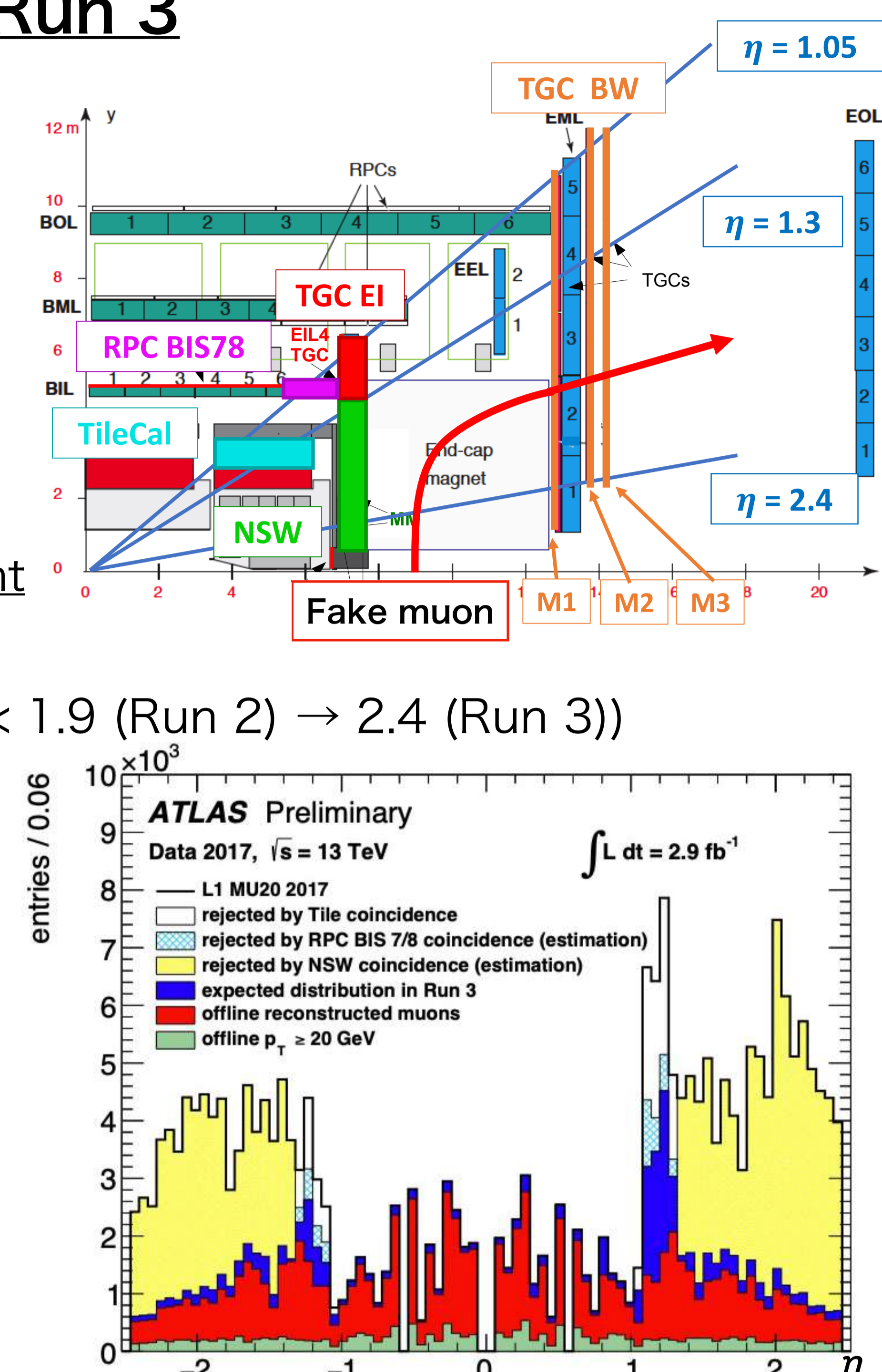


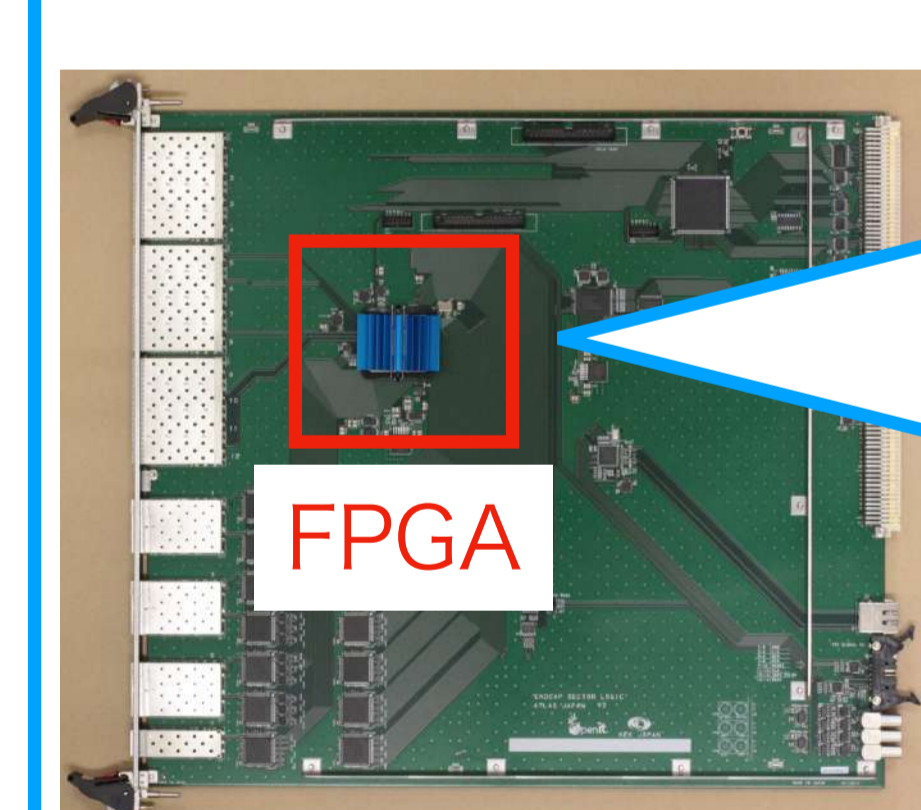
ATLAS Level-1 Endcap Muon Trigger for Run 3

- Detector/Hardware configuration
 - Custom hardware trigger based on **Big Wheel of Thin Gap Chamber (TGC-BW)**
 - Development of new muon detectors and new trigger/readout system hardware
- Identification of muon track candidates with high transverse momentum (p_T)
 - Coincidence with three stations of TGC-BW to estimate p_T
 - ✓ p_T measured in 15 thresholds (previously 6 in Run 2) using predefined look-up tables
 - Coincidence between TGC-BW and inner detectors to reduce contaminations from lower p_T muons below trigger threshold and “fake muons” from out of interaction point
- Inner detectors :
 - New Small Wheel (NSW)** : New detectors with wider coverage for coincidence ($|\eta| < 1.9$ (Run 2) \rightarrow 2.4 (Run 3))
 - Resistive Plate Chamber in Barrel Inner Station (RPC BIS78)** :
Newly installed in transition region between barrel and endcap trigger
 - TGC in Endcap Inner station (TGC-EI)** : existing detectors since Run 2
 - Tile hadronic calorimeters (TileCal)** : existing detectors since Run 2
- Expected performance for triggers with $p_T > 20$ GeV threshold (“MU20”) [1]
 - 90%** reduction of “fake-muon”-oriented events in the endcap region (from Run 2)
 - Effective suppression of triggers by lower p_T muons below trigger threshold
 \rightarrow **~ 45%** rate reduction expected for MU20 (endcap + barrel)
with comparable efficiency in Run 2

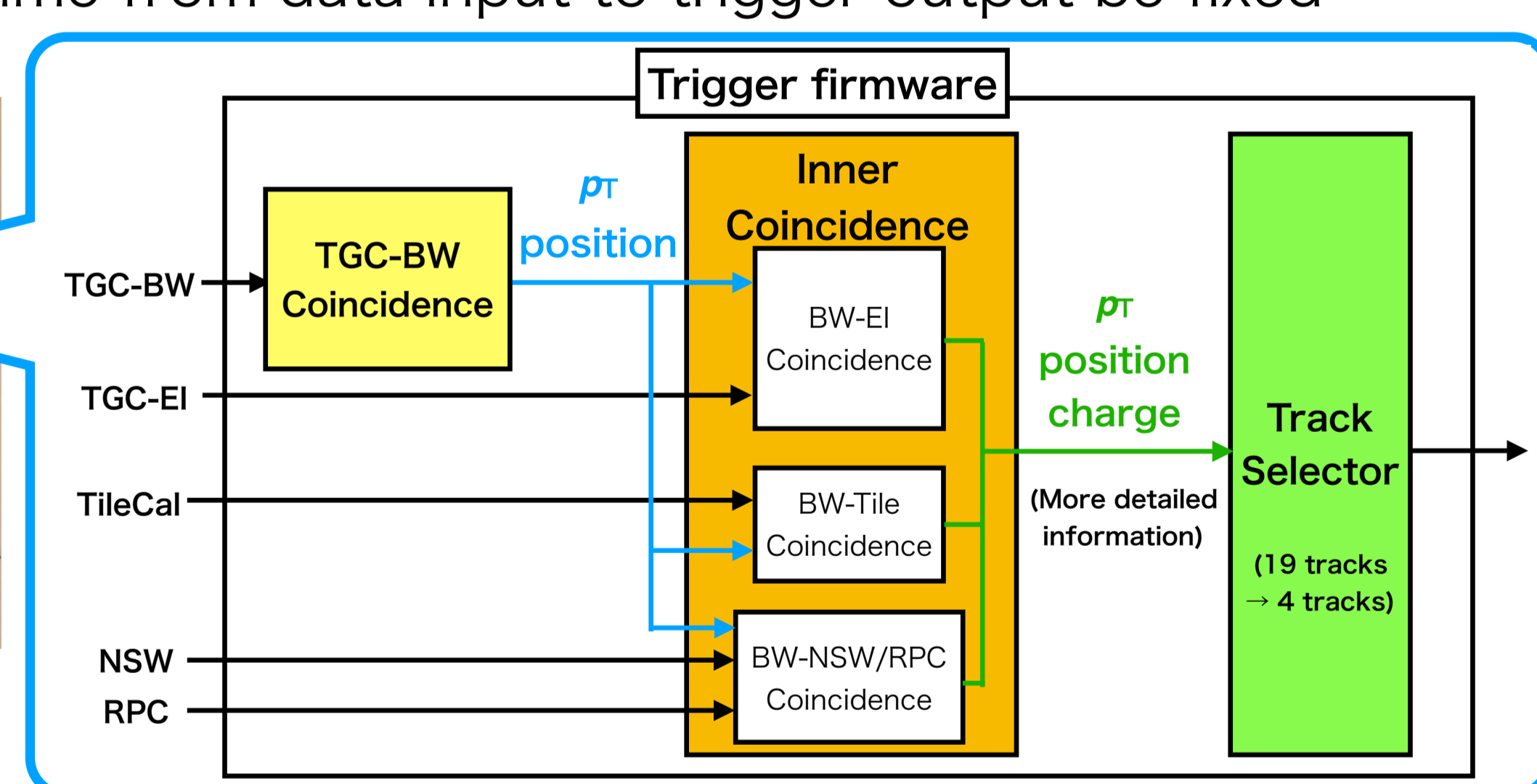


Upgrades in Run 3

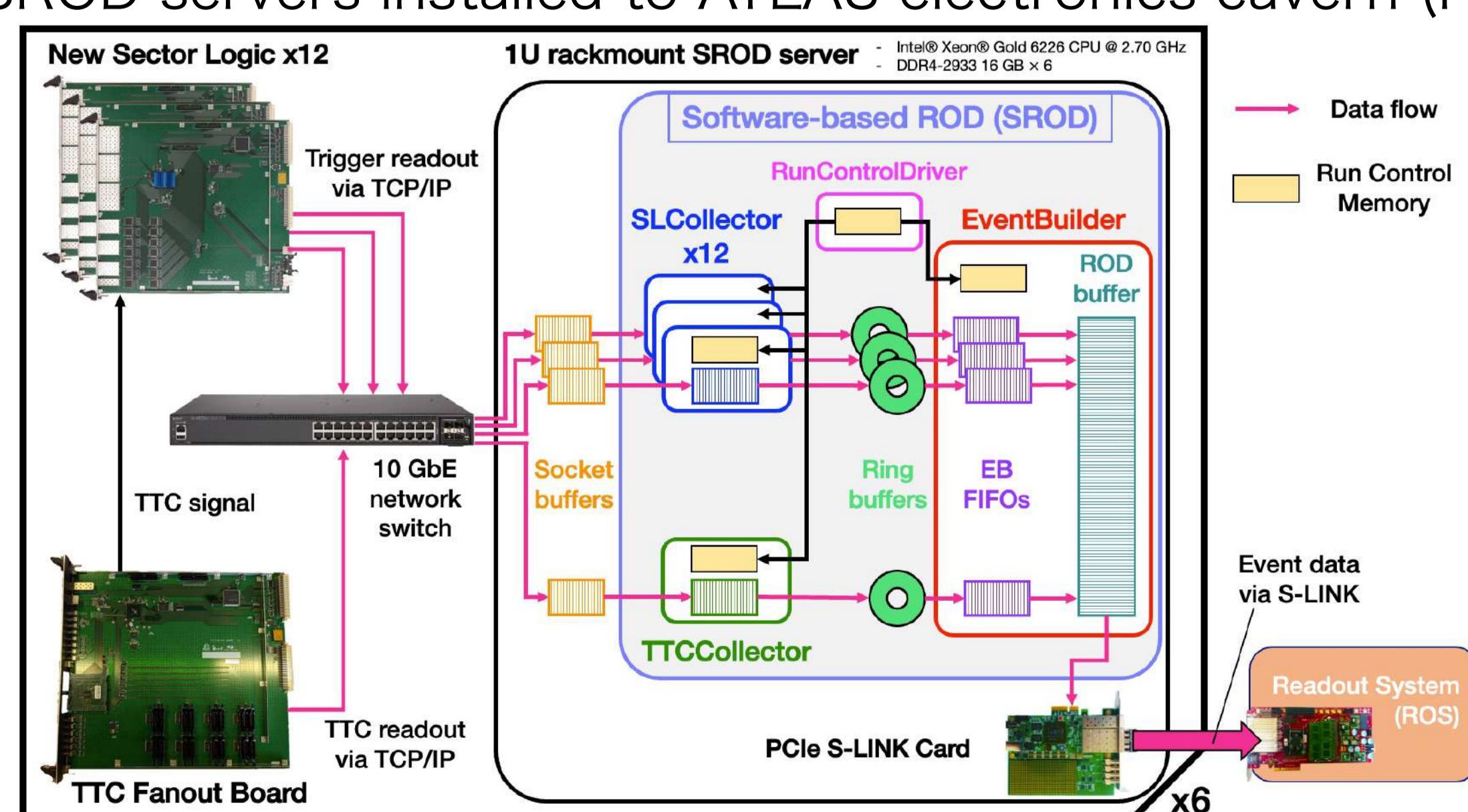
- Trigger System
 - New Sector Logic (New SL)** boards
 - ✓ FPGA with larger resource for main trigger algorithm
 \rightarrow more sophisticated algorithm and higher performance realized
 - ✓ Receivers of data from five types of detectors including new inner detectors (6.4 Gbps/links)
 - Development of trigger firmware implemented in FPGA
 - ✓ Divided into three parts
 - TGC-BW Coincidence, Inner Coincidence and Track Selector
 - ✓ Designed to satisfy “fixed latency” scheme
 - Processing time from data input to trigger output be fixed



New SL board

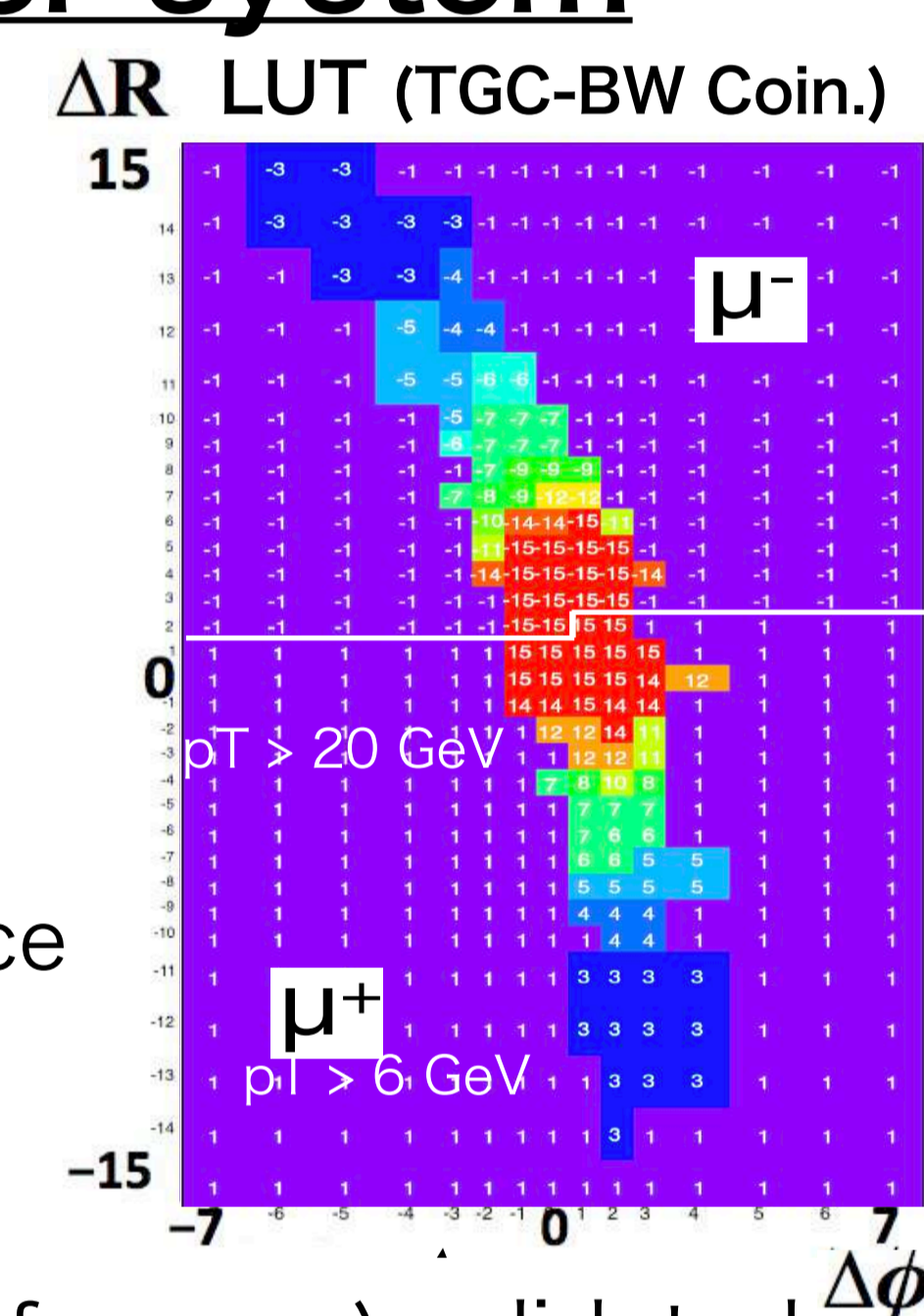


- Readout system
 - Software-based Readout Driver (SROD)** developed to read out trigger data from New SL, which include both inputs and outputs of the trigger logic in New SL
 - ✓ Receiving trigger data via TCP/IP from 12 New SLs
 - ✓ Building events using data
 - ✓ 6 SROD servers installed to ATLAS electronics cavern (Feb 2020)



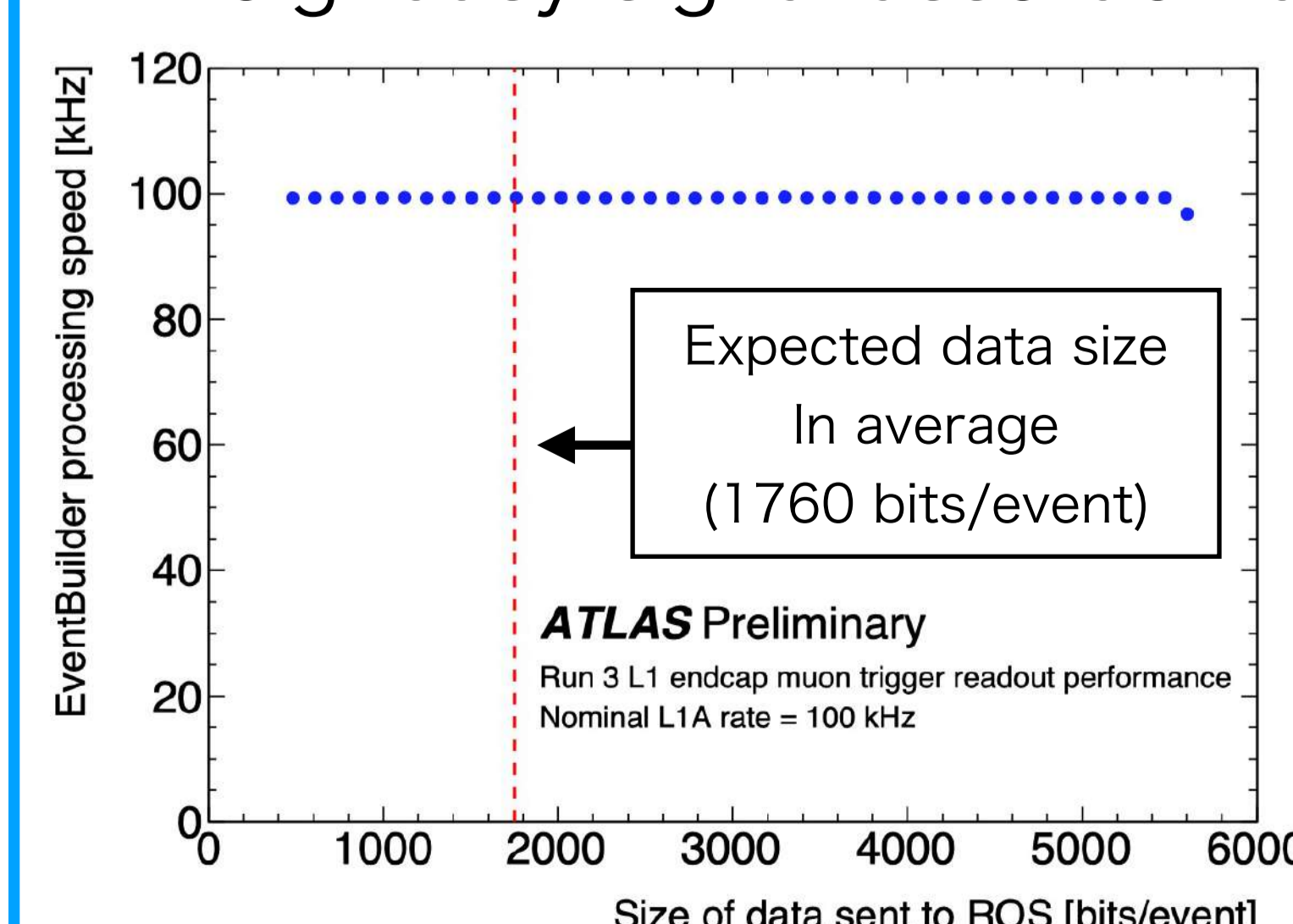
Commissioning of the trigger system

- Setup of trigger logic validation test
 - Various test data from TGC-BW front-end circuit to New SL
 - Look-up table for actual operation
 - ✓ Defined by hit maps generated by simulation
 - ✓ Using difference of hit position (ΔR : $\Delta \phi$) between three stations for TGC-BW Coincidence
- Stable data transfer** between TGC-BW and New SL confirmed
- TGC-BW Coincidence outputs (p_T and position of muons) validated
- Expected latency** for trigger firmware processing confirmed
 - Requirements for Level-1 latency in Run 3 satisfied
- Next step
 - Validation of Inner Coincidence mainly between TGC-BW and NSW

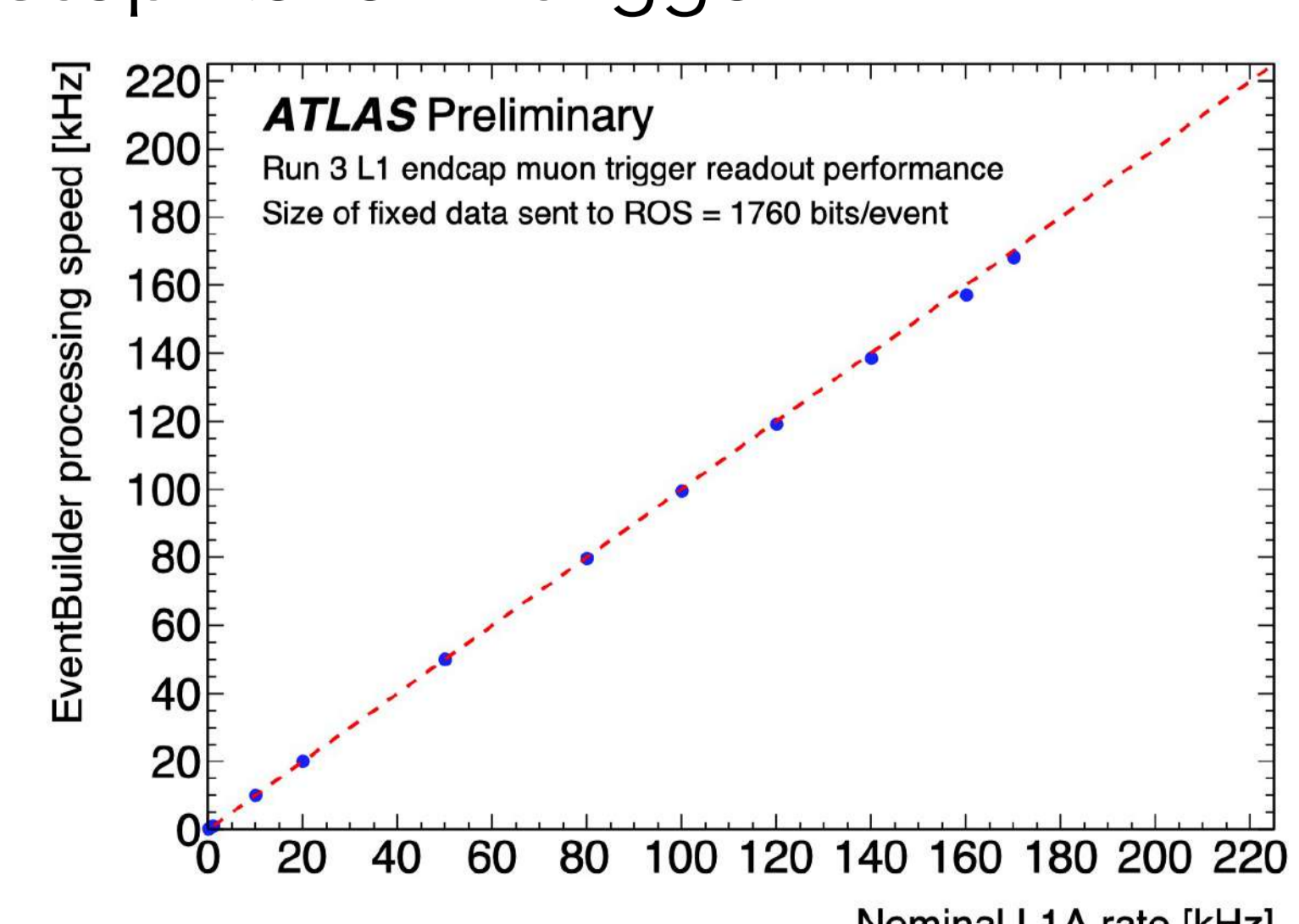


Performance of the readout system

- Setup of performance evaluation tests
 - Fixed data sent from 12 New SLs to 1 SROD
 - Processing speed measured for SROD EventBuilder application which determines whole trigger readout performance.
- Sufficient performance achieved** for stable operation at Run 3 in terms of event data size and trigger rate
- Handshake with Central Trigger Processor established
 - e.g. busy signal assertion to stop Level-1 trigger



Varied data size with average trigger rate fixed to 100 kHz [2]



Varied average trigger rate with data size fixed to 1760 bits/event [2]