CALICE SiW eCAL Compact Digital Readout Electronics

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On behalf of the groups working on the SiW ECAL within CALICE

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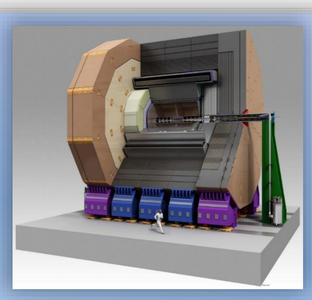
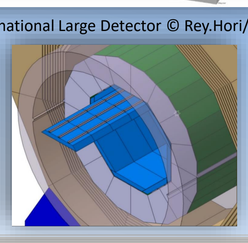
Summary

Ultra compact electronics are required in particular for calorimeters at future e+e- colliders. Their development is conducted within the **CALICE** Collaboration and an application is the **Silicon Tungsten Electromagnetic Calorimeter** (SiW Ecal) of the ILD Detector. The SiW Ecal is based on highly integrated slices of active layers (slabs) using many **ASU** boards (Active Sensor Units) housing the front-end ASICs (**SKIROC** from **OMEGA** group). The digital electronics which controls the system and performs the readout of physics data is situated at the extremity of the detector slabs with very stringent requirements on **space and power**.

The paper will present this digital electronics interface, the **"SL-BOARD"**, which has been designed together with a **kapton-based interconnection and readout (CORE)** system in order to fit these requirements.



International Large Detector © Rey.Hori/KEK



The International Linear Collider/ Detector

The **International Linear Collider (ILC)** is a particle accelerator that will collide electrons and positions at energies between **91.2 GeV** (Z-Pole) - **1 TeV**.

The **International Linear Detector (ILD)** is a detector for the ILC that combines excellent **tracking** and **finely-grained calorimetry** systems which permits precisely reconstructing the energy of individual particles, known as **Particle Flow Approach**.

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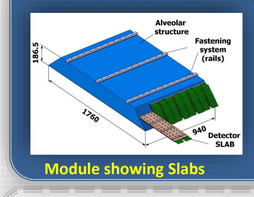
The SiW Ecal structure

The SiW Ecal structure of ILD will consist of about 2400 m² of **Silicon Sensors** with a total weight of **~ 130 t**

The Ecal Modules are made of **alveoli columns** where the **slabs** containing the sensitive layers are slid.

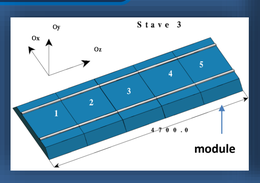
The slabs have a **Tungsten** core wrapped into Carbon Fiber. The Silicon sensors are located on both sides of the core. The PCBs housing the **Front End electronics** (**SKIROC** Asics) are glued to the silicon layers.

The total number of channels of the Ecal will be of the order of **10^8**

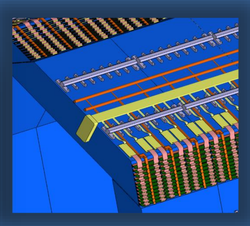


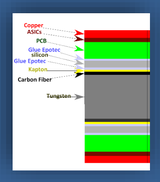
Module showing Slabs

- **1 ASU** (18 x 18 cm) = 16 Skirocs = **1024 channels**
- **1 slab** = up to 15 interconnected ASUs

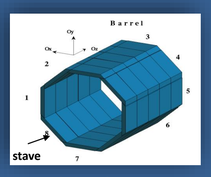


Barrel stave made of 5 modules



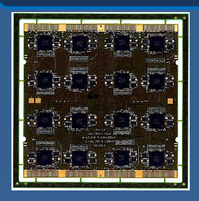


Layers in a slab



Barrel showing staves

Constraints on Readout Electronics

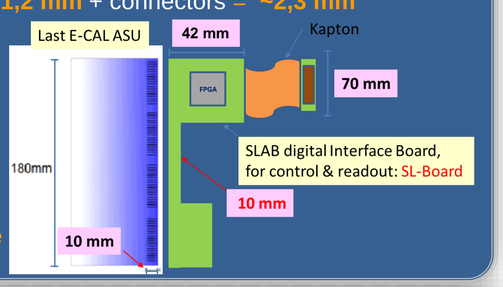


Spatial constraints for the Active Sensor Units (ASUs)

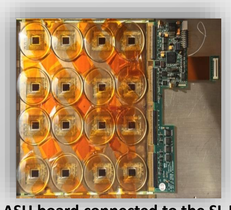
- There is very limited space **for each layer** **(depending on the total number of layers)**. Two protoype versions have been realized with different SKIROC packaging and thickness:
  - ✓ BGA option : PCB + components*(1,2 mm)* + connectors = **~ 3,2 mm**
  - ✓ COB (Chip On Board) option : PCB and ASICs **= 1,2 mm** + connectors = **~2,3 mm**

Constraints for the Slab Interface Board (SL-Board)

- The SI-board will be installed between ECAL and HCAL, separated by only 67 mm
- C-shape because of the cooling system
- Maximum Height : **6 to 12 mm depending on the location**
- Control & Readout electronics at the extremity of the Slab
- Signal Integrity over a Slab : up to 15 interconnected ASUs
- Very low Power consumption (< 100 mA/ Slab) : needs to run in **power pulsing mode**



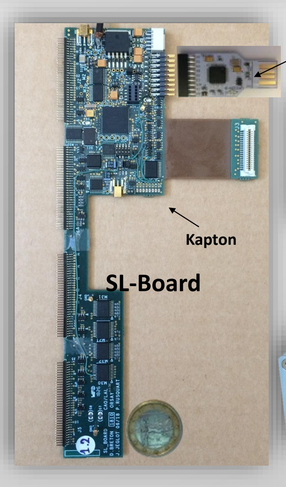
The SL-BOARD

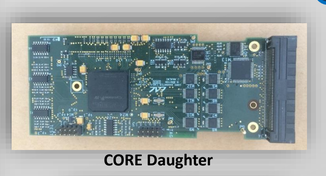


The ASU board connected to the SL Board

- Each ASU houses 16 SKIROC Asics: **1024 channels** in total.
- The SKIROC chip handles 64 channels with **15-slot analog memory**. It is self-triggering on the channels during a given acquisition window (~1 ms) and gives the **converted charge and time.**

- The **SL-Board** is the sole interface for the **~10,000 channels of a slab**
- It delivers the **regulated power supplies,** including **High Voltage**, **controls** the SKIROC ASICs, and **performs the full data readout**.
- It is connected to the CORE-Kapton via an internal **kapton layer** and a 40-pin connector.
- It is based on a **MAX10 from ALTERA**, which is a mix of CPLD and FPGA, and also includes an ADC which will be used to monitor the pulsed power supply.
- Its **size is very limited** because of its location (18 cm in width, 10 to 42 mm in length), and its own power consumption should be as low as possible **(< 1W)**.
- It can also be an **autonomous system** with direct computer access for testing and characterization purposes (using the **FTDI USB module**).





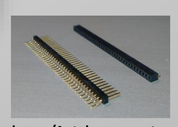
CORE Daughter

CORE Module

The CORE Module

CORE Daughter

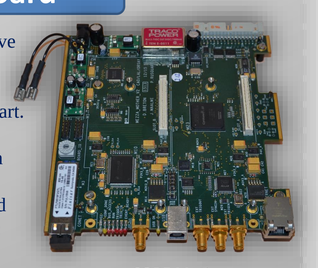
- The **CORE Daughter** is based on a Cyclone IV FPGA. It is the interface between the CORE motherboard and the Kapton which permits driving and reading out **up to 15 slabs**.
- It buffers all the clocks and fast signals, and deals with the control and readout links through the Kapton Interface.
- It houses the second level of **event buffers** (derandomizers)**.**



Gradconn /Antalec connectors (1.5 mm high)

CORE MotherBoard

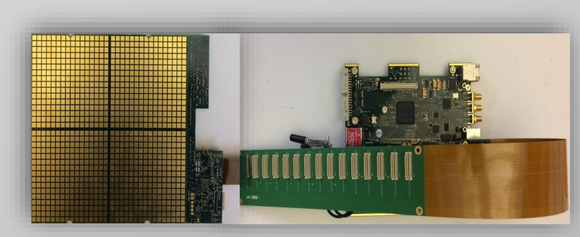
- The **Control and Readout Motherboard** have been developed for housing up to 2 **Mezzanines**: it permits separating the **acquisition** part from the specific front end part.
- **External** input and output signals permit **synchronising** or interfacing the module with other systems.
- The CORE mother sends common clocks and fast signals to the Core Daughters to keep the **system synchronised**
- The control and readout is possible through **USB(2.0)**, **UDP or Optical link** (Ethernet over optical



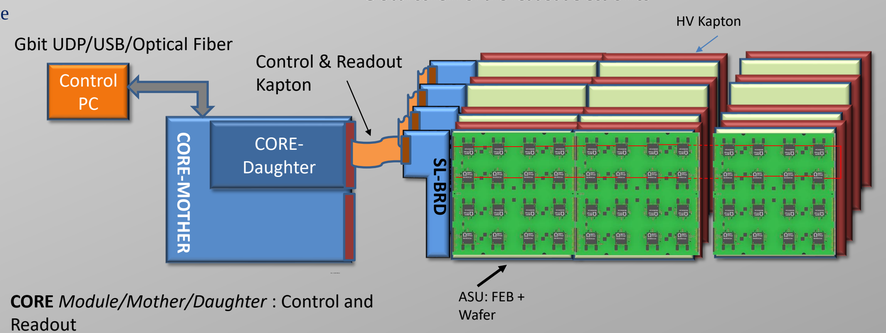
CORE Mother

The SL-Board/CORE link (CORE Kapton)

- The **CORE kapton** measures 40 cm. It is the **interface** between the CORE Daughter and the SL-Board. It permits driving and reading out **up to 15 slabs**.
- It transmits all the clocks and fast signals, and houses the control and readout links.
- It handles the **synchronisation** of the **15 slabs**.
- The Kapton Interface makes use of **asynchronous serial transmissions** in order to greatly simplify the synchronization of the numerous control and data links.



Global schem of the readout electronics

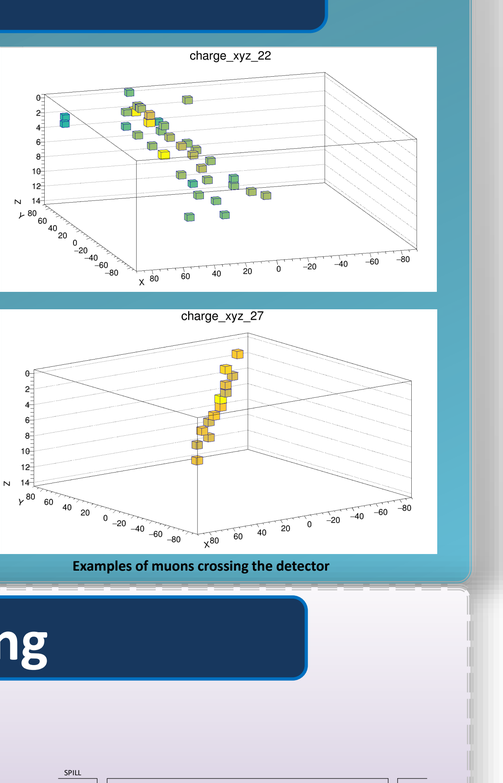


CORE *Module/Mother/Daughter* : Control and Readout
SL-BOARD : Interface board to Slab

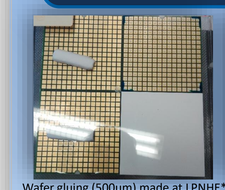
- Skiroc chips are chained for slow control and readout

Control & Readout Software

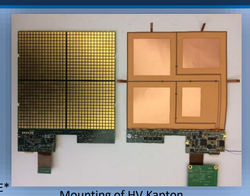
- The acquisition Software can handle the communication through a the FTDI Module directly to the SL-Board **or** through the **CORE Module**.
- It handles the control and readout of a **whole detector module**:
  - **Two sides with 15 SLABs each.**
  - **Each slab with up to 5 ASUs.**
- It is written in **C** and developed under **Labwindows CVI**
- The **C-functions** that handle the communication (readout and configuration) can be used as a library with any other programs in any language that can be linked to the C-library.
- Advanced measurements can be performed Online such as threshold scan, temperature and AVDD monitoring, rates per Channel/ASIC/slab….



1st Test Beam (July 2019)

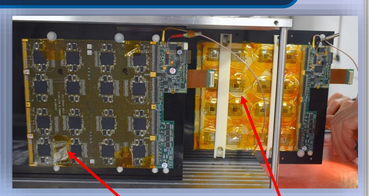


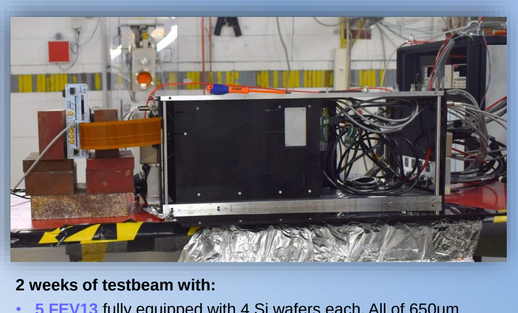
Wafer gluing (500um) made at LPNHE*



Mounting of HV Kapton

SL-board + ASU on support

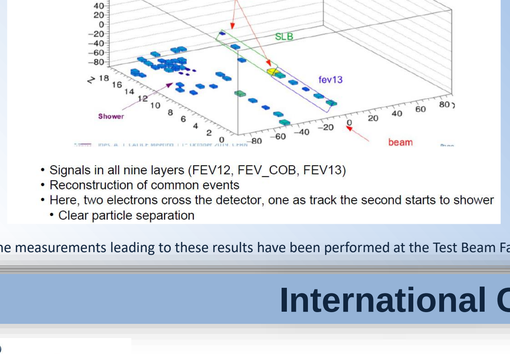




2 weeks of testbeam with:

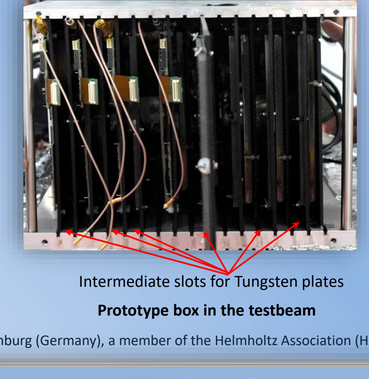
- **5 FEV13** fully equipped with 4 Si wafers each. All of 650um except one slab with 320um. Interface card SMBv5 with the old Detector Interface Card.
- **2 COB** boards with one wafer each (500um) readout with **SL-Board**
- **2 FEV12** boards with one wafer each (500um) readout with the **SL-Board**
- Data taking w/ and w/o tungsten
- Individual runs, then common runs with the 9 Layers.

Reconstructed event with particle seperation



- Signals in all nine layers (FEV12, FEV_COB, FEV13)
- Reconstruction of common events
- Here, two electrons cross the detector, one as track the second starts to shower
- Clear particle separation

Mechanical Design of the prototype box*
**Designed by Alexandre Gallas and Alice Thiebault, (LAL Orsay)*

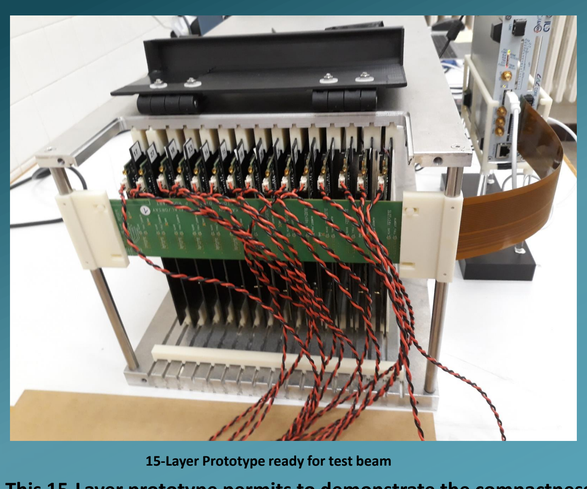


Intermediate slots for Tungsten plates

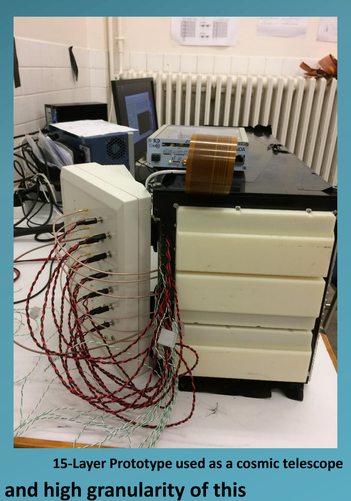
Prototype box in the testbeam

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

15-Layer Prototype



15-Layer Prototype ready for test beam

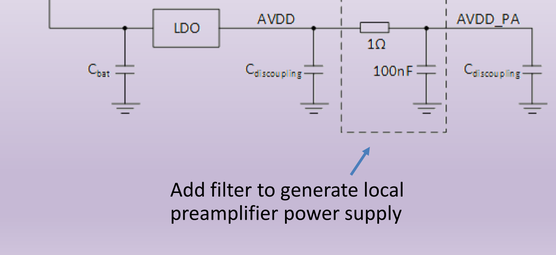


15-Layer Prototype used as a cosmic telescope

This 15-Layer prototype permits to demonstrate the compactness and high granularity of this calorimeter: It contains 15,000 channels within a volume of 18x18x25 cm3.

Examples of muons crossing the detector

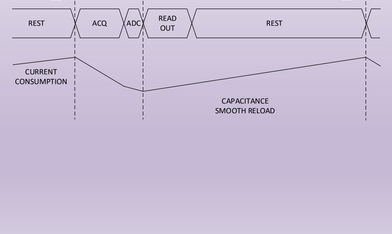
Long Slab & Power-Pulsing



Add filter to generate local preamplifier power supply

In order to avoid important voltage drop along the slab and the potential effects of strong magnetic field (both due to the **propagation of high current calls towards the external power supplies),** we decided, in the new design of the Front-End Board (collaboration with LLR), to :

- **Stricly limit the current** through the slab.
- Add **large capacitors with low ESR** for local **energy storage** (around each SKIROC chip)
- Generate local power supply with **LDO** (Low Drop Out) to avoid **voltage variations**



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