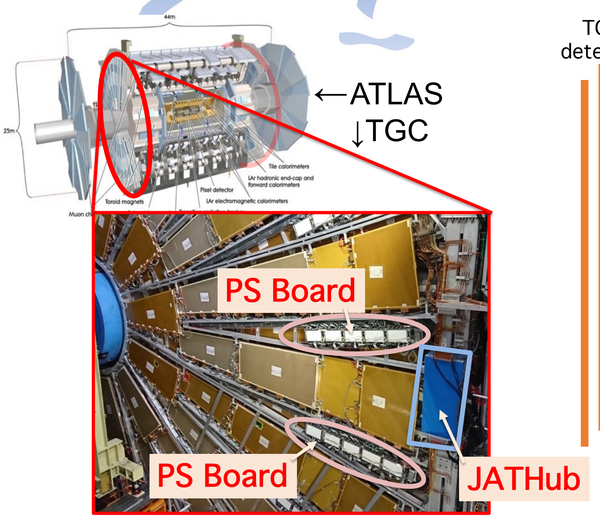
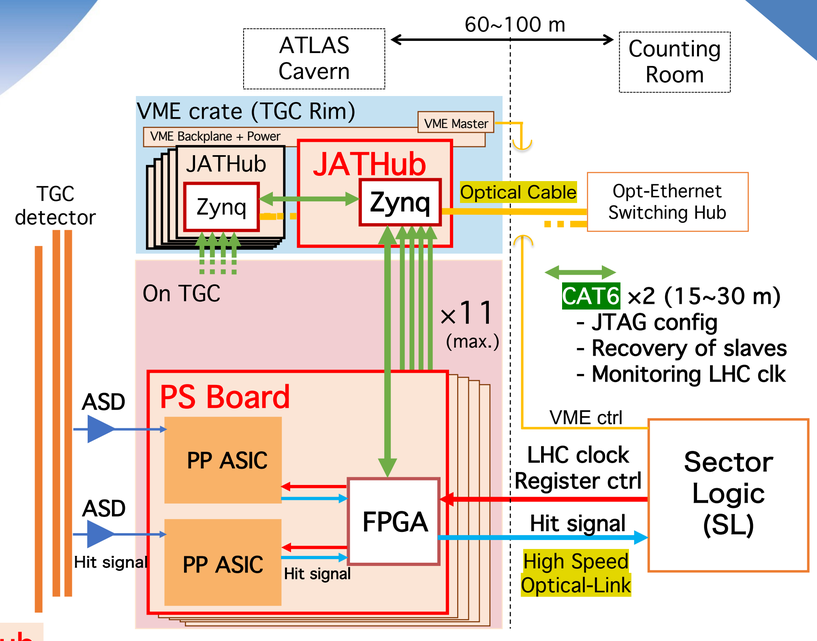
System-level performance study and commissioning of TGC front-end electronics for Phase-2 upgrade of ATLAS-LHC

#470

TIPP 2021 Poster session, virtual conference, 24-28 May





[1] Technical Design Report of HL-LHC ATLAS [Link]

TGC Electronics System for Phase-2 upgrade

The Large Hadron Collider at CERN (LHC) will be upgraded to deliver a peak instantaneous luminosity up to 7.5 $\times 10^{34}$ cm^{-2} s^{-1} , corresponding to the pile-up of 200 inelastic proton-proton collisions per bunch crossing at 40 MHz. The operation will start in 2027. In order to cope with the high luminosity environment and to collect collision data for searching for physics of interest, the ATLAS experiment will upgrade the readout/trigger electronics of the Thin Gap Chamber (TGC) detector (Phase-2 upgrade [1]).

TGC system is responsible for the endcap muon trigger of the ATLAS. The TGC electronics system consists of ASD [~20K boards], Processing Board (PS Board) [1434 boards], JTAG Assistance Hub (JATHub) [148 boards] in the ATLAS cavern, and Sector Logic (SL) [48 boards] in the ATLAS counting room. This system covers ~320K ch. of the TGC detector.
[Readout/trigger] When a charged particle is detected by the TGC detector, the ASD amplifies and sends the hit signals to the PS Board. The PS Board sends ALL hit signals to the SL with high speed optical-link. Then the SL performs all the trigger calculation. In order not to restrict data transition, the TGC system exploits modern FPGA. This simplified system can be an optimal solution for the trigger logic.
[Control・Config/Monitor] LHC clock at 40 MHz is distributed to all LHC electronics system for DAQ. In the TGC system, the SL distributes the LHC clock to the PS Boards via FPGAs. In terms of the control of front-end electronics, the SL controls registers of the PS Boards via FPGAs. The JATHub takes a role in configuring FPGA, in recovering functionality of the PS Board, and in monitoring the distributed LHC clock on the PS Board.

Development of PP ASIC and PS Board

◆ Design and Function of the PS Board

The PS Board has 8 PP ASICs (4 on mother board, 4 on mezzanine board) and 1 FPGA (Kintex-7 by Xilinx).

The PP ASIC receives hit signals from the ASD and delays signals to absorb the signal-timing difference caused by the Time-Of-Flight and the length of cable between the ASD and the PP ASIC. The PP ASIC performs bunch crossing assignment with configurable gate width. The step size is <1 ns. The PP ASIC generates test pulse to the ASD to test readout access and timing calibration.

The FPGA receives all hit signals from the PP ASICs and transfers ALL of them to the SL by optical-link without any treatment. The FPGA controls and monitors the thresholds of the discriminator of the ASD. The FPGA receives the 40 MHz LHC clock from the SL by optical-link with fixed latency. This LHC clock is sent to the clock jitter cleaner and is supplied to the FPGA and the PP ASICs as system clock.

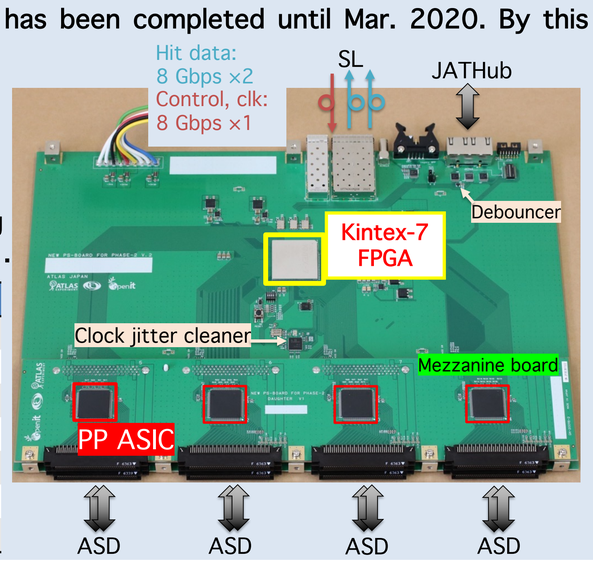
◆ PP ASIC QA/QC

An automated quality test system for QA/QC is developed. It takes 1~2 min for ONE chip. All functions of the PP ASIC, all I/O pins, and the power consumption are tested in this system.
The PP ASIC production of 25,000 chips has been completed until Mar. 2020. By this test system, >20,000 chips are confirmed to be as of Apr. 2021 (~90% yield).
Completion of the quality test of all chips is expected in Jun. 2021.

◆ Testing of PS Board prototype

All the testing of the prototype are going well and expected to be done in Jun. 2021.

PS Board Testing	Status
FPGA configuration	Clear
SL interface	Clear
JATHub interface	Clear
Clock jitter cleaner configuration	Clear
PP ASIC configuration	On going
Signal path access from/to ASD	On going
ASD threshold control	Clear



Development of JATHub

◆ Design of the JATHub

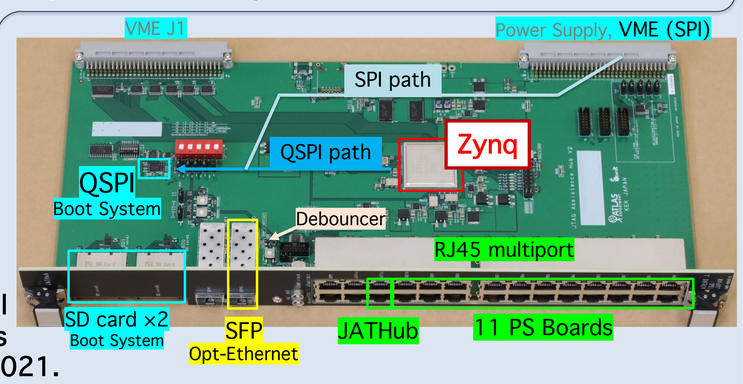
The JATHub is a control hub module for the FPGAs on PS Boards. The JATHub is equipped with Zynq-7000 System-on-a-Chip (SoC) device of Xilinx as the main driver. A Zynq SoC integrates an ARM-based processor with Kintex-7 FPGA.
The JATHub will be installed into the VME crate at the rim of TGC; 6 JATHubs in 1 crate. The JATHub connects to max. of 11 PS Boards with 2 Category-6 (CAT6) cables for each.

◆ Function of the JATHub

In order to access Linux OS running on the Zynq from outside, the JATHub establishes ethernet (1000 Base-X) connection with the counting room, connecting the Zynq and the switching hub with optical fibers. Once the JATHub is accessible from outside, control, monitoring, and debugging of the remote PS Boards in the cavern are easily curried out.
- Configuration and debugging of the FPGAs of PS Boards is performed by JTAG access.
- The JATHub monitors the system clock of the PS Boards (LHC clock).

The JATHub also takes a role in recovering the functionality of slave modules (PS Boards, neighbouring JATHub). Usually, the slave FPGAs recovers Single Even Upset (SEU) error automatically by the dedicated firmware (~0.1 SEU s^{-1}) in the LHC run time. But, when unrecoverable SEU error is occurred on a slave FPGA, the JATHub receives the SOS signal from the slave and sends back the long reset signal (>10 ms). This reset signal triggers the reconfiguration of the slave FPGA. In order not to be affected by the crash of CPU part of Zynq, the JATHub only uses the FPGA part of Zynq, which works independently, for this recovery procedure. Against the radiation damage on the FPGA, voting logic is implemented at various places of the recovery path.

In order to operate in the high luminosity environment, the JATHub needs redundant boot system against radiation damage. The JATHub has 2 SD cards and 1 QSPI flash memory to store several BOOT files. The Zynq can automatically choose the valid (not damaged) BOOT file, and the Zynq can reboot without issue even in the LHC run time. QSPI flash needs to be reprogramed on any occasion, even when the Zynq cannot access the flash due to the Zynq's crash. The QSPI flash memory of the JATHub is also accessible directly from VME path in the SPI protocol by bit-banging.



◆ Testing of JATHub prototype

Most of the testing of the prototype are successful and only the test of the redundant boot system is on going. The test is expected to be done in Jun. 2021.

Combined Test and System-level Study

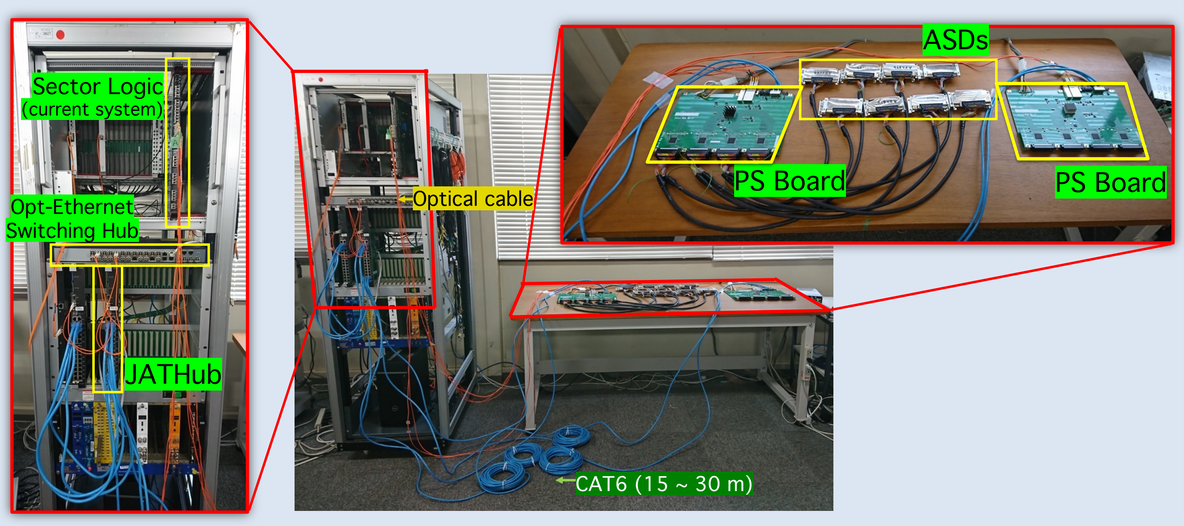
A testbench is built at KEK (Japan) with the ASD, the PS Board prototype, the JATHub prototype, and a SL of the current TGC system. A combined test of Phase-2 TGC front-end electronics is on going at the testbench.

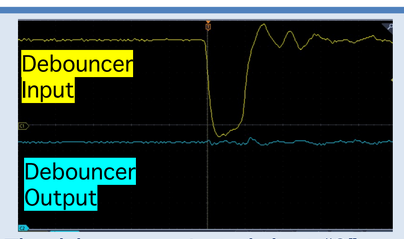
◆ Goals of the combined test

(0) [Done] Develop the data format and protocol between the PS Board and the SL
[Done] Demonstrate the register control in the PP ASICs, the FPGAs
(1) [Done] Demonstrate the JATHub control with the infrastructure close to the cavern
(2) [Done] Demonstrate readout chain using the ASD test pulse functionality
(3) [Done] Demonstrate clock distribution, measurement, and adjustment

◆ Future prospects

- Integration of Phase-2 SL prototype into the testbench is expected after autumn of 2021.
- This testbench will be used as the commissioning system of the Phase-2 TGC electronics, when production-models are installed into the ATLAS cavern.





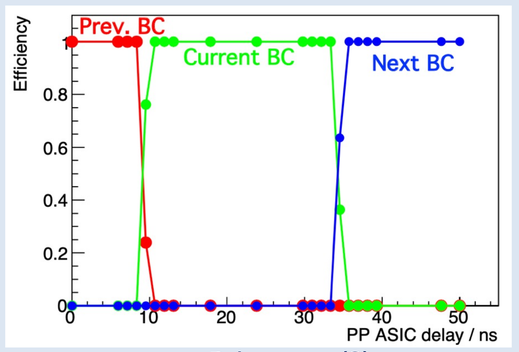
The debouncer rejected short "0" reset signal (1)

◆ (1) Demonstration of the JATHub control

- JTAG access with long CAT6 (15 ~ 30 m) is achieved. The optimized JTAG frequency is 1.25 MHz.
- Reset signal is handled properly in the recovery procedure; unwanted short reset signals (~1 μs) to the slave was rejected by a debouncer.

◆ (2) Demonstration of readout chain

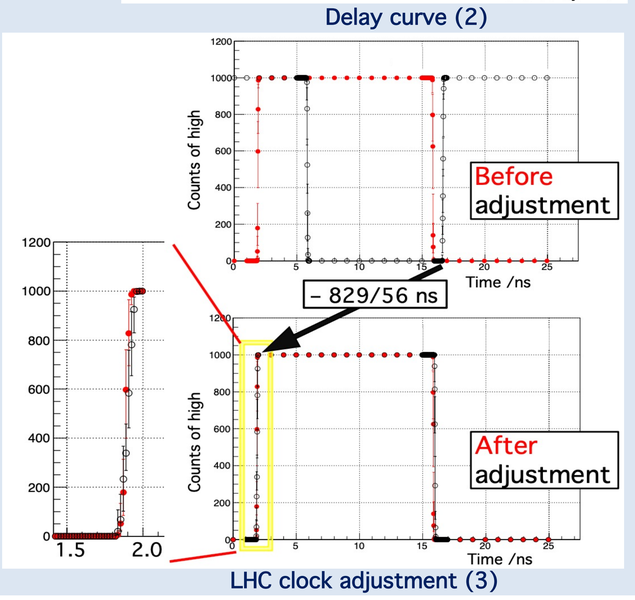
I, The SL controlled the variable signal delay of a PP ASIC one by one and checked the delay by reading the test pulse from the ASD. As the result, perfect Delay Curve was created. Besides, fixed latency between the SL and the PS Board is achieved.
II, The SL read all hits for a test pulse injection successfully.



Delay curve (2)

◆ (3) Demonstration of the LHC clock adjustment

The phase of the LHC clocks on all PS Board needs to be matched in accuracy of <1 ns. However, because of the different fiber length between the PS Boards and the SLs, adjustment of the LHC clock on the PS Board is required.
I, It's succeeded to realize the way to monitor the LHC clocks on the PS Boards in accuracy of 1/56 ns by the JATHub.
II, Phase difference between the clock on the SL and the distributed clock on the PS Board was measured by the JATHub. With 10 times reconfiguration of the FPGA on the PS Board, Max. of 20 ps variation was observed. Thus, fixed latency of clock distribution is achieved with good accuracy.
III, The clock phase of two PS Boards was measured by the JATHub. According to the monitoring result, the parameter of the PS Board was adjusted by the SL to shift one of the clocks by – 829/56 ns. Therefore, the phase matching with sufficient accuracy was achieved.



LHC clock adjustment (3)

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