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System-level performance study and commissioning of TGC frontend electronics for Phase-2 upgrade of LHC-ATLAS

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The Thin Gap Chambers (TGCs) of the LHC-ATLAS are responsible for triggering muons in the endcap region at the hardware trigger stage. The frontend system of TGC will be upgraded for HL-LHC to send binary hit-map at every bunch crossing (BC) to the backend system. Such an operation requires lots of unique challenges: high-performance hit BC Identification, fine-tuned clock distribution, robustness for SEU, and the capability of timing calibration. Accommodating these requirements, the primary processor board (PS-Board) is in charge of data processing and reception of control signals distributed by the backend. An independent control module (JATHub) will take responsibility for FPGA configuration and clock phase monitoring of the PS-Boards with an SoC-based design. Prototyping and initial system-level demonstration with the prototypes have been successfully performed. Exploiting the experience, we are developing the final design and the in-depth strategy for the commissioning.

TIPP2020 abstract resubmission?

No, this is an entirely new submission.

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