THE HL-LHC UPGRADE OF THE ATLAS HADRONIC TILE CALORIMETER

Abstract

The High-Luminosity phase of LHC, scheduled to begin in late 2027, will deliver five times the LHC nominal instantaneous luminosity to the experiments. To ensure sound performance under the higher pile-up and radiation conditions, the ATLAS hadronic Tile Calorimeter (TileCal) will replace both the on- and off-detector electronics systems during the LHC long shutdown 3 (2025-2027).

The upgraded front-end system will continuously digitize and read out shaped photomultipler tube (PMT) signals from every TileCal cell at a rate of 40 MHz, transmitting them over high-speed fiber links to the new back-end electronics to be stored in latency pipelines and digitally summed to produce improved trigger tower data for the Level-1 trigger. The front-end electronics are based on radiation-qualified commercial components, and use extensive redundancy to minimize single point failures.

The Tile upgrade program has undergone extensive R&D and beam tests, and a "demonstrator" module was installed on ATLAS in 2019 for integration and testing in the actual detector environment.

System Overview

A schematic overview of the upgraded readout path is shown in Figure 1. Light from the scintillating plastic tiles is transported to PMT blocks inside the back beams of the wedge-shaped calorimeter modules.

Front-end cards ("all-in-one") in each PMT block shape the signal pulses, amplify them with two gains, and send them to a Main Board (MB for digitization at 40 MHz.

The digitized samples for both gains are continuously read out to a control and link Daughter board (DB), which formats and transmits them over 9.6 Gb/s optical links to the off-detector Pre-Processor (TilePPr) system.

The TilePPr stores the data in latency pipeline memories awaiting readout, while in parallel producing digital hadronic tower sums at 40 MHz for the ATLAS calorimeter hardware trigger.

The TilePPr also sends 4.8 Gb/s optical links to GBTx ASICs on the DBs for timing and control of the on-detector electronics, including calibration using integrators and charge injection (CIS) circuits in the front-end cards.

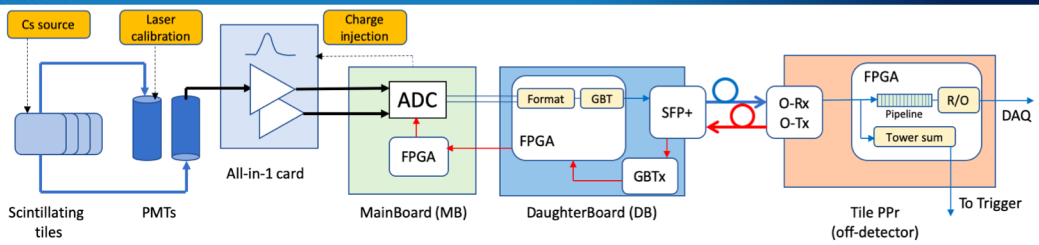


Figure 1: Schematic overview of the upgraded TileCal electronics data path.

Redundant design

The upgraded on-detector system architecture makes extensive use of redundancy to ensure high reliability. In the new design, each calorimeter module has been subdivided into four independent modules called mini-drawers (MD) each with one MB, one DB and up to 12 PMTs.

Each calorimeter cell is read out on two sides to separate PMTs; to avoid loss of both sides due to a single point of failure, the MB and DB are divided into independently powered sides (Figure 2), each serving one side of the module.

The DB design allows both sides to continue receiving timing and commands from the PPr if one of the two input links are lost, and each DB side has two redundant output links to the PPr, providing additional fault tolerance.

Radiation tolerance

With the exception of the CERN-developed GBTx ASICs, the on-detector electronics are built from commercial components that must be radiation qualified for the higher radiation doses expected at HL-LHC. This includes the large FPGAs that provide the digital functionality of the MB and DB, which can be disrupted by single event effects from hadrons. Altera/Intel Cyclone IV (MB) and Xilinx Kintex Ultrascale (DB) devices have been successfully tested for ionizing does, displacement damage and single-event effects.

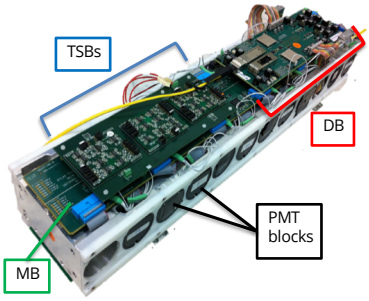


Figure 3: A Demonstrator mini-drawer (MD). Analog outputs from "all-in-1" boards in the PMT blocks are digitized by ADCs on the Main Board (MB) and read out to the Daughter Board (DB) for fiber-optic transmission to the PPr. The Demonstrator is additionally equipped with trigger summing boards (TSB) that produce analog tower sums for compatibility with the legacy ATLAS trigger.

Demonstrator system

A "Demonstrator" system has been built for testing the upgraded system in actual ATLAS conditions. It comprises four MDs, each with a prototype MB and DB, and up to 12 PMT blocks. (Fig. 3).

For compatibility with the existing ATLAS L1 trigger, the front-end boards have extra analog outputs that are summed into trigger towers by analog trigger-summation boards.

The Demonstrator was developed and tested in five test beam campaigns at SPS from 2015-2018. It was then inserted in ATLAS in June 2019 and successfully integrated with the full system including full-detector calibration runs and long-term stability tests.

The Demonstrator has shown stable performance, comparable laser and CIS calibration performance, and lower pedestal noise (Figure 4). Ongoing tests, including environment monitoring and trigger integration, will continue to provide valuable experience for future installation at HL-LHC.

References

1. ATLAS collaboration: Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter CERN-LHCC-2017-019, ATLAS-TDR-028, 2018]

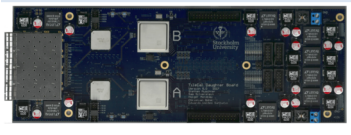
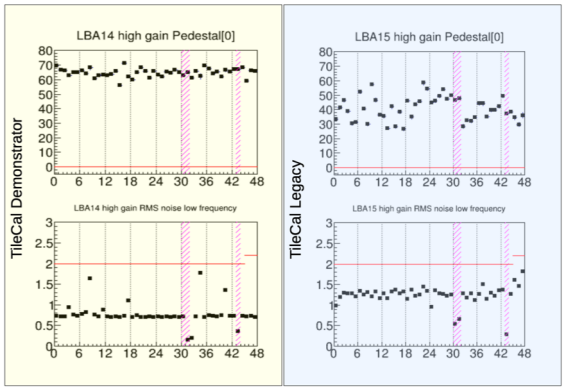


Figure 2: A Daughter board (left) and a Main board (below), both divided longitudinally into independently powered and operating sides.

Figure 4: Pedestal noise in the Demonstrator vs. legacy readout. The lower RMS is due in part to the smaller LSB of the MB ADCs.



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