Electronics Performance of the ATLAS New Small Wheel Micromegas wedges at CERN

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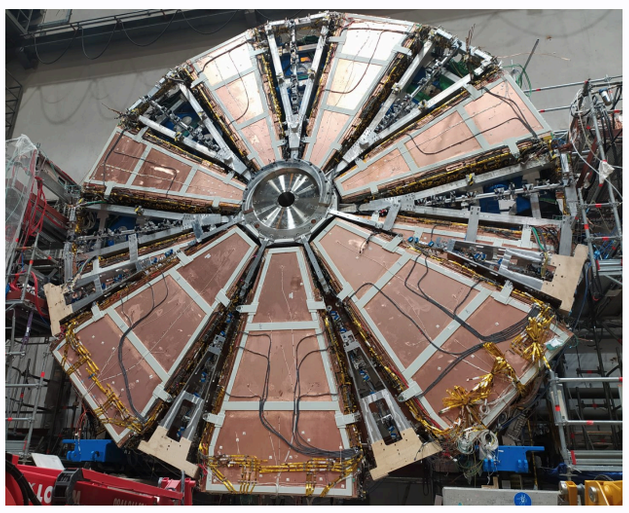
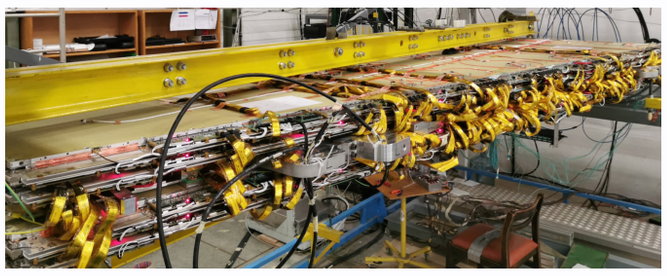
ATLAS NEW SMALL WHEEL - MICROMEGAS Detector

The New Small Wheel (NSW) Upgrade, the most challenging and complex one of the ATLAS Phase-I upgrade projects is currently in full swing at CERN. Preparing the ATLAS detector for the High-Luminosity era (up to $7.5 \times 10^{34} cm^{-2} s^{-1}$), the present Muon Spectrometer's Small Wheels system will be replaced by the NSW in order to cope with the increased trigger and readout data rates. The NSW will be equipped with the Micromegas (MM) double wedges (DW) and the small strip Thin Gap Chambers (sTGC). The majority of sectors have been already placed on NSW, which is expected to be installed in the ATLAS underground cavern during the summer of 2021.



The NSW/side A assembly with 8 Small and 3 Large Sectors in B191 facility at CERN.

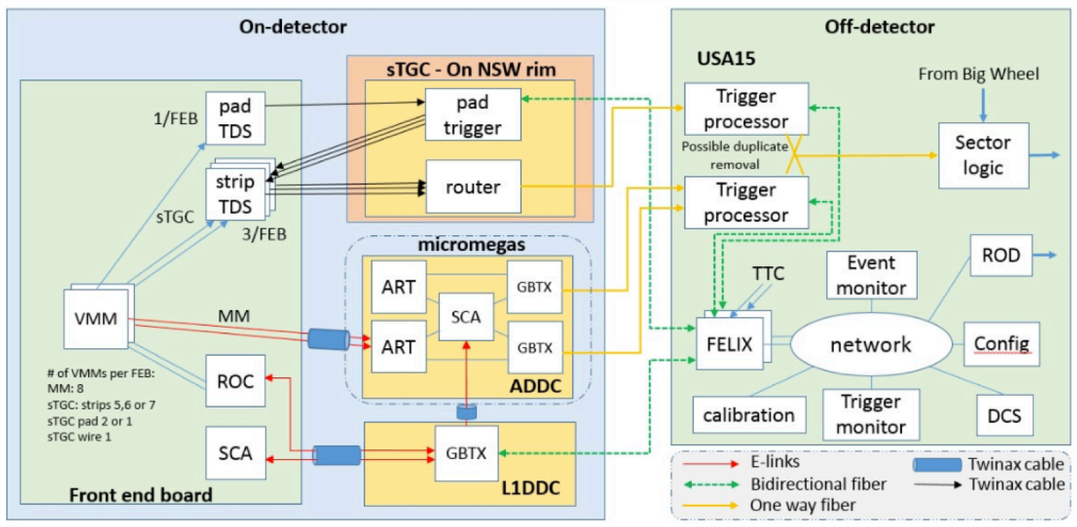
Micromegas detectors have a small conversion region (5 mm) and fine strip pitch (~0.4 mm) resulting in excellent spatial resolution and are primarily used for precise tracking. They are able to track particles with a precision of order 100 μm/detection gap while withstanding a particle rate up to around 20 kHz/cm^2. In total the MM NSW has ~1 K Data Driver Cards (Level-1 DDC & Address in Real Time - ART DDC), ~8 K Front-End Boards (MMFE8) and ~500 Low Voltage Distribution Boards (LVDB). With 2.1 M electronic channels in total, the operation of MM detector and the interface of NSW with the ATLAS Trigger and Data Acquisition (TDAQ) system with proper way, is challenging.



A fully equipped Micromegas DW.

NSW ELECTRONICS TRIGGER AND DATA FLOW

The NSW electronics for the trigger and Data Acquisition (DAQ) path of both detectors can be divided into two major categories, on-detector and off-detector electronics. The communication between the on-detector electronics boards is established with the use of mini Serial Attached Small Computer System Interface (SCSI) (miniSAS) cables.



Overview of the NSW Electronics scheme. The FE detector boards are depicted on the left (for MM and sTGC), L1DDC, ADDC in the middle alongside the Pad Trigger and Router, while the back-end electronics can be seen on the right.

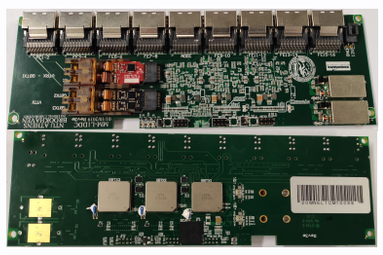
The off-detector electronics (Front End LInk eXchange (FELIX), TP sector logic and services running on commercial server Computers like Read Out Drivers (ROD), Detector Control System (DCS), event monitoring, configuration of boards, trigger monitor and calibration) will be placed outside the cavern in an area without radiation or magnetic fields. The readout chain is based on optical link technology (GBT links) connecting the back-end to the front-end electronics via FELIX, a newly developed system that will serve as the next generation read out driver for ATLAS.

NSW MICROMEGAS ELECTRONICS

The functionality of the MMFE8 is based on eight 64-channel VMM Application Specific Integrated Circuits (ASICs), and two companion chips: The Read-Out Controller (ROC) ASIC, and the Slow Control Adapter (SCA) ASIC, all custom radiation-tolerant chips, tailored for the needs of the NSW Upgrade. Each channel is connected to the corresponding detector readout strip. The signal of each strip transmitted to the Analog-to-Digital Converters (ADCs). The ROC's task is to gather the digitized data from the VMMs, in order to forward them towards the L1DDC upon reception of the Level-1 Accept (L1A) signal.

On the other hand, the SCA configure the VMMs, according to commands received by the L1DDC. Both companion chips are interfaced with the L1DDC via e-link, a custom serial communication scheme comprised of two data lines and a clock line, capable of reaching speeds up to 320 Mbps.

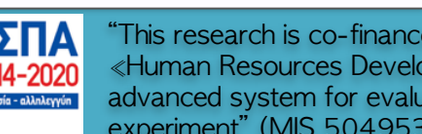
Micromegas FE8 board with VMM chips.



L1DDC with the MMFE8/ADDC connectors (up) and 3 GBTx (down) are shown.

The L1DDC, features three GigaBit Transceiver (GBTx) ASICs which act as high-speed transceivers, capable of accepting front-end data from multiple sources and forwarding them by optical link at a data rate of 4.8 Gbps. The L1DDC uses differential pairs for the communication with the front-ends combined in groups called e-links. One e-link consist of three differential pairs being the Clock, Data in, Data out. These serial streams can run at 80/160 or 320 Mbps. The main peruse of L1DDC board is to send configuration data to the FE and ADDC boards, receive the L1 data (time, charge, strip address) from the FE and send them to the FELIX network interface, distribute the TTC information, and receive monitoring data.

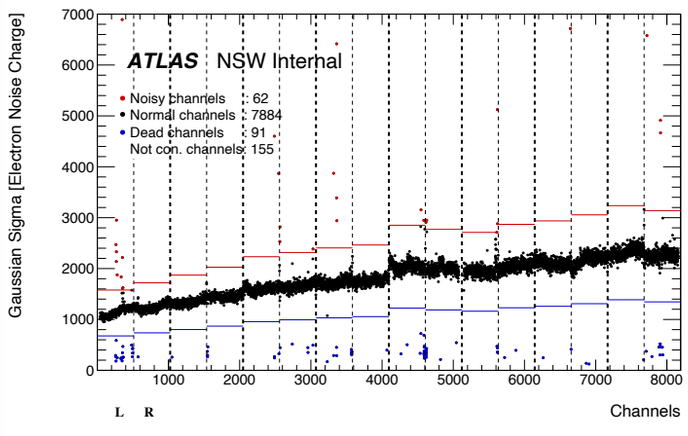
The ADDC houses two GBTx to receive the ART data from 64 VMMs (1 GBTx per 4 MMFE8s), and two ART ASIC custom-designed chip to perform hit-selection processing in real time. The processed ART data is then sent via optical links to the Trigger Processor. There, the FPGA's trigger algorithm makes the triggering decision based on the selected roads and ART hits.



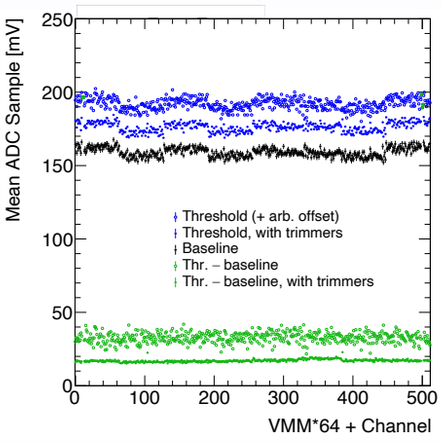
ADDC board with MMFE8/L1DDC connectors.

VALIDATION OF ON-DETECTOR ELECTRONICS

Before the installation of a sector on the NSW, various tests are taking place in order to validate the electronics. After the integration of MMFE8 boards, baselines are taken to identify noisy detector regions and dead/noisy channels. The noise level

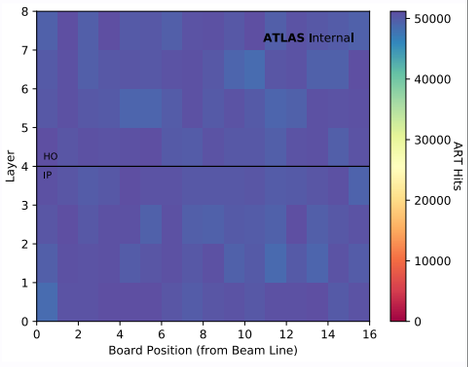


Baseline RMS per strip for one eta layer of a Micromegas Small Sector.



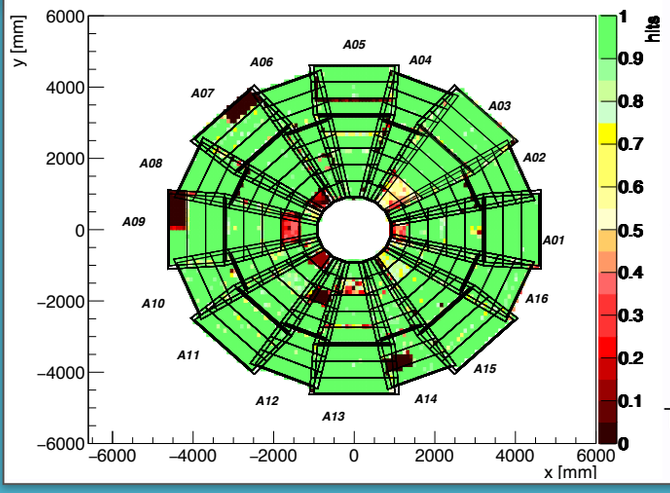
Threshold with trimmers per channel per MM VMM.

depends on the input capacitance to each electronic channel and as expected, the RMS value is increasing as a function of the strip number and the corresponding strip length. The reduction of noise levels is a crucial electronic challenge. Before the cosmic ray validation of the detector, the threshold level per channel is trimmed to mask the noise. Furthermore, the ART Connectivity test is used to validate the trigger scheme between MMFE8s, ADDCs and the Trigger Processor's readout. Using the VMM's internal pulser, ART data are produced from test pulses and they are used to simulate the propagation through the detector's front end electronics.



Connectivity test with TP per board per MM Layer.

The final step of the MM sector validation is performed with cosmic rays. The trigger is provided by scintillators at ~100 Hz with full coverage along the precision coordinate covering partially the detector. For the Micromegas sector operation the nominal High Voltage settings are applied, +570 V for the strips, −300 V for the drift gap. The selected gas is Ar:CO_2 93:7. The overall electronics performance is shown through the efficiency maps, where each module's specific HV tunings are considered.



Track efficiency map of one layer of NSW side A.

DAQ FIRMWARE OVERVIEW - READOUT CHAIN

The SoftWare ReadOut Driver (ROD) is a new component of the ATLAS DAQ system that was developed to receive data from the FELIX. The SW ROD implements a high performance customizable framework that supports custom input data formats and different event fragment aggregation strategies as required by the new ATLAS detector and trigger components.

For the integration of the detector into the ATLAS data acquisition system, a dedicated Micromegas segment has been implemented, in the framework of the new ATLAS TDAQ online software, in order to include the detector inside the main ATLAS DAQ partition. The Software Read-Out Driver interfaces with FELIX, processes the incoming data before sending them to the High Level Trigger. The system is still in developing mode and focuses on data format and running functionalities. It needs initialization, recovery and integration with ATLAS Timing,Trigger & Control system. In the last step, the data are packed up into architecture-defined ROOT files, a capable format for data analysis.

Ευρωπαϊκή Ένωση
Ευρωπαϊκό Κοινωνικό Ταμείο

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