The Particle Flow Algorithm in the Phase II Upgrade of the CMS Level-1 Trigger

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Particle Flow and PUPPI in L1 trigger

Inclusion of tracking at L1, combined with Calo and Muon

Efficient tracking, fine granularity calorimetry allows online PF PUPPI

Part of Correlator Trigger

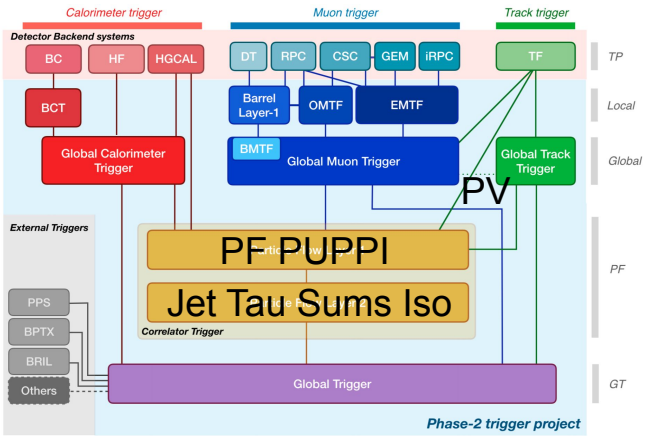
1. Layer 1 PF PUPPI, Combine all detector information
2. Layer 2 PF PUPPI Objects then used as input for jets, tau, sums, isolation

The goal of the Correlator Trigger is to calibrate and combine information from different sub-detectors to build PF/PUPPI objects in layer 1, and then to build higher level objects such as jets with those PF/PUPPI object in layer 2, to build trigger logic with those high level objects.

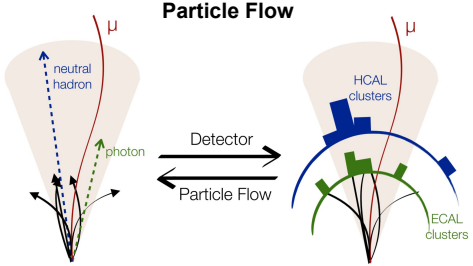
High pile-up in HL-LHC environment PF PUPPI are necessary, and PF PUPPI objects used for downstream advanced online trigger algorithms

Detector subdivided into eta-phi **regions**, process the regions separately

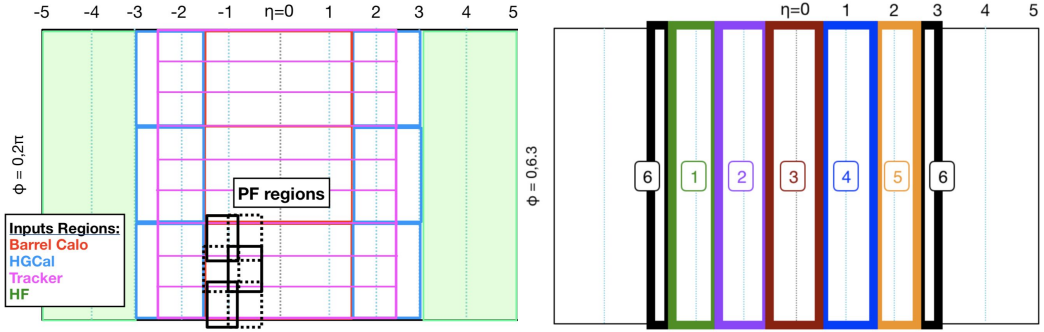
L1 Trigger Diagram



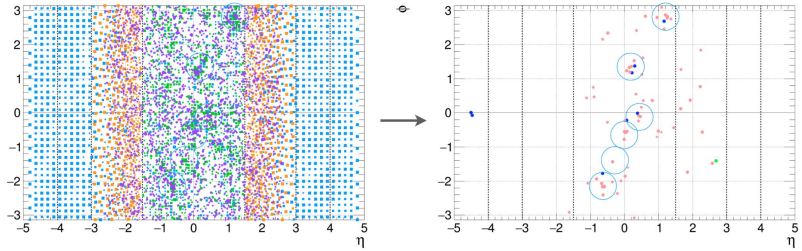
Particle Flow



PF Region Definition



Detector Inputs **PF/PUPPI Reconstruction**



Layer 1 Firmware Implementation

In Layer 1, sub-detector inputs are regionized, then we link objects to build PF, then PF with PV we get weighted PUPPI

Full detector at 40MHz, Fixed Latency <1μs, Firmware implemented and tested in Xilinx VU9P FPGA on prototype boards, might change to newer chips in the future

Fast FPGA firmware development of complex algorithms with High Level Synthesis (HLS) tools, and stitch together with optimized VHDL algorithms(regionizing, sorting, shifting, infrastructure)

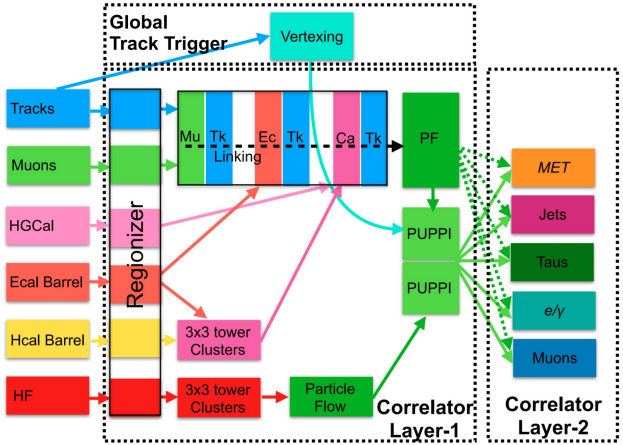
Different Initiation Interval(II) and region numbers vs FPGA resources studied (possible with HLS tools)

36 boards(18 barrel, 18 endcap) at TMUX=6, 6boards/BX, 9Clocks/BX, 18regions/board(Barrel), 9regions/board(Endcap)

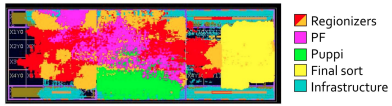
- Endcap: in each region max 30 tracks, 20 clusters, 4 muons → 18 highest pt sorted puppi candidates
- Barrel: in each region max 25 tracks, 18 calo, 12 emcalo, 2 muons → 18 highest pt sorted puppi candidates

Algorithm meets timing, and perfect agreement is achieved between the regionizer firmware and software emulation → Now let's build higher level objects!

Dataflow

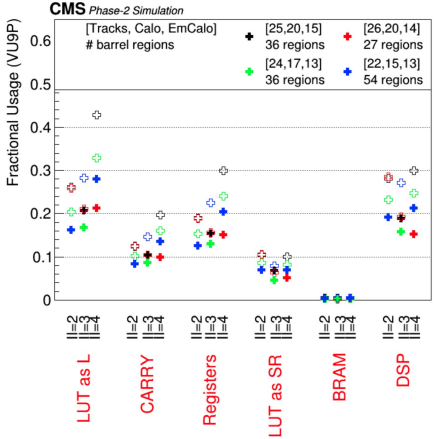


FPGA (VU9P) Floorplan

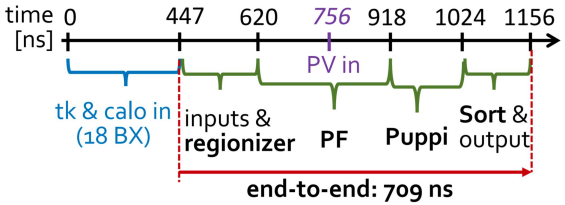


3SLRs

FPGA Resources vs II&Region

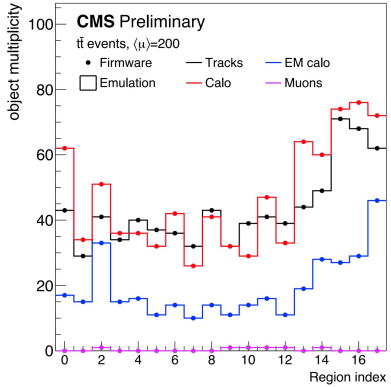


Latency Budget



II = 4 for the endcap (16ns)
II = 2 for the barrel (8ns)

Firmware vs Emulation



Layer 2 Algorithms & Firmware

30 boards, receive input from layer 1 at TMUX=6 via 25Gbps links, each layer 1 board sends up to 162 PF/PUPPI candidates (64 bits) on 3 link to each layer 2 board

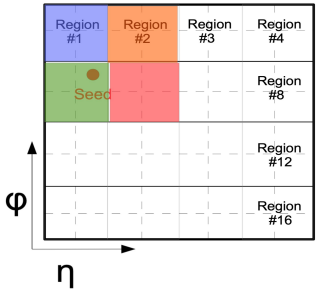
With PF PUPPI object inputs from Layer 1, we can build higher level objects: **Jets, Taus, Sums, Isolation, for each object consider a range of algos**

Studies performed prior to hardware implementation

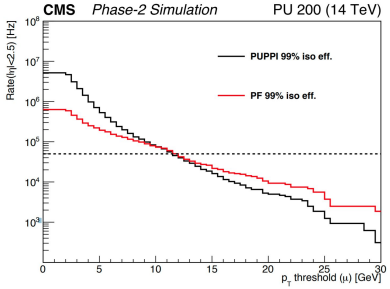
CT output sent to GT on 30, 25-Gbps links, meaning we can output 27 objects (128 bits per object).

Seeding for downstream algorithm implemented using grid structure, take highest pt PF/PUPPI candidate per region, once seed is chosen, LUT used to select 4 neighboring regions, also considering seed-based algorithm without regions

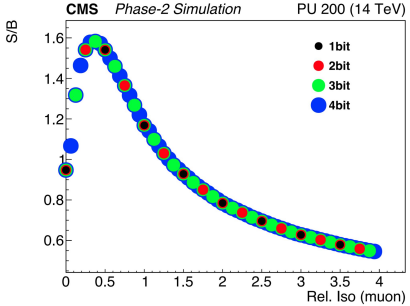
Seeding for Layer 2



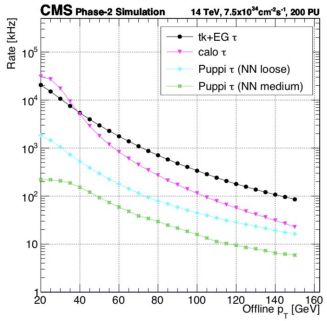
PF/PUPPI Isolation



Bit Precision for Isolation



Neural Net Tau Rate

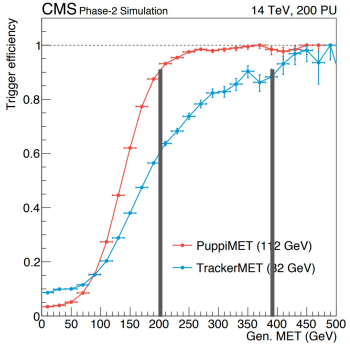


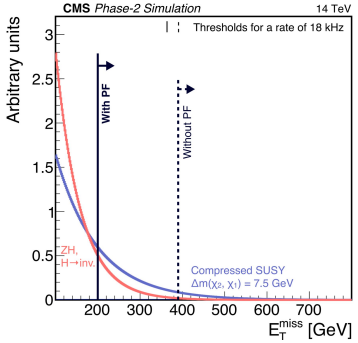
Firmware development finished / actively pursued at the moment!

Trigger Performance and Physics Implication

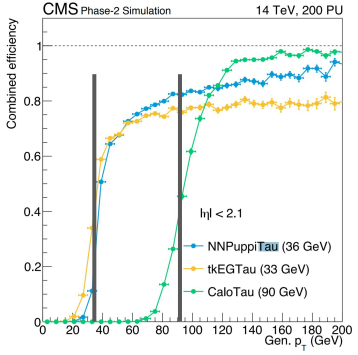
Performance improvement vs Calo or Track only
PF + PUPPI allows for **sharper & earlier** turn ons, **major gains in signal acceptance**

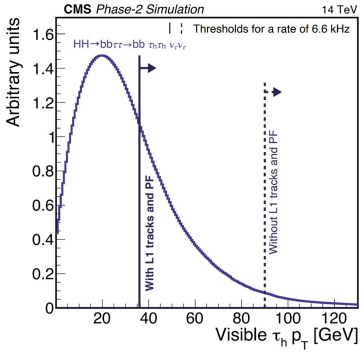
MET



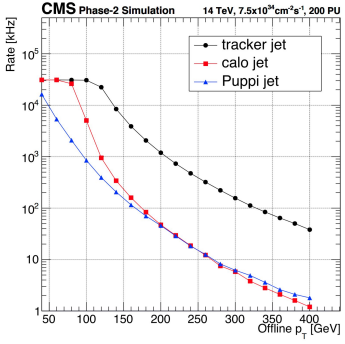


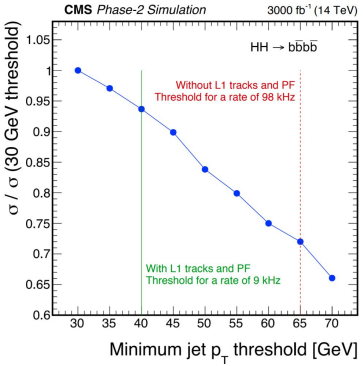
τ_h



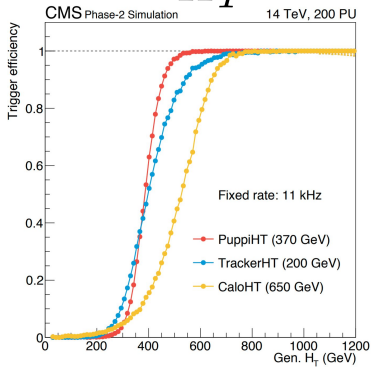


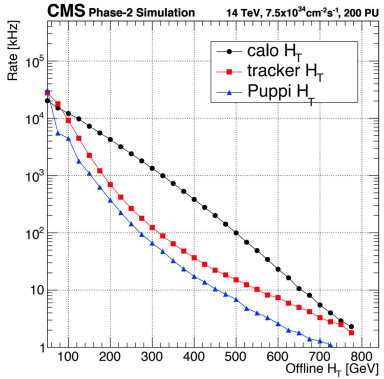
Jet





H_T





References

CMS Phase 2 Level 1 Trigger Technical Design Report

http://cds.cern.ch/record/2714892/files/CMS-TDR-021.pdf