Development of FPGA based 128-Channel TDC for Time Projection Chambers

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ASIC Vs FPGA TDC

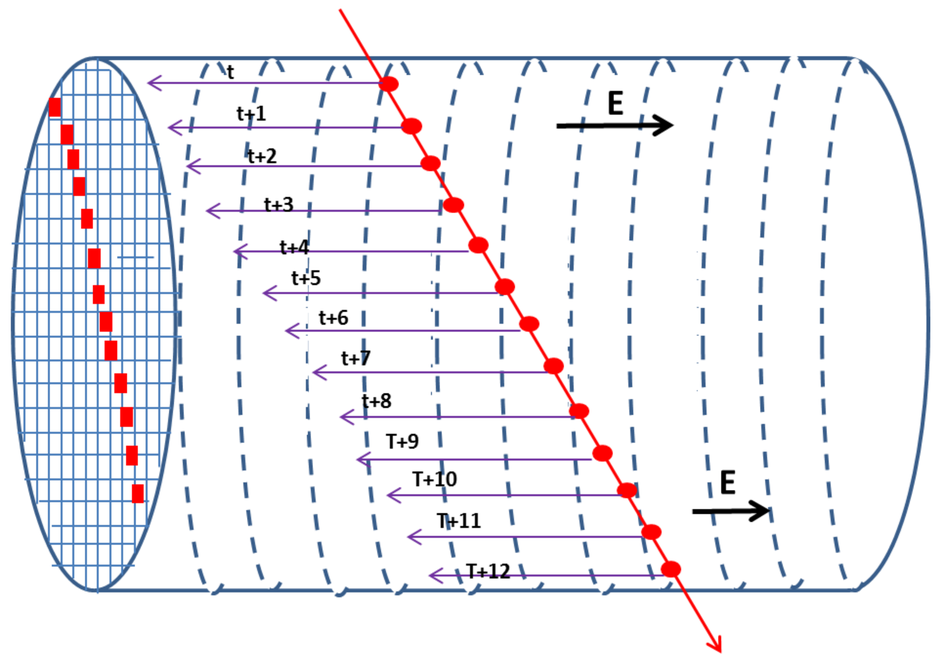
ASIC TDC

- Long time to design
- Design Cost is high
- Non Reconfigurable
- Better Performance in Ambience

FPGA TDC

- Quick to deploy
- Cost Effective
- Reconfigurable
- Higher Channel Density
- Prototyping Friendly

Importance of timing in TPC

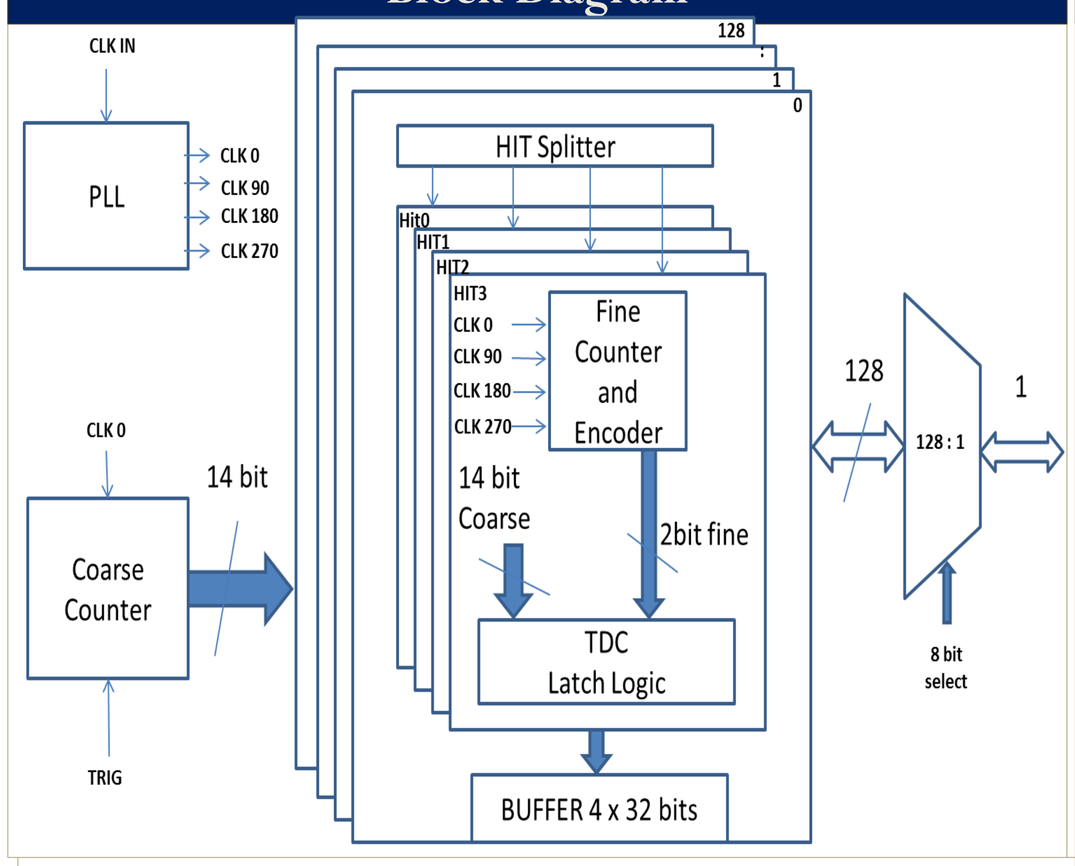


- Charged particle traverses the TPC volume, ionizes the gas atoms along its trajectory.
- The free electrons produced move towards anode with a speed depending on the gas mixture and the applied field.
- Arrival times and hit channel information are used to track the particle.
- Arrival times of these slow-moving electrons at the anode provides precise position of interaction.

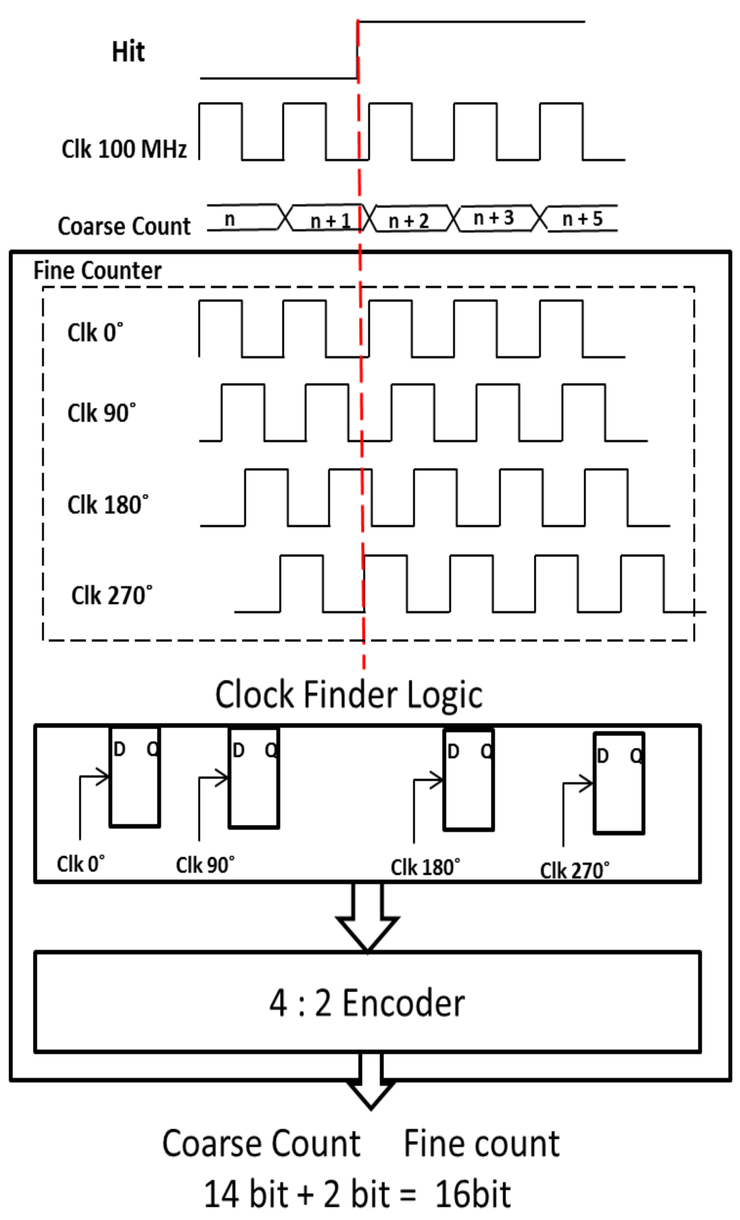
Working Principle

- An FPGA-based Start-Stop type Time to Digital Converter is designed.
- To Acquire the trajectory of the particle A trigger is generated using coincidence of scintillator detectors placed top and bottom of TPC.
- The TDCs common 14 bit Coarse counter Starts on Trigger arrival.
- When a electron\hit signal arrives the TDC latches 14 bit counter value
- Also a 2 bit fine counter value captured from the 4 Phase shifted clocks
- This method is called Shifted Clock Sampling
- Together this forms a 16 bit timestamps of arrived hit signal.

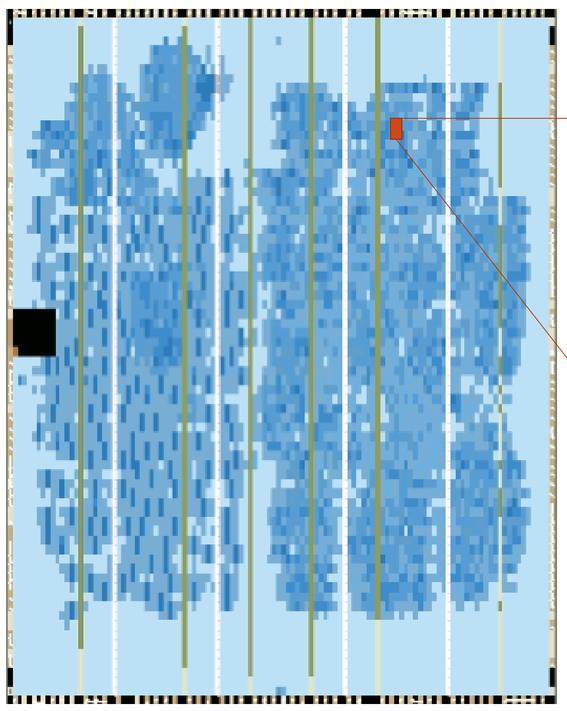
Block Diagram



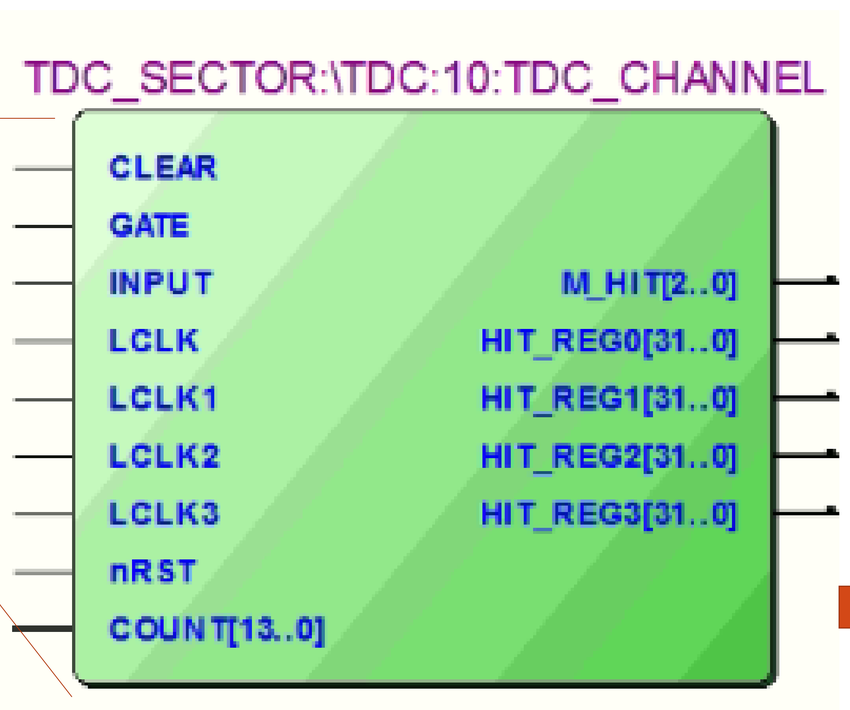
Timing



FPGA Real Estate



TDC Core



- Each Channel is connected to dedicated TDC sector
- Each TDC Sector Takes coarse count and 4 phase shifted clocks as input for time stamp.
- Each sector is provided with dedicated 4 32 bit registers for storing hit time stamps.

FPGA Resources

Family Cyclone IV E
FPGA Device EP4CE115F29C7
Total logic elements
40,620 / 114,480 (35 %)
Total pins
362 / 529 (68 %)
Total memory bits
2,939,328 / 3,981,312 (74 %)
Embedded Multiplier
4 / 532 (< 1 %)
Total PLLs 2 / 4 (50 %)

TDC Specifications

- 100 MHz Coarse clock
- 128 Channels
- Dynamic Range 160us
- Resolution 2.5ns
- Multi hit up to 4
- Both Leading and Trailing edge measurement
- 32 bit Time stamp
- Configurable Parameters
- Multiplexer based Timestamp Register Access
- Can be scaled to 256 Channels

Conclusion

- TPCs requires marginally lower resolution of timing device but more channel density
- Designing an ASIC with more channel density complicates the design.
- FPGA based TDC can be easily scaled to more channels.
- Also with higher operating Frequency higher Resolution can be achieved.
- PLL and DCMs must be used to maintain jitter free clock

Visiit: http://www.ino.tifr.res.in/ino/