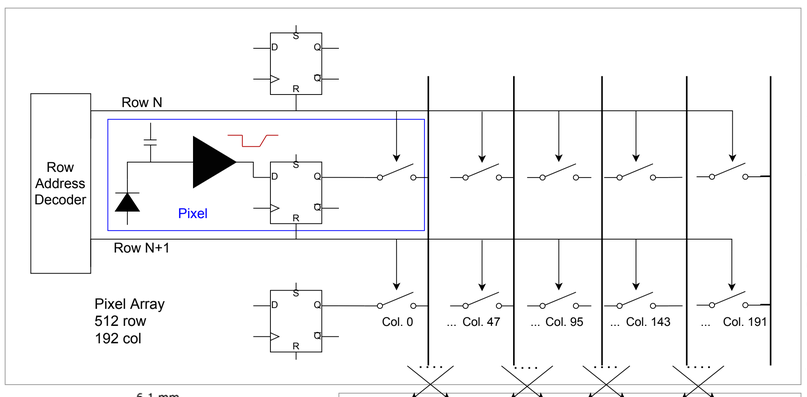
The DAQ and control system for JadePix3

Abstract: The silicon pixel sensor is the core component of the vertex detector for the Circular Electron Positron Collider~(CEPC). The JadePix3 is a full-function large-size CMOS chip designed for the CEPC vertex detector. To test all the functions and the performance of this chip, we designed a test system based on the IPbus framework. The test system controls the parameters and monitors the status of the pixel chip. By integrating the jumbo frame feature into the IPbus suite, the block read/write speed is further extended in order to meet the specifications of the JadePix3. The robustness, scalability, and portability of this system have been verified by pulse test, cosmic test and laser test in the laboratory. This paper summarizes the DAQ and control system of the JadePix3 and presents the first results of the tests.

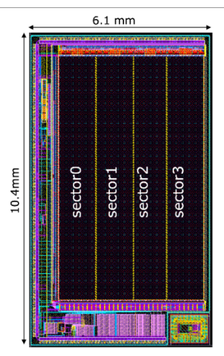
JadePix3 Overview

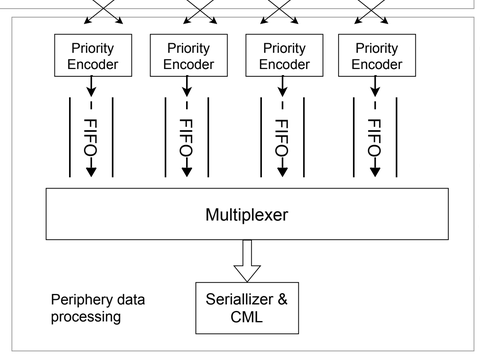
A prototype sensor, namely JadePix3, has been developed for the CEPC vertex detector. The goals of the JadePix3 project are to study the designs of the silicon sensor of high spatial resolution, low power consumption, modest readout speed and small-sized front-end circuits. The JadePix3 is a CMOS pixel sensor manufactured in the TowerJazz 180 nm CMOS image sensor process. The total size of the chip is 10.4×6.1 mm^2 (512×192 pixels), with the minimal size of the pixel at 16×23.11 μm^2.



Rolling shutter readout structure is adopted for its simple structure.

The working mode of rolling shutter is to read one row at a time, turn on the output switch of one row through the control line of the row distribution, and reset the register of the previous row at the same time.





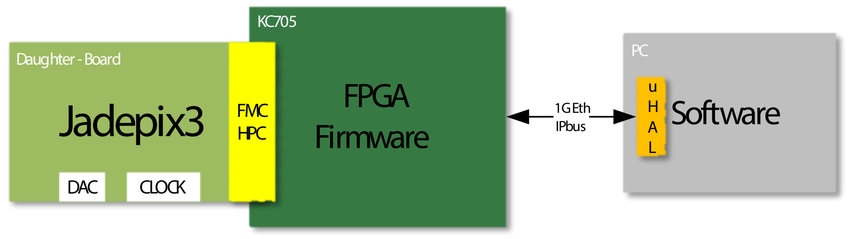
The JadePix3 uses a weak inversion current comparator to amplify and discriminate the signals in the pixel.

The threshold signal is stored in the register in the pixel and to be read out by row-by-row scanning.

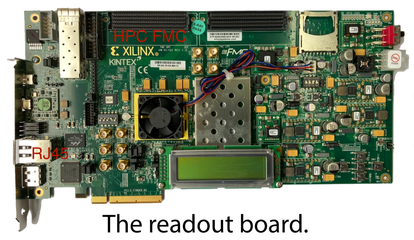
The scanning speed is 192 ns per row, and the time to complete a frame is 98.3 μs.

Test Setup

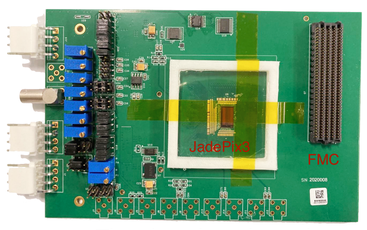
The test system includes the chip to be tested, the FPGA readout board, the daughter board, and the control and data acquisition system based on the IPbus framework.



Overview of the test system.



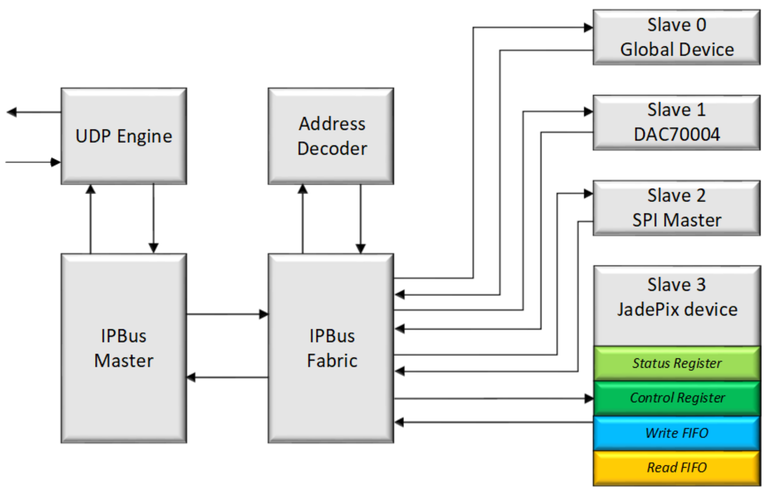
The readout board.



The daughter board.

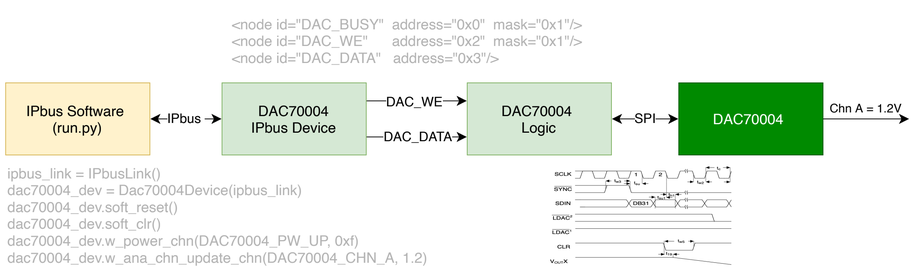
A commercial FPGA board (Xilinx, KC705) is using as the Read Out Board.
A daughter board contains a JadePix3 chip was designed for testing. Besides the JadePix3 chip, low voltage (LV) power supplies, a digital to analog converter (DAC70004) and an FMC connector are also mounted on the daughter board.
The readout board controls all these chips via the FMC connector.

The IPbus framework of the JadePix3

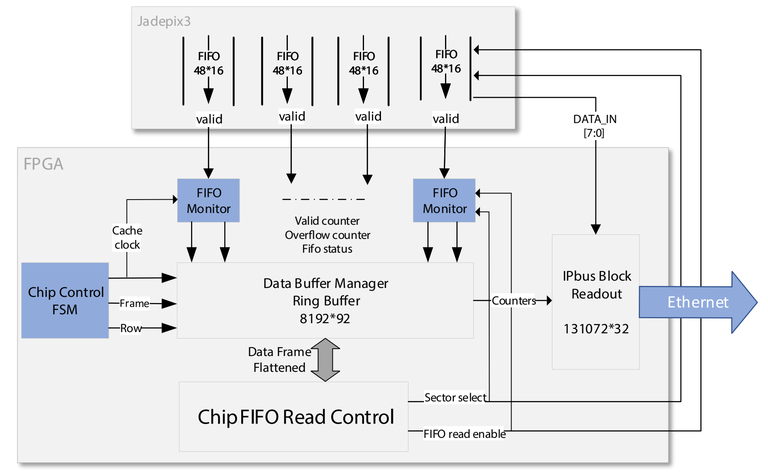


The IPbus slaves in firmware. Four slave devices are developed according to controlling and data readout needs.

IPbus: a flexible Ethernet-based control system for xTCA hardware
https://ipbus.web.cern.ch/ipbus

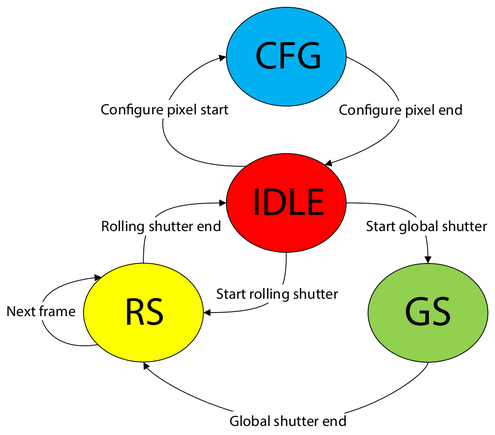


An example of how the DAC70004 is controlled via the test system.
1. The software sets the parameters of DAC by the DAC70004 nodes defined in the XML file. There are three register nodes (two control registers and one state register) are defined in the DAC7004 XML file.
2. While the DAC70004 device in firmware received the IPbus commands, the control timing will be generated, then the DAC70004 outputs the desired voltage.



This the structure of the JadePix3 readout firmware, which needs to steer the data flow in the JadePix3.
FIFO Monitor: Monitor the FIFO status (valid counter, overflow counter) in the chip.
Ring Buffer: Record the frame number, the row number and the value of their corresponding FIFO counters.

Working FSM



The diagram of the working states and transitions.

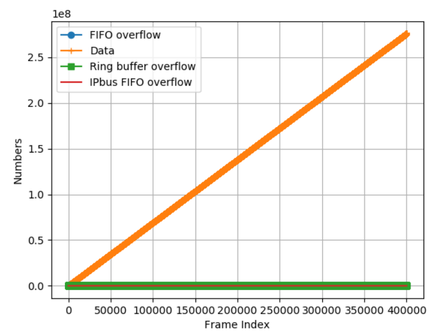
IDLE: initial state.

CFG: configure two D-latches (MASK, PULSE) of each pixel.

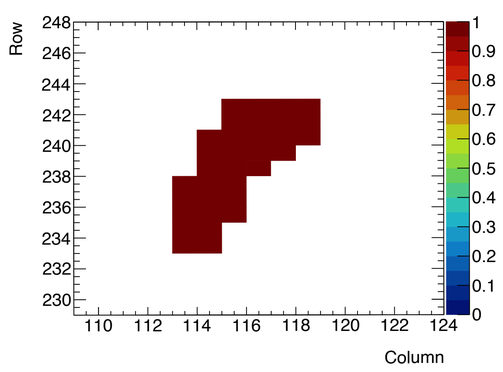
RS: transmits data to the end of a column through the column-level data line, and reads the signal through the data processing logic at the end.

GS: all sensor pixels "expose" simultaneously and readout afterwards .

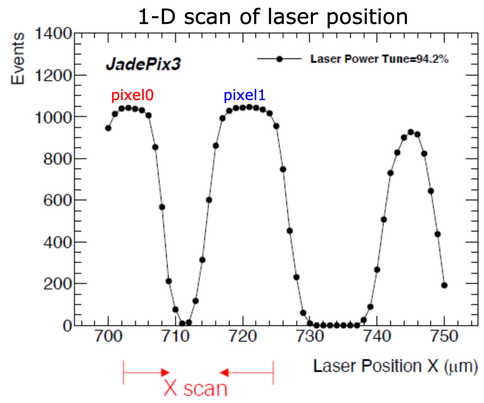
Pulse test, cosmic test and laser test



Pulse test: hit number per each event = 2048, frame number = 400000. The status of data accumulation and system overflow status. Event interval = 110 μs. The data throughput is 595.8 Mbps× 39.3 s, no overflow is found.



Cosmis test: BANDGAP_ALT=1.2 V, frame_num=400000. The chip is perpendicular to the ground. This figure is one of the four captured signals.



1-D scan of laser position. The laser wavelength is 1064 nm, the scan direction is from pixel0 to pixel 1, and the scan step is 1 μm.

The JadePix3 test system is developed based on the IPbus framework. This system is reliable and flexible for chip testing. The system has tested almost all the chip modules, the stability and portability of the system have also been verified under different test conditions. The jumbo frame feature has been integrated into the IPbus suite for meeting the readout speed requirement of the experiment. This system has been successfully applied to the testing of the JadePix3 and it has great potential to be applied to similar readout architecture pixel chips.

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