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The DAQ and control system for Jadepix3

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The silicon pixel detector is the core component of the vertex detector in the CEPC experiment. The Jadepix3 is one of the chips designed to study the performance and design of pixel sensor chips. The chip is a design of the full-function large-size chip based on CMOS technology. To test all the functions and the performance of this chip, we designed a test system based on the IPbus framework and the EPICS framework. The data acquisition system is developed by using the IPbus framework. The data of the chip will be read out into an FPGA first and then transferred to PC via a 1 Gigabit ethernet. Besides the devices on the test PCB, some important parameters of the readout system are also controlled and monitored by using the EPICS framework. The robustness, scalability, and portability of this system have been verified in the laboratory tests.

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No, this is an entirely new submission.

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