Firmware development for trigger-less mPSD readout at mCBM experiment at GSI

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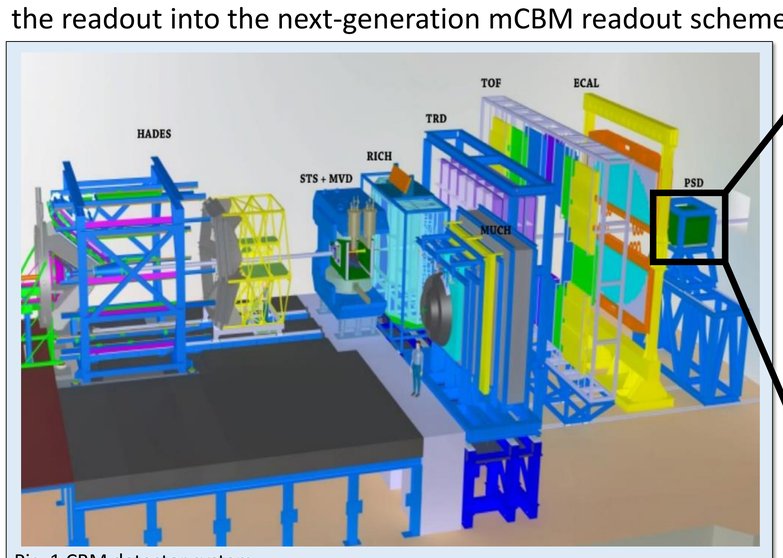
The Compressed Baryonic Matter (CBM) experiment at FAIR needs a detector to measure the nucleus-nucleus collision centrality and orientation of the reaction plane. This will be obtained with the Projectile Spectator Detector (PSD), which is a sampling lead/scintillator forward hadron calorimeter with transverse and longitudinal segmentation. As the CBM experiment will measure relativistic nucleus-nucleus collisions with collision rates up to 10MHz, the data acquisition system is based on triggerless-streaming. Here, most of the detectors readout electronics is being developed based on CERN GBTx data aggregation units.

The PSD readout system is based on ADC FPGA board which was originally designed for ECAL@PANDA. This hardware employs two Kintex-7 FPGAs which are processing the incoming data from ADCs with 14-bit resolution and 125MHz digitization rate for 32 channels per one FPGA. In order to integrate the PSD ADC board to the common CBM DAQ, a FPGA-GBT component was included into the FPGA design. Here, a clock switching procedure to run the ADC board with the recovered GBT receive clock in order to synchronize the hardware to the common CBM DAQ time was implemented and successfully tested in a test experimental run with a reduced set of detectors (mCBM).

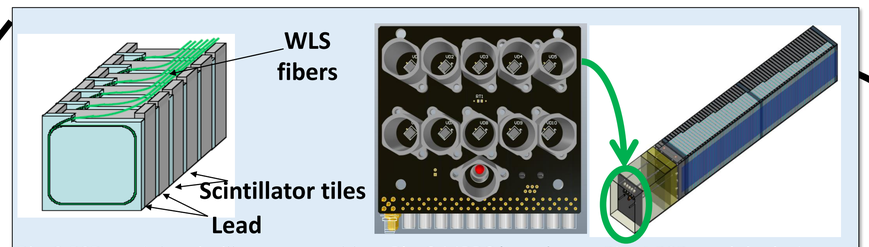
The development of components for digitizing waveforms reaching 1MHz readout rate per channel tested in mCBM test runs and the trigger-less readout will be discussed as well as the inclusion of the readout into the next-generation mCBM readout scheme.



Pic. 1 CBM detector system.

CBM will explore strongly interacting matter at highest net-baryon densities by investigating nucleus-nucleus collisions in fixed-target mode with extracted beams from the SIS-100.

- high-rate capability of up to 10^7 interactions per second;
- CBM will employ fast and radiation-hard detectors and readout electronics;
- free-streaming data acquisition system;
- self-triggered front-end electronics.



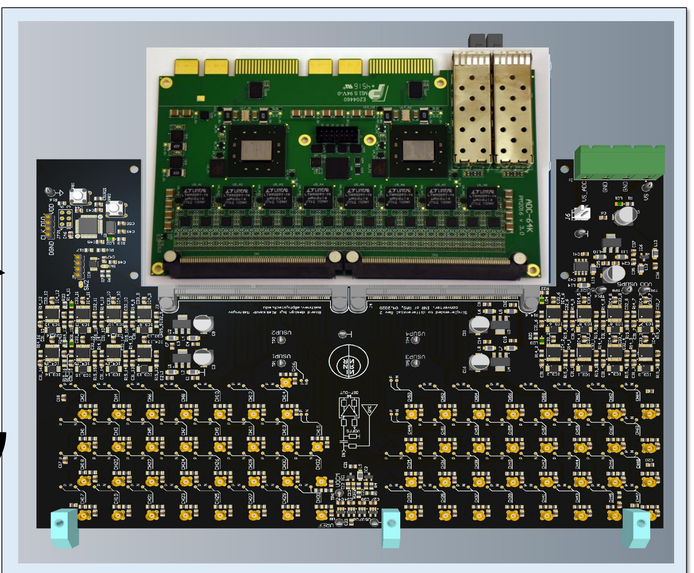
Pic. 2 PSD module scintillators assembly.

Pic. 3 MPPC board.

Pic. 4 PSD module design.

- Module transverse size 200x200mm^2 .
- Longitudinal structure: 60 Pb/Scint tiles layers: (Pb(16mm), Scint(4mm) grouped in 10 sections.
- Hamamatsu *S12572-010P;* Sensitive area 3x3 mm^2; Number of pixels 90 000; Nominal gain 1x10^5; Pixel recovery time 10 ns.
- 10 MPPCs; Calibration LED; Temperature sensor; Light protection hardware.
- 44 PSD modules = 440 channels.

46 modules x 10 channels 50m coaxial cables (460 in total)



Pic. 6 ADC board + addon assembly.

8 x 2 optical GBT links

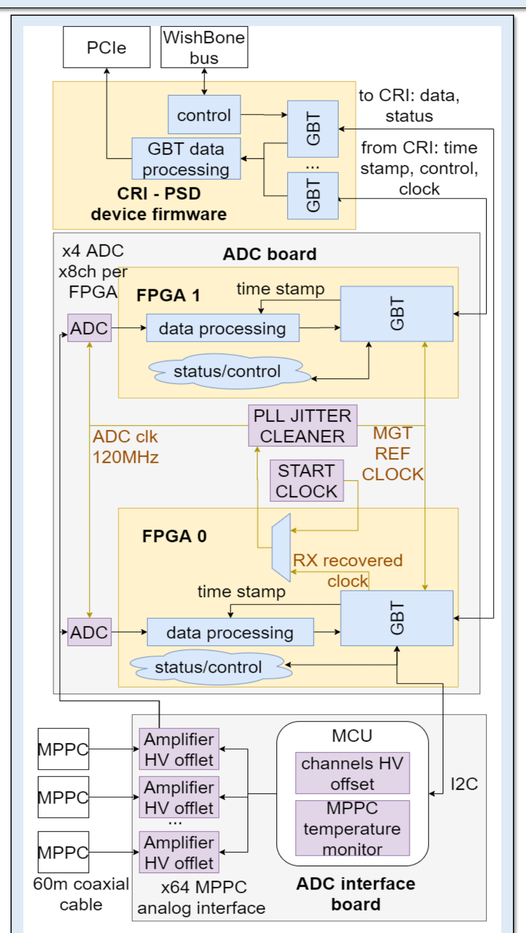
Pic. 5 CRI board.

The Common Readout Interface (CRI) board, based on the the BNL-712 card, is a PCIe Gen3 x16 device interfacing up to 47 GBT links. This CRI board will be the main component of the DAQ system.

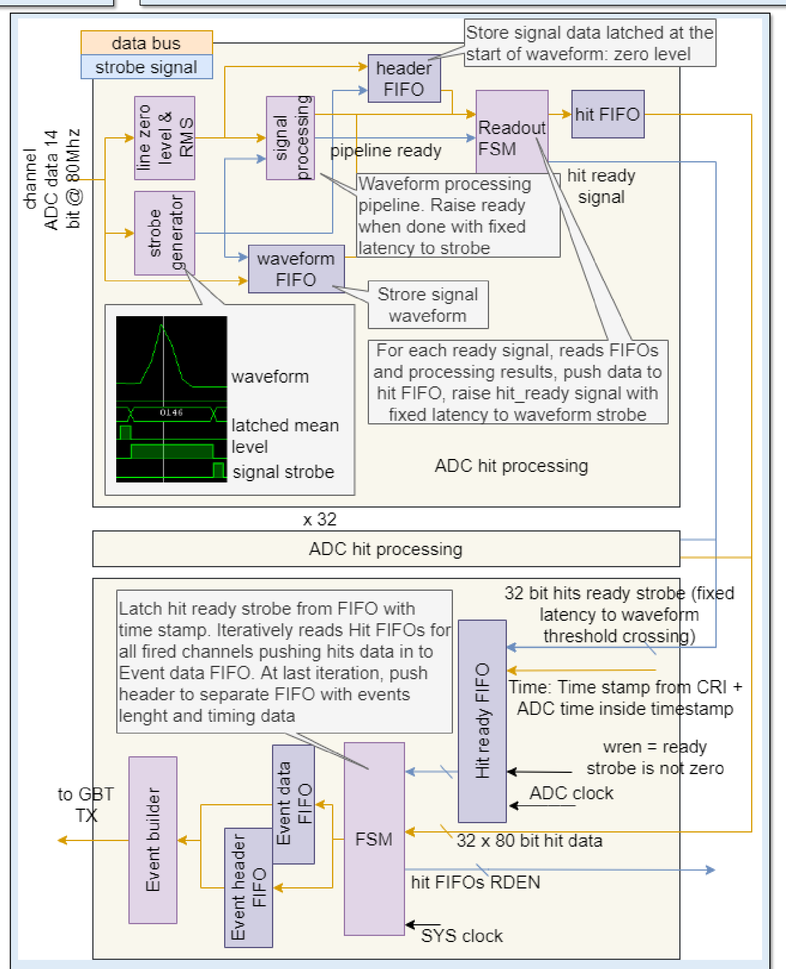
Readout module 64ch X 8 boards

- Single-ended ADC interface module: adjustable input and output zero level, 1:2 conversion ratio;
- High voltage adjustment circuit via per-channel common-mode compensation;
- MPPC board temperature monitoring;

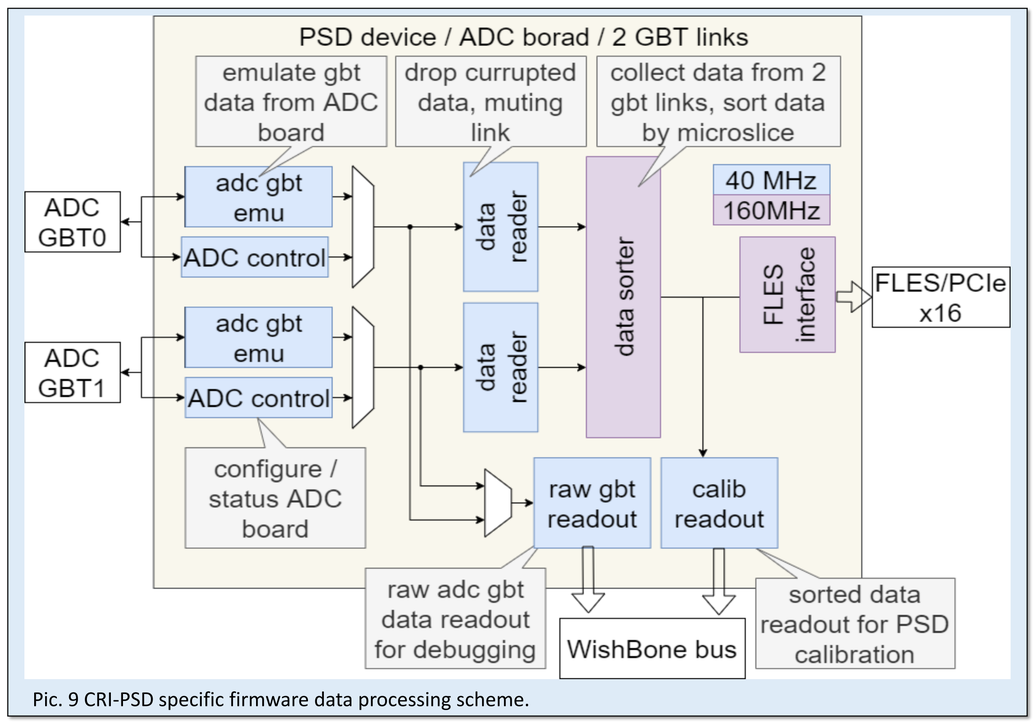
- ADC64 board
  - LTM9011 ADC;
    - 125Msps / 80Msps (used now); 14-bit digitization; Selectable Input Ranges: 1VP-P to **2VP-P (used);**
  - Two FPGA Kintex 7
    - 32 channels per one FPGA; Separated optical link for each FPGA; Signal processing on the fly;
  - Readout rate
    - 3 Gbit/s (GBT 80bit@40MHz); Top limit: 3.2 Gbit/s / 32 channels / 1 MHz readout rate = 100bit/hit (80bit used now).



Pic. 7 PSD readout data path and ADC – CRI communication, clock distribution scheme.



Pic. 8 ADC firmware hits acquisition and data collection scheme.



Pic. 9 CRI-PSD specific firmware data processing scheme.

Signals from MPPCs are collected by the ADC Addon board, which provides a single-ended interface based on single-ended to differential converters with adjustable input and ADC baseline level, as well as high voltage correction circuit through common mode compensation[1]. MPPC temperature measuring system (designed, not prototyped yet) will be also placed on ADC addon board. Control of the board is accomplished through an STM32F103 microcontroller placed on the Addon board, which receives commands and adjustment data from the ADC board via I2C interface.

The ADC board initially designed for the ECAL detector of PANDA experiment [2]. The 64-channel board is based on two Kintex 7 (xc7k160) FPGA (field-programmable gate array) and LTM9011 ADC (analog-to-digital converter) with digitization rate up to 125Msps (currently 80MHz is used) and 14-bit digitization resolution. Clock from TD-100 is used for initial FSM and forwarded to LMK0460 jitter cleaner, output is used as source of clock for ADCs and MGT GBT transceiver. GBT-FPGA [3] link is connected to Common readout interface (CRI) of CBM DAQ system and is used for data transport, clock distribution and board control. After GBT RX locks and is stable, source of LMK0460 is switched to GBTRX recovered clock, that makes ADC synchronous to CBM DAQ. Time stamp from CRI is used for measuring event time synchronously to whole CBM DAQ in trigger-less readout concept. Second FPGA also is connected to CRI via GBT link and use recovered ADC and MGTREF clock from first FPGA.

The prototype of ADC firmware allow analog signals acquisition individually for each channel by threshold crossing. Force triggered acquisition s is possible by ‘and’ and ‘or’ combinations of channels events and asynchronous pulser. Bottleneck of data throughput is GBT bandwidth 80bit@40MHz, kipping 80bit per single hit data the maximum hit rate is 1.2MHz if all 32 channels are fired, that fit CBM requirements 1MHz event rate for PSD. Also online monitoring of baseline zero level and noise RMS, measuring readout rate in range 0.5 to 4.5MHz features are implemented. Possibility to send raw signals waveforms simplify calibration and debugging of PSD readout. Online signal processing will be based on proni-fit[4] and implemented with instruction pipeline architecture. Current design use approximately half of FPGA resources.

Specific firmware unit was designed for PSD data processing in CBM common readout interface (CRI). Design control and combine data from two gbt link of single ADC board and provide data sorted by time stamps in FLES (First Level Event Selector) interface. Data taking is also possible through slow control wishbone bus for calibration and debugging purposes. Control and readout software was implemented with python3 macros for upcoming beam tests.

Conclusion

ADC board and ADC board addon assembly, were tested at mCBM beam tests in 2019-2020 with single PSD module (mPSD) [5]. Integration into mCBM DAQ based on GBT link was done and time synchronization into the whole detectors system for mPSD hits acquisition was proved. In 2021 full PSD readout chain prototype included ADC board, ADC board addon, MPPC board, 65m coaxial cable for analog signals was assembled and installed with mPSD module for upcoming test at mCBM beam tests in May – June. Currently the mPSD readout prototype as well as developed firmware for ADC board and CRI – PSD was successfully tested with cosmic and LED runs. Next steps in ADC firmware development are test readout with two active FPGAs, increasing ADC clock frequency from 80 to 120 MHz and implementation of signals waveform fitting procedure.

Refereces

[1] Development of readout chain for CBM Projectile Spectator Detector at Conference Series 1690 (2020) 012059 oi:10.1088/1742-6596/1690/1/012059

[2] Serneguet Sorli, ´A. (2015). A multichannel digitizer for the PANDA experiment. http://hdl.handle.net/10251/56722

[3] GBTX manual http://cern.ch/proj-gbt

[4] Methods of signal processing and cosmic muon calibration for the BM@N sampling lead/scintillator hadron calorimeter Published in: JINST 15 (2020) 05, C05050 DOI https://doi.org/10.1088/1748-0221/15/05/C05050

[5] The readout system of the CBM Projectile Spectator Detector at FAIR CBM Collaboration Published in JINST 15 (2020) no.09, C09015 DOI: 10.1088/1748-0221/15/09/C09015