A new data transfer scheme for the HL-LHC upgrade of the ATLAS Tile Hadronic Calorimeter

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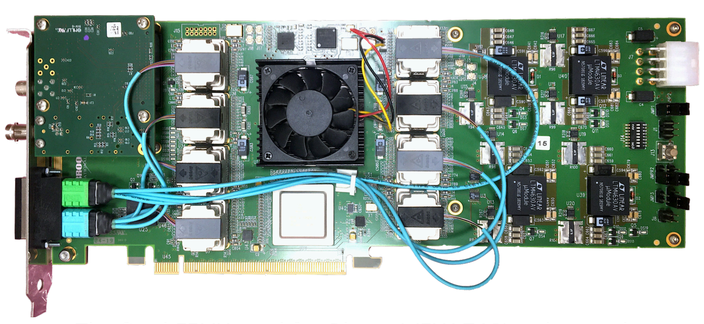
THE ATLAS TILE CALORIMETER PHASE-II UPGRADE

The Large Hadron Collider (LHC) is undergoing a series of upgrades towards a High Luminosity LHC (HL-LHC) that will deliver five times the LHC nominal instantaneous luminosity. To prepare for data taking in high-luminosity conditions, the ATLAS Tile Hadronic Calorimeter (TileCal) will replace completely on- and off-detector electronics using a new read-out architecture.
The TileCal detector signals will be digitized by on-detector electronics and transferred to the TileCal PreProcessors (TilePPr), which comprise the main component of the off-detector electronics. In the TilePPr, the digitized data will be stored in pipeline buffers and be packed and read out to the Front-End LInk eXchange (FELIX) system upon the reception of a trigger decision.
FELIX is a new detector readout component being developed as part of the ATLAS upgrade effort. FELIX is designed to act as a data router between the data acquisition detector control and TTC (Timing, Trigger and Control) systems and the new or updated trigger and detector front-end electronics. Whereas previous detector readout implementations relied on diverse custom hardware platforms, the idea behind FELIX is to unify all readout across one well supported and flexible platform.
In this contribution we present the TileCal read-out strategy for the HL-LHC, a detailed description of the PPr interface with the FELIX and tests performed with the PPr and FELIX prototypes in the testbench.

NEW DATA TRANSFER SCHEME IN THE TILE CALORIMETER

FELIX

FELIX will function as a router between custom serial links and a commodity switch network using standard technologies to communicate with commercial data collecting and processing components.
The downlink (up to 4.8 Gbps), used to receive slow controls, TTC commands and the LHC clock shall be implemented using the latency optimized GBT protocol for recovery of the LHC clock with deterministic latency.
The uplink (up to 9.6Gbps in Full Mode), used to transmit triggered data to the FELIX, does not require deterministic latency but demands more data bandwidth depending on the trigger scheme.
The worst-case scenario from the data bandwidth to FELIX requirement point of view is the L0-only scheme, where the PPr has to transmit triggered data at 1 MHz.
The complete TileCal readout system will include 161 bi-directional links with FELIX: 128 for data readout, 32 for trigger primitives monitoring and 1 for the Laser calibration system.



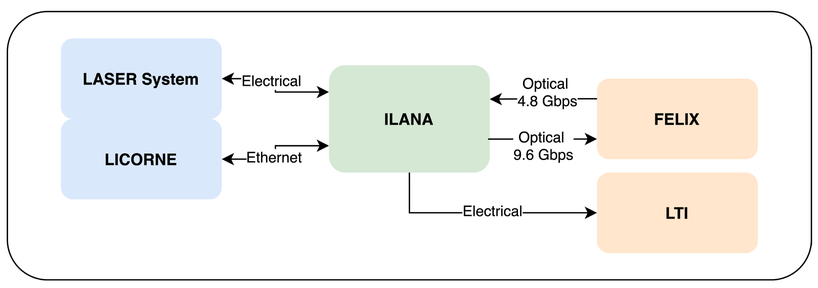
The final FELIX card for Phase I (FLX-712) to be used in beam tests.

ILANA

ILANA is the TileCal Interface for the Laser system to the New Acquisition infrastructure. ILANA will be responsible for:

- control of the LASER pump, filter wheel and shutter
- injection of a known charge to calibrate the photodiodes
- measurement of the PMTs and photodiodes signals
- measurement of the time of arrival of the PMTs signals

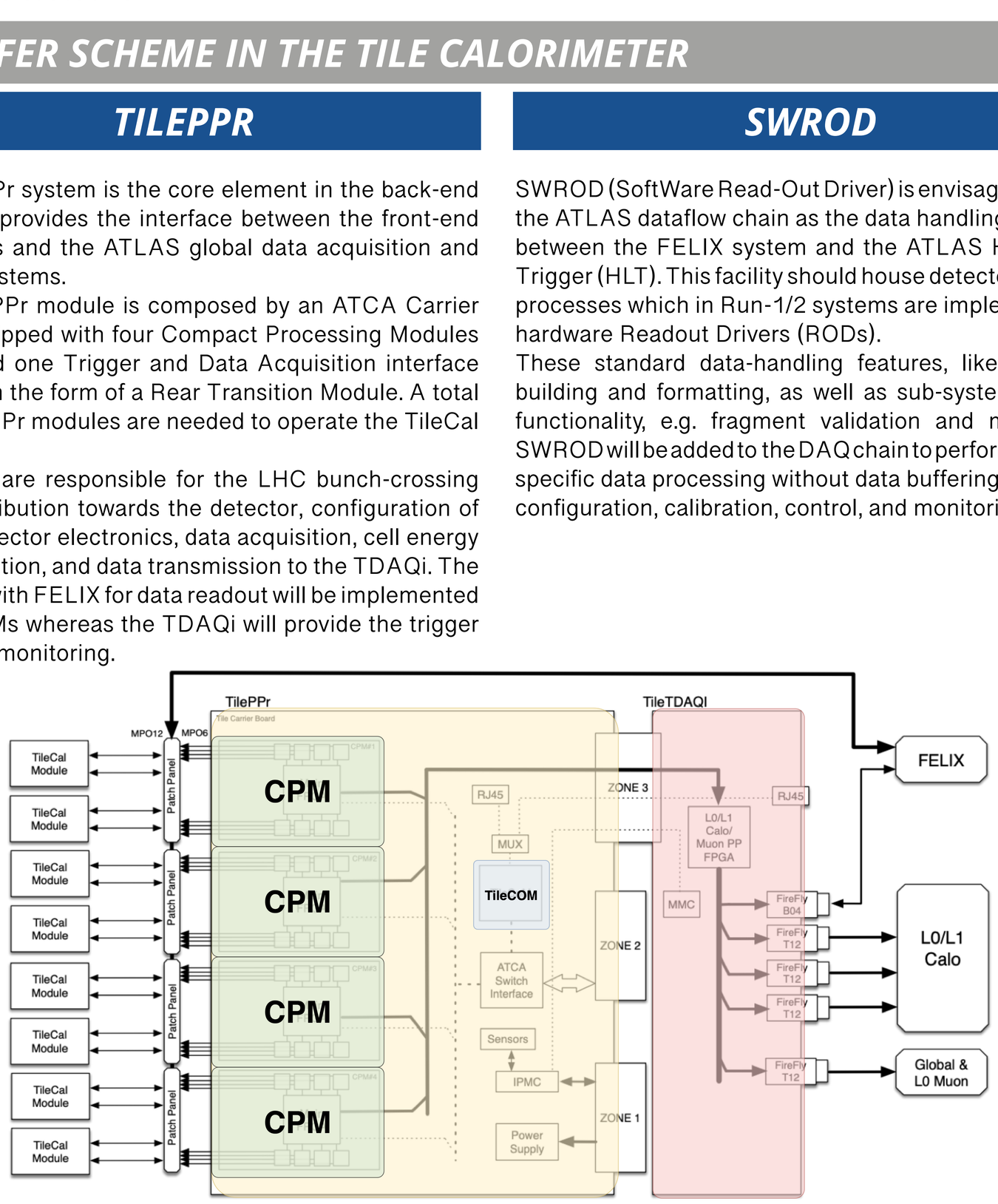
ILANA will transmit data to FELIX at a rate of approximately 1 MHz (L0A rate) while it is provided with the TTC and control signals from FELIX.



Schematic diagram of the ILANA system.

TILEPPR

The TilePPr system is the core element in the back-end system. It provides the interface between the front-end electronics and the ATLAS global data acquisition and triggers systems.
Each TilePPr module is composed by an ATCA Carrier board equipped with four Compact Processing Modules (CPM) and one Trigger and Data Acquisition interface (TDAQi) in the form of a Rear Transition Module. A total of 32 TilePPr modules are needed to operate the TileCal detector.
The CPM are responsible for the LHC bunch-crossing clock distribution towards the detector, configuration of the on-detector electronics, data acquisition, cell energy reconstruction, and data transmission to the TDAQi. The interface with FELIX for data readout will be implemented in the CPMs whereas the TDAQi will provide the trigger primitives monitoring.



Schematic diagram of the PPr system. A complete PPr system is able to process the data from eight Tile super-drawers, consists of an ATCA motherboard blade with four CPMs plus one TDAQi RTM.

SWROD

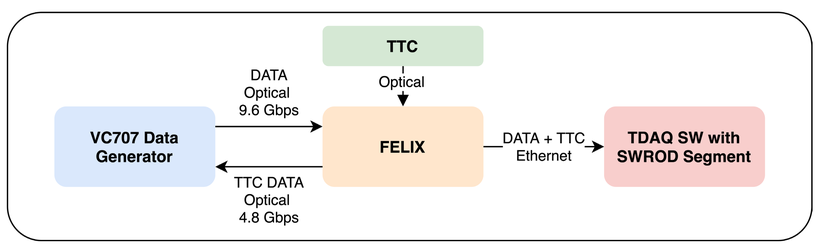
SWROD (SoftWare Read-Out Driver) is envisaged to act in the ATLAS dataflow chain as the data handling interface between the FELIX system and the ATLAS High-Level Trigger (HLT). This facility should house detector-specific processes which in Run-1/2 systems are implemented in hardware Readout Drivers (RODs).
These standard data-handling features, like fragment building and formatting, as well as sub-system specific functionality, e.g. fragment validation and monitoring. SWROD will be added to the DAQ chain to perform detector specific data processing without data buffering, including configuration, calibration, control, and monitoring.

CURRENT WORK

TTC information, Data Integrity Check, and Data Processing Tile Custom functions are being developed for SWROD. This functions will be capable of generating histograms from received data and reconstructed energy. Further integration tests will be done with the first final TilePPr prototype module, which is currently under fabrication, and the FLX-712 in Full Mode. This implementation aims to be ready for the TileCal test beams at the SPS later this year.

TEST BED

Our test bed is composed of a TilePPr Demonstrator module that feeds the Mini-FELIX with pseudorandom generated data. The Mini-FELIX is a prototype version of the FELIX board based on a commercial Xilinx VC709 with a custom TTCfx mezzanine card used to connect the FELIX card to the ATLAS TTC system.
SWROD is integrated into the official ATLAS TDAQ Software adapted to the testbed configuration.



Schematic diagram of the current test bed.

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