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Development of new high speed data acquisition system prototype for SOI pixel detector using 10 Gb Ethernet SiTCP

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The SOI (Silicon-On-Insulator) pixel detector is the monolithic imaging device developed by the SOIPIX group led by KEK. This detector is being tested for practical use such as X-ray imaging, but the readout FPGA (Field-Programmable Gate Array) board SEABAS2 (Soi EvAluation BoArd with Sitcp 2), which is mainly used for the readout of this detector is becoming obsolete. This has led to problems such as insufficient readout speed, restrictions on the implementation of advanced processing due to the insufficient circuit scale of the FPGA. Therefore, in order to improve the performance and usability, we are developing the new readout board with newer generation FPGA and 10 GbE SiTCP (10 Gigabit ethernet network processor library logic circuit running on FPGA). Prior to the development of new board, we constructed a prototype system using the FPGA evaluation board KC705 to evaluate the 10 GbE SiTCP. We will report this prototype system's evaluation.

TIPP2020 abstract resubmission?

No, this is an entirely new submission.

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