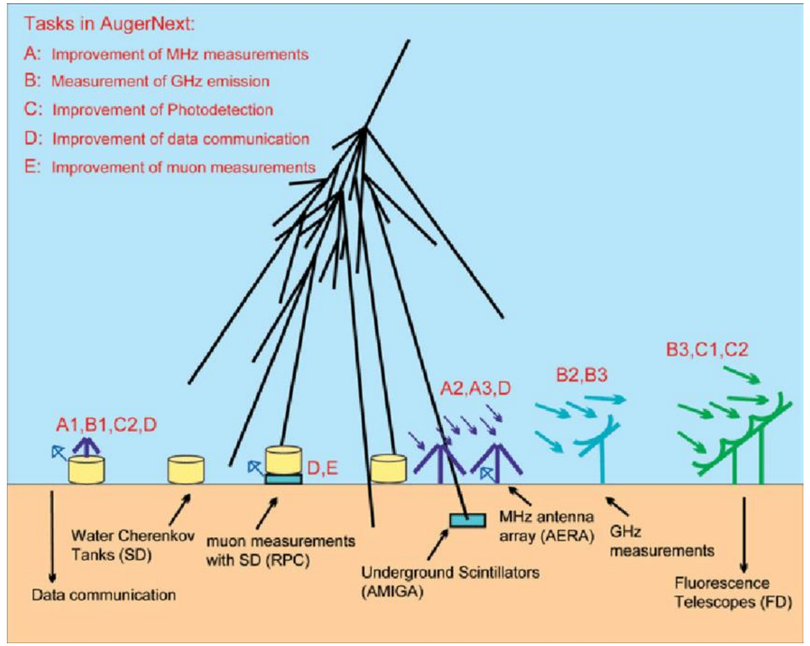
# The GRANDProto300 antenna and acquisition board

by: Rene Habraken

*~ FPGA programming and hardware design*

# AERA
## – *Auger Engineering Radio Area*

Installment in May 2013 in Argentina
150 antennas
17 km2

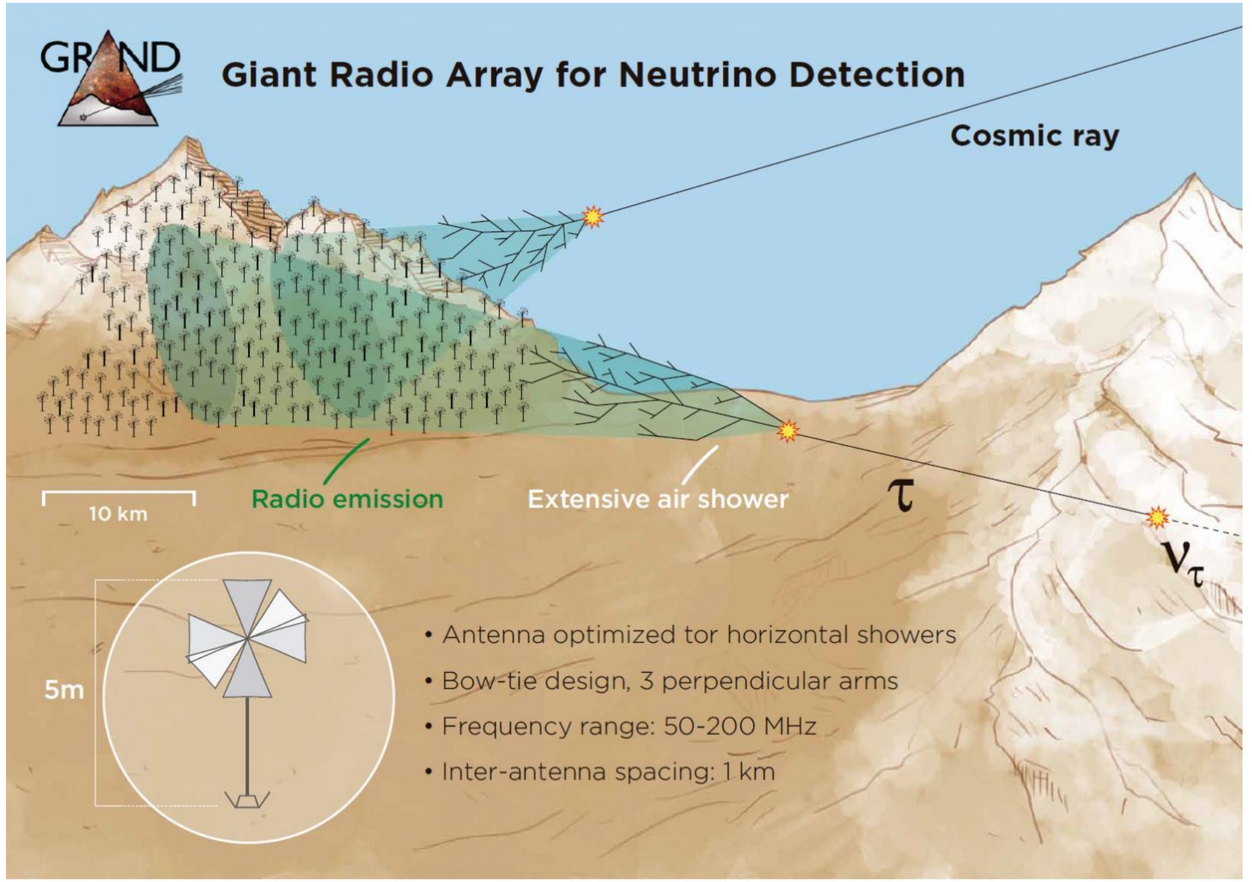



# GRAND – Giant Radio Array for Neutrino Detection

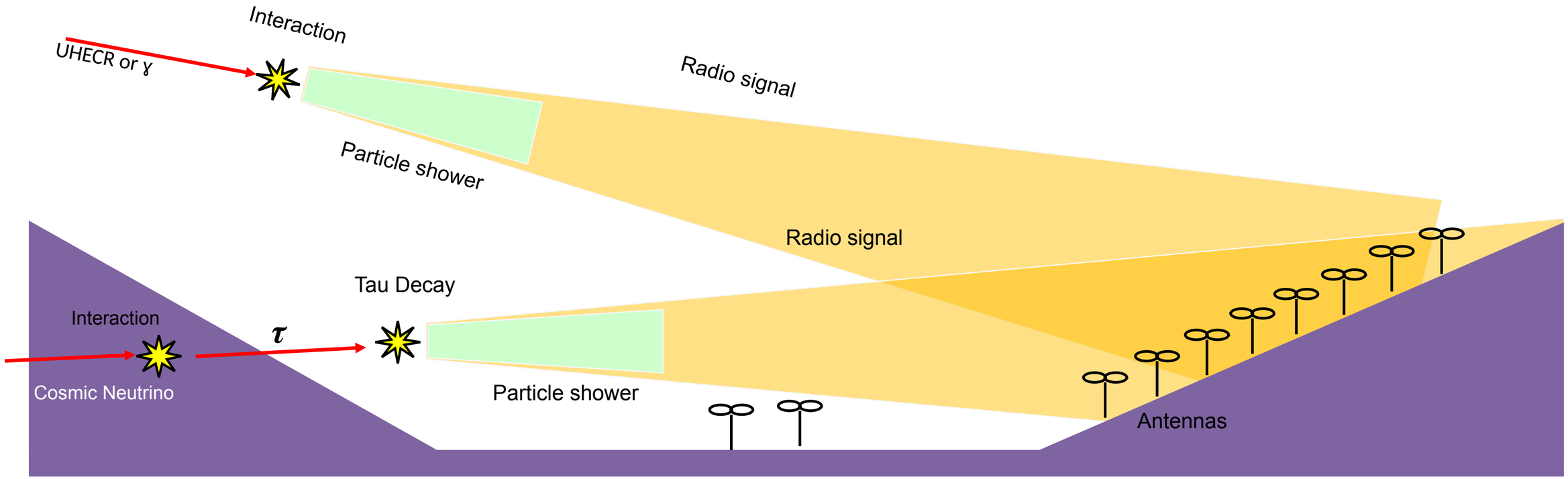
The GRAND collaboration consists of:
~80 collaborators from 11 countries

Goal is to detect neutrinos and UHECR using several arrays of 10.000 antenna stations each. These arrays will be placed on a number of remote places on the planet. Final goal is to end up with ~20 sub-arrays covering over 200’000 km$^2$.

Currently GRANDproto300 is under development and the first 100 stations will be installed this summer in central-west China.

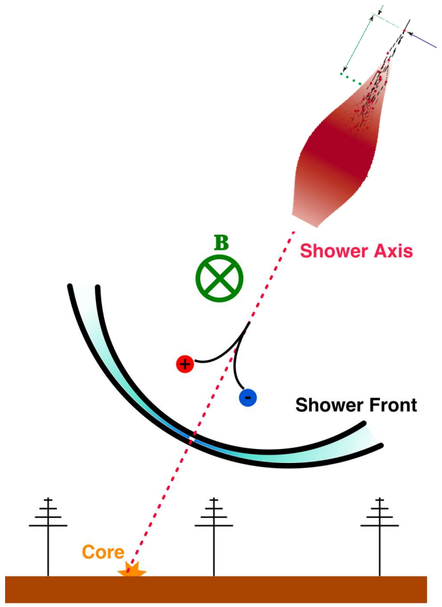


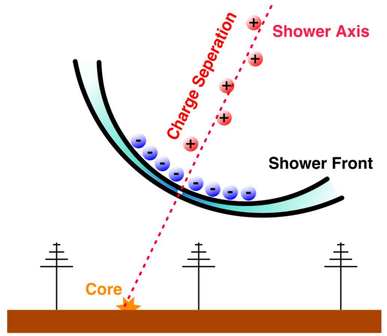
# Detection Principle for EeV (and beyond!) particles



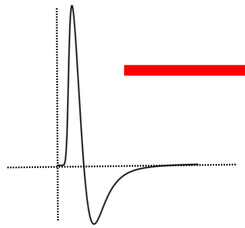

Giant Radio Array Neutrino Detector
GRAND

# Radio detection of air showers

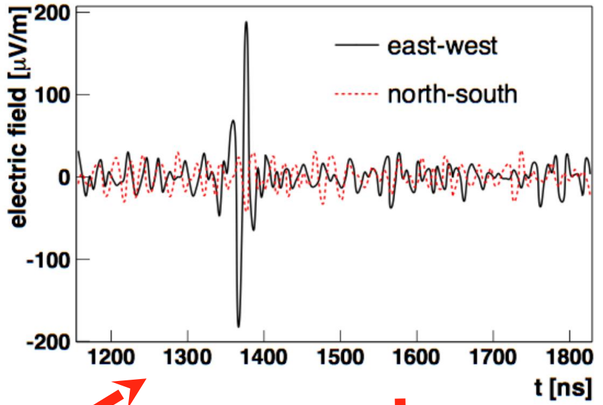


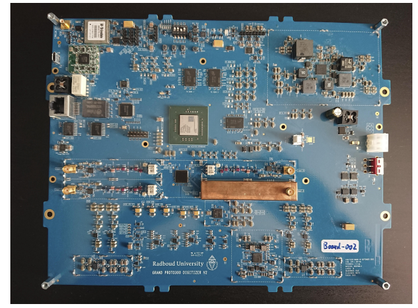




Short Pulse
(~100ns)



antenna
(30-200 MHz)



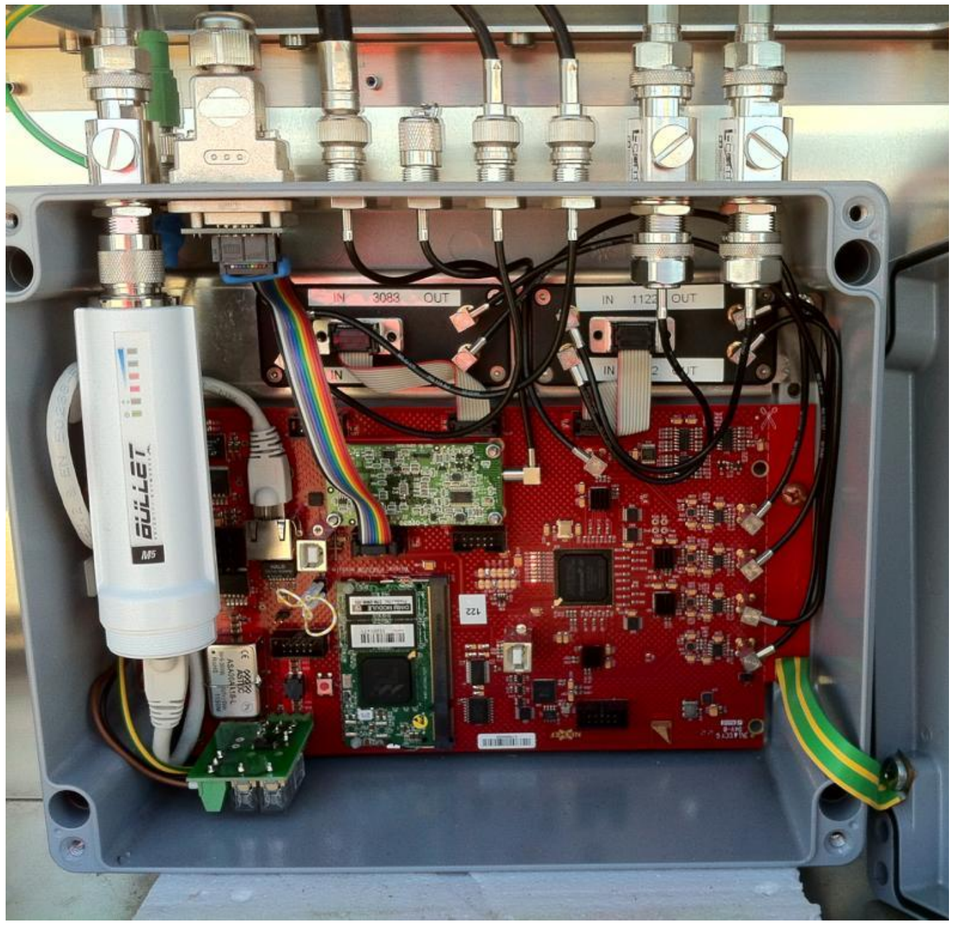



# What challenges had to be solved for GRAND?

- Increase measurement bandwidth from 30 - 80 MHz to 30 – 200 MHz and the resolution from 12 to 14 bit.
- Increase data throughput between FPGA and CPU
- Make the station more reliable
- Study trigger on the radio signal
- Prevent saturation of ADC
- Increase the monitoring of the direct environment around the antenna stations
- Use less power
- Make the station cheaper

… with less resources :-)

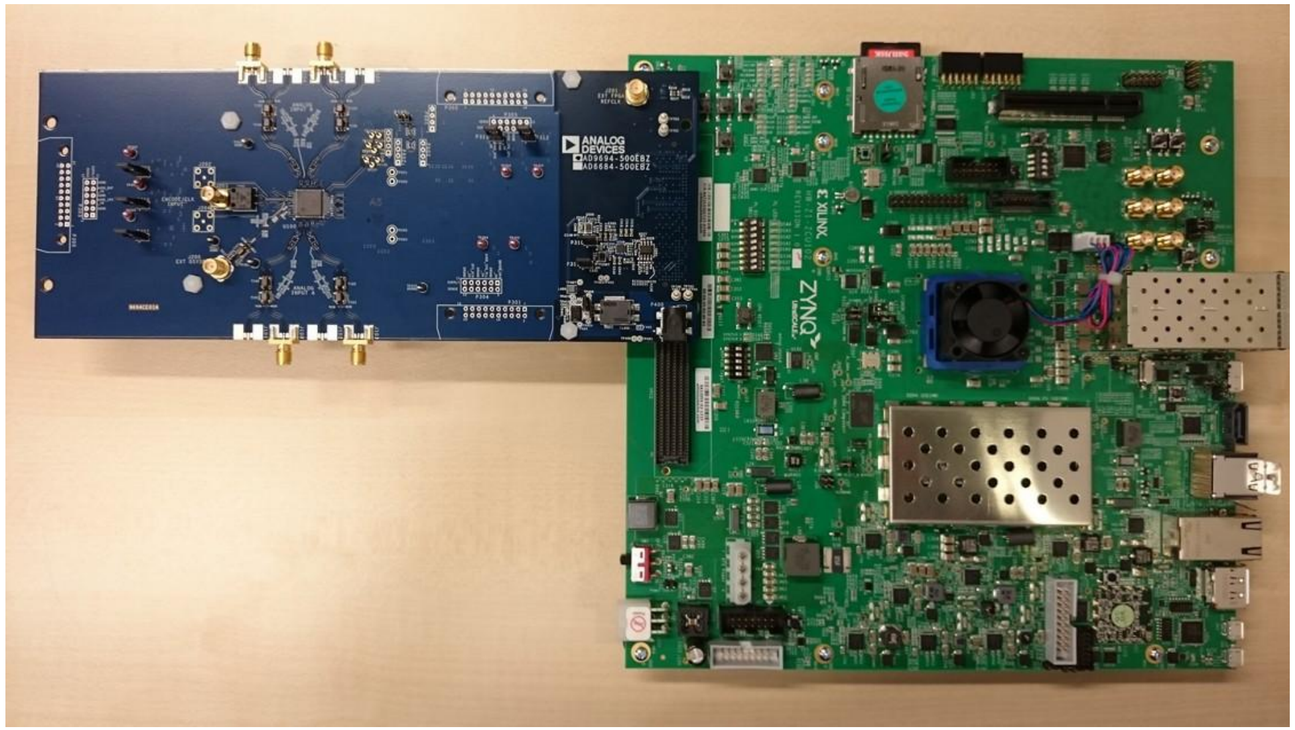
This should make way for new physics!




12bit, 200MHz digitizer for AERA

# Merge Analog Devices with Xilinx reference design

Analog Devices
ad9694-500ebz
reference board




Xilinx ZCU102
reference board

Both companies provide schematics, BoM, board layout

# GRAND prototype V2

**Key features DAQ**

Digitize, buffer and transmit signals measured on the 4 inputs via a long range WiFi data channel.

Xilinx Ultrascale Zynq FPGA with (among other features) an integrated dual core ARM processor

4 input channels

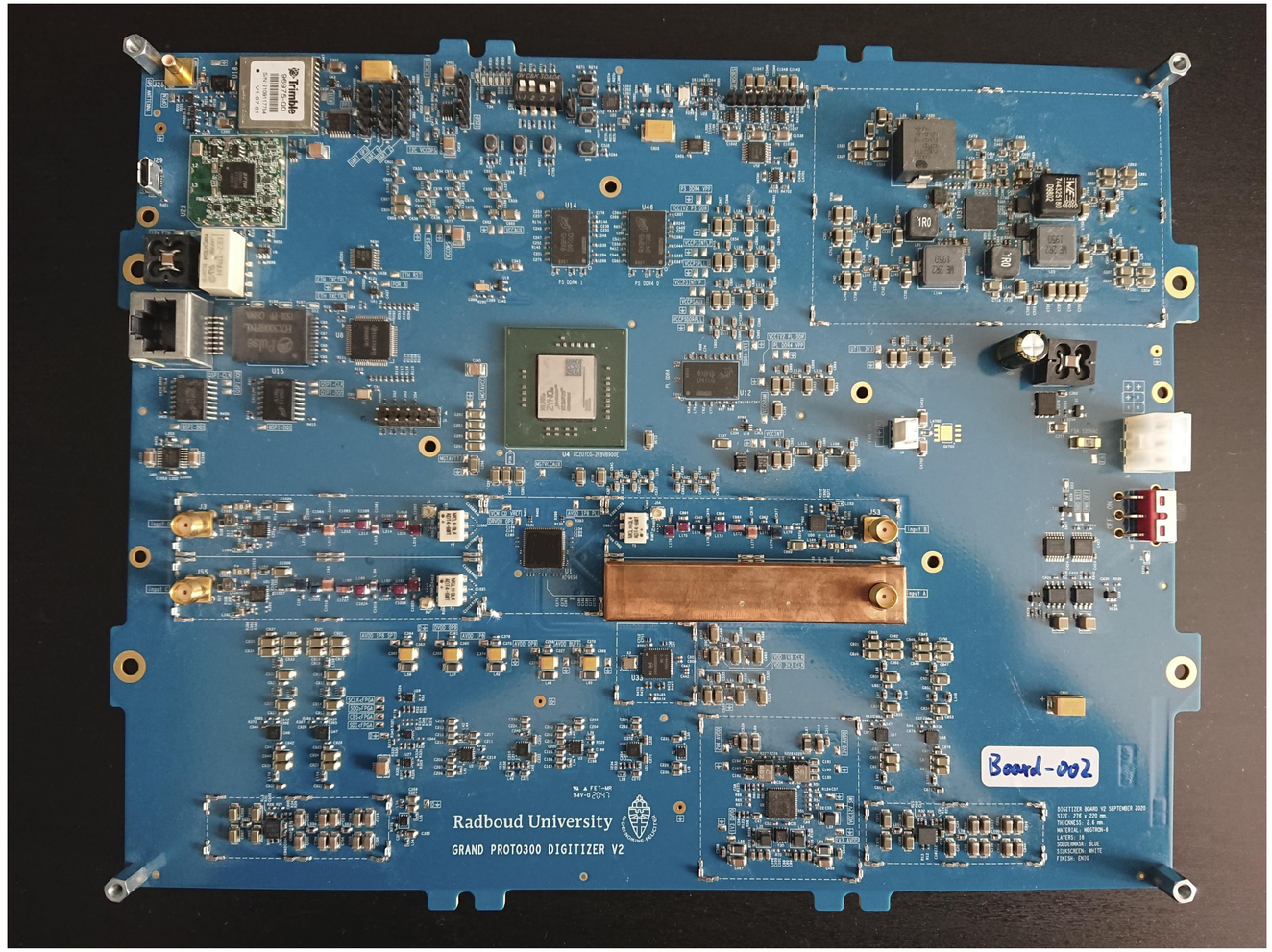
14 bit, 500MSPS ADC

30 – 200 MHz

GPS for position and accurate timing

Long range WiFi data transfer

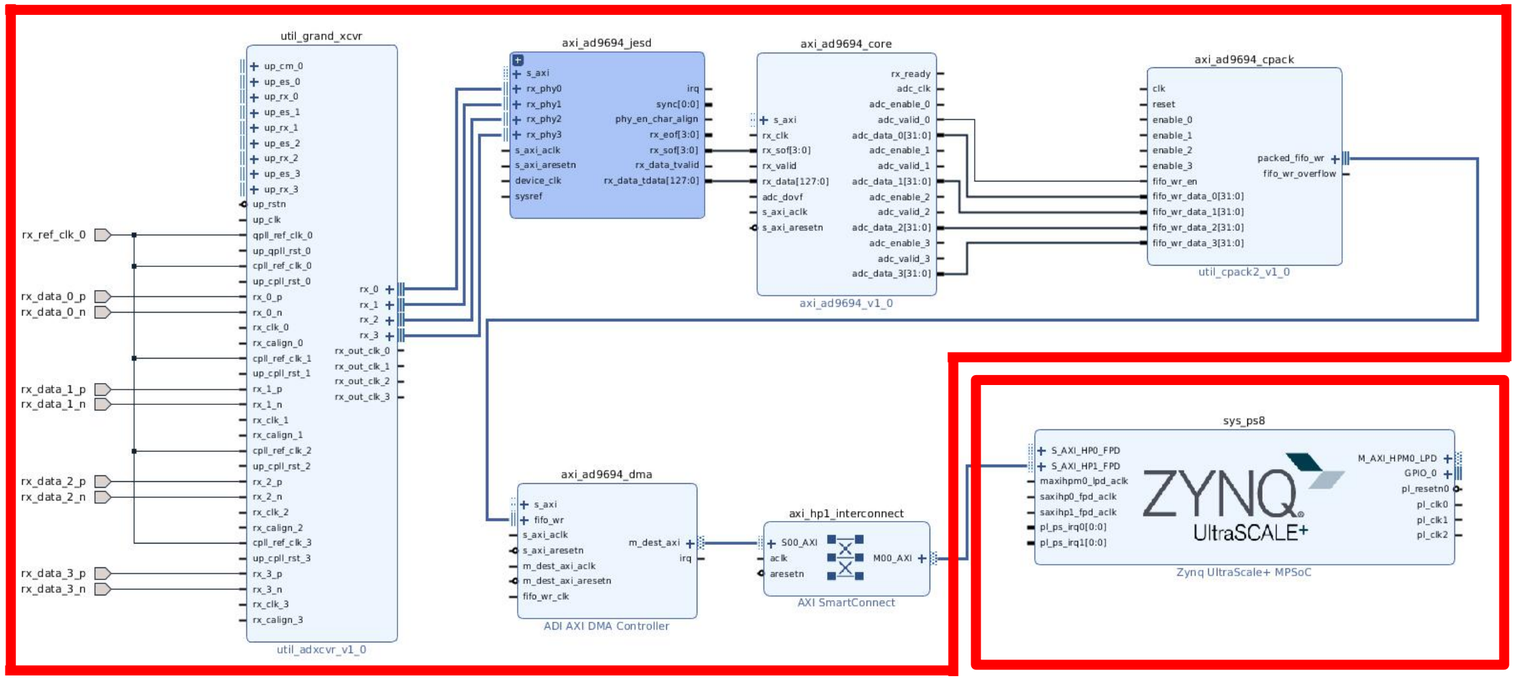
16 W total power consumption

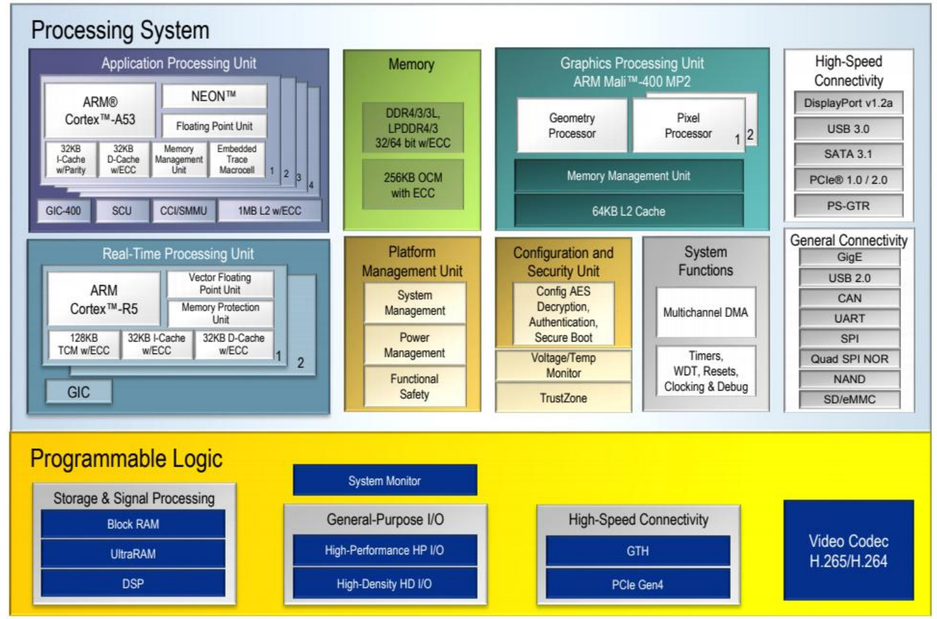


# Xilinx ZYNQ Ultrascale+ FPGA

- Implement ADC readout, trigger logic and event building in Programmable Logic (PL).
- Running Linux on Processor System (PS)
→ **lower power consumption and high speed interface (2.4GB/s) from PL to PS**

```
/*
 * dts file from: FMCDAQ3 on Xilinx ZynqMP ZCU102 Rev 1.0
 *           to: GRANDproto_v1 Xilinx ZynqMP ZU7CG Rev 1.0
 *
 * Copyright (C) 2018 Analog Devices Inc.
 * Modified by R. Habraken: Radboud University Nijmegen
 *
 * Licensed under the GPL-2.
 */

/* i2c and axi-bus*/
```





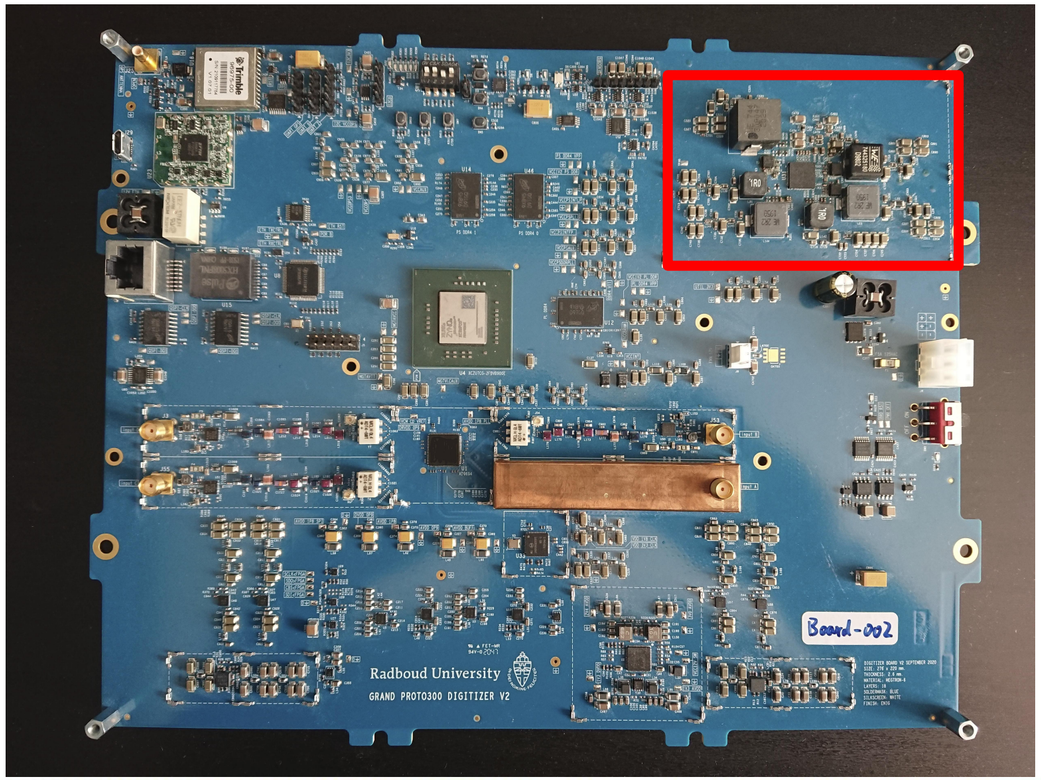

XILINX ALL PROGRAMMABLE


Radboud University

# Use less power: Single power management IC provides all the voltage rails for the FPGA

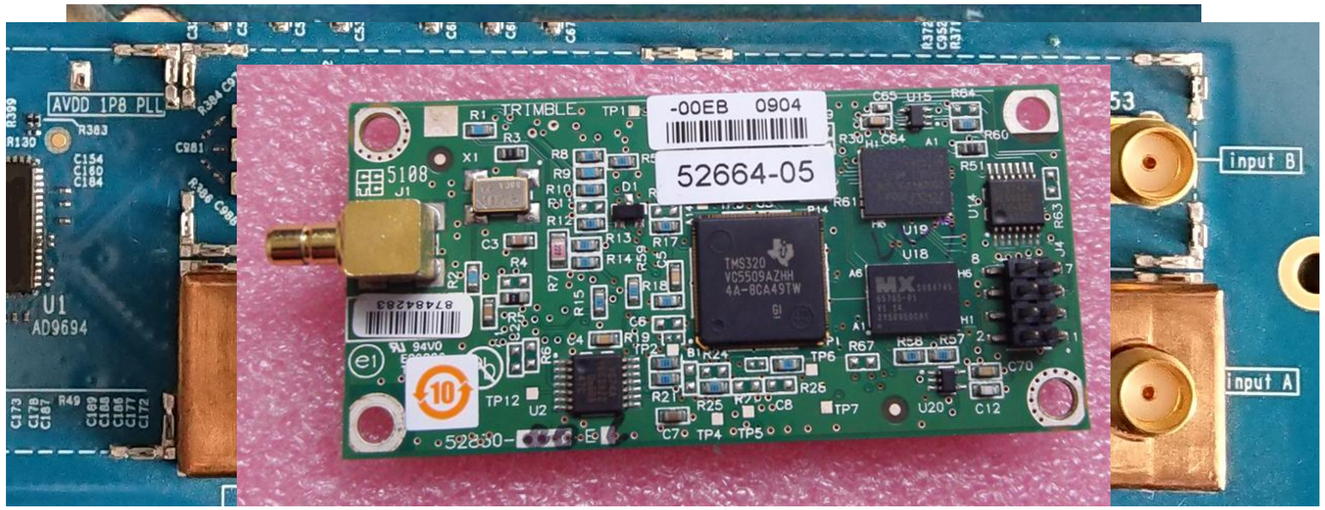
Reduced power by 8W compared to the Xilinx ref design.
Controllable in Linux via I2C communication

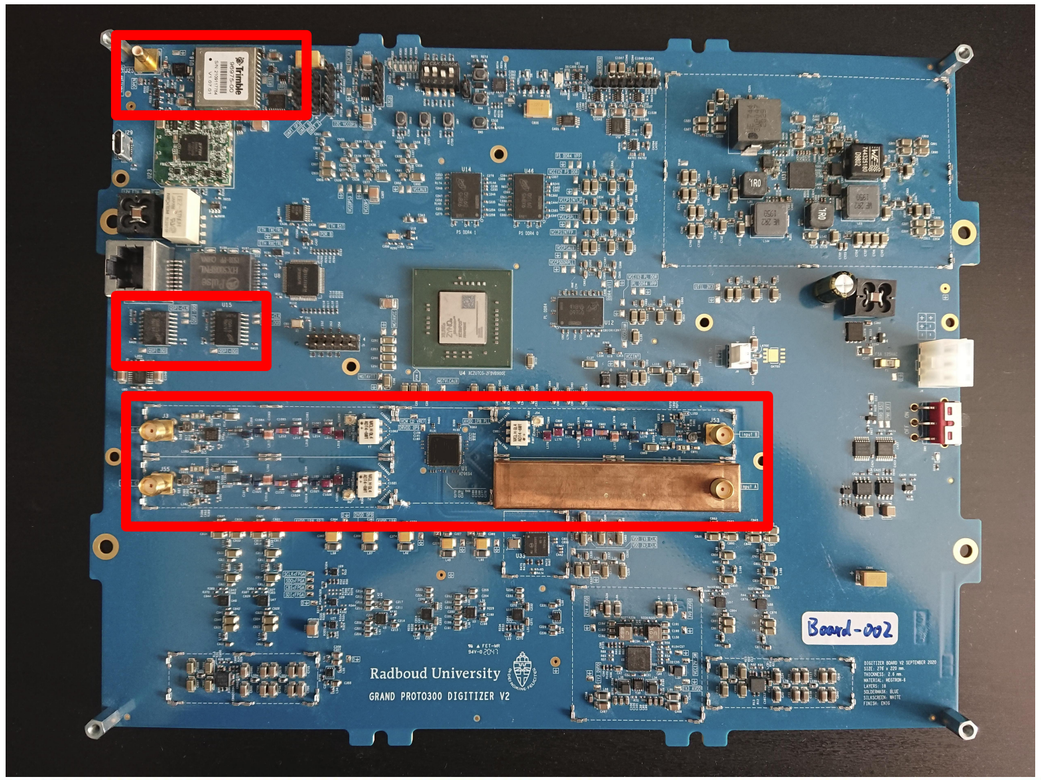
```
    pmic: tps65086@5e {
        compatible = "ti,tps65086";
        reg = <0x5e>;
        interrupt-parent = <&gpio>;
        interrupts = <77 GPIO_ACTIVE_LOW>;
        #gpio-cells = <2>;
        gpio-controller;

        regulators {
            ldoa2 {
                regulator-always-on;
            };
        };
    };
};
/*END I2C0 BUS */
```



# Make it more reliable: Reducing the connectors

GPS circuit mounted on board
Removed SD card and use flash storage for bootloader, bitfile and Linux image
Added the frontend to the board design (i.s.o. separate modules connected with cables)



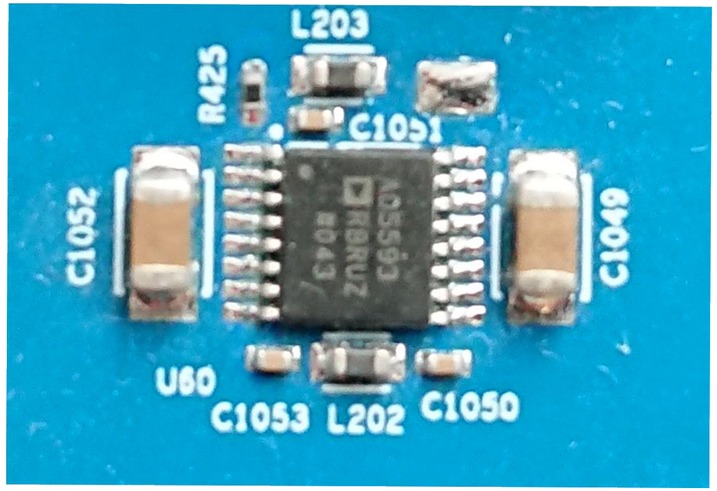
# Prevent saturation of the ADC's

React to noisy (or clean!) RFI background and prevent saturation with an variable gain amplifier (-12 dB to +22 dB):

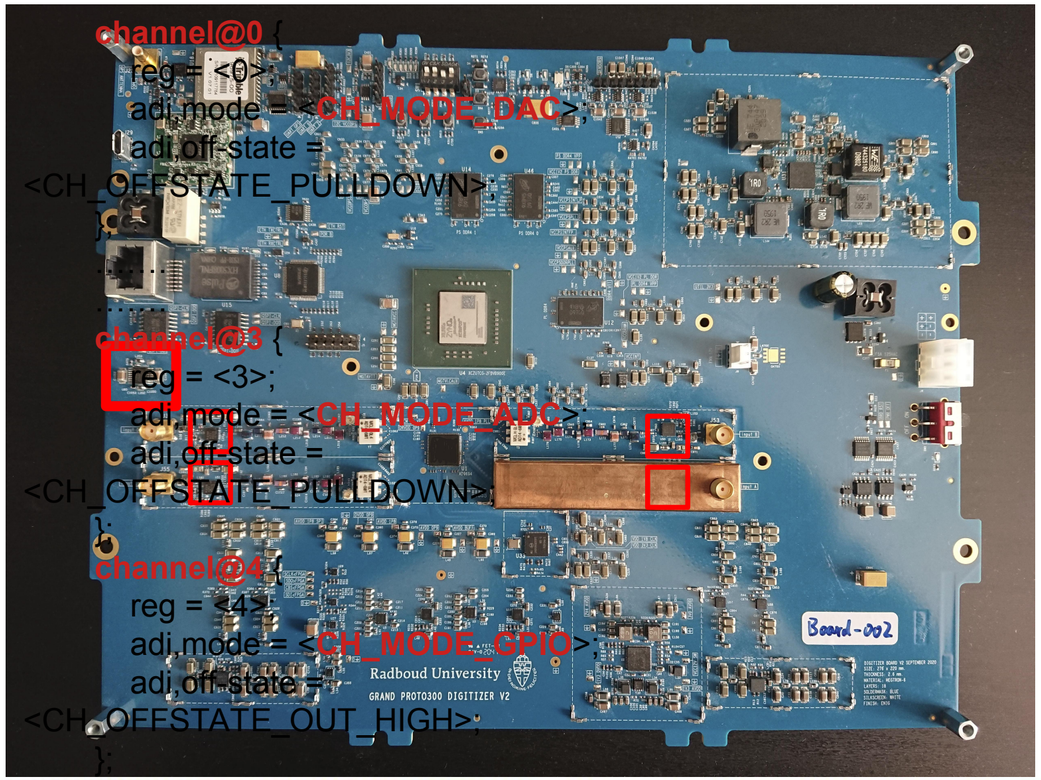
→ AD8368

At run time the gain can be set from the Linux OS with the general purpose chip that can be configured as an ADC, DAC or GPIO:

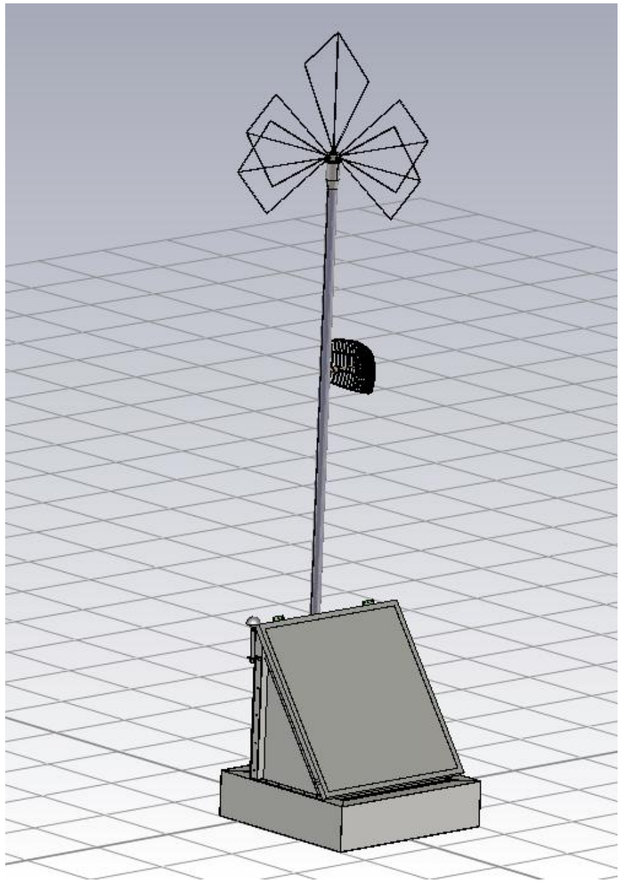
→ AD5593

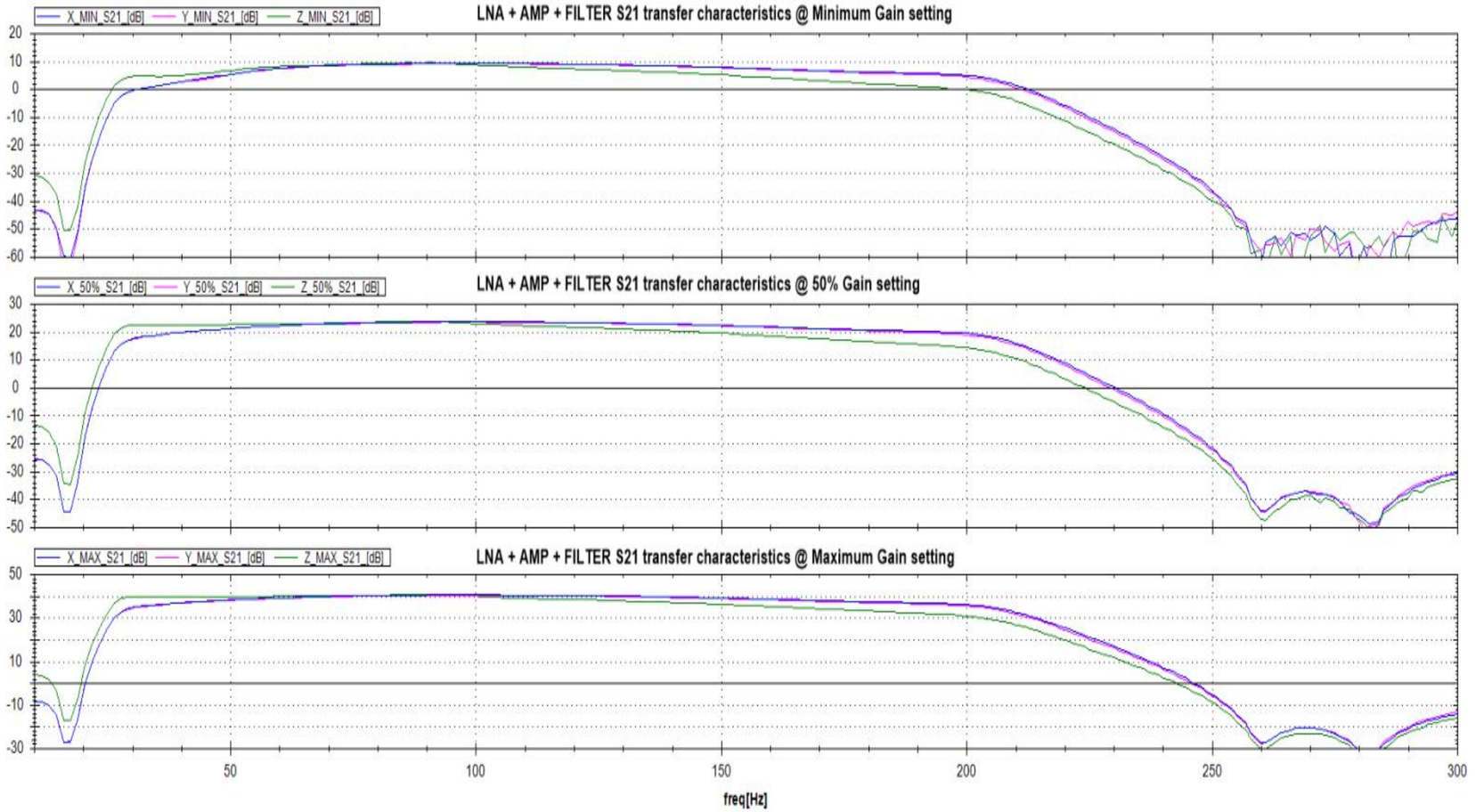



```
/* AD5593 GPIO - ADC - DAC | U60 */
ad5593r@11 {
    compatible = "adi,ad5593r";
    reg = <0x11>;

    channel@0 {
        reg = <0>;
        adi,mode = <CH_MODE_DAC>;
        adi,off-state =
<CH_OFFSTATE_PULLDOWN>;
    };
    ......
    channel@3 {
        reg = <3>;
        adi,mode = <CH_MODE_ADC>;
        adi,off-state =
<CH_OFFSTATE_PULLDOWN>;
    };
    channel@4 {
        reg = <4>;
        adi,mode = <CH_MODE_GPIO>;
        adi,off-state =
<CH_OFFSTATE_OUT_HIGH>;
    };
```



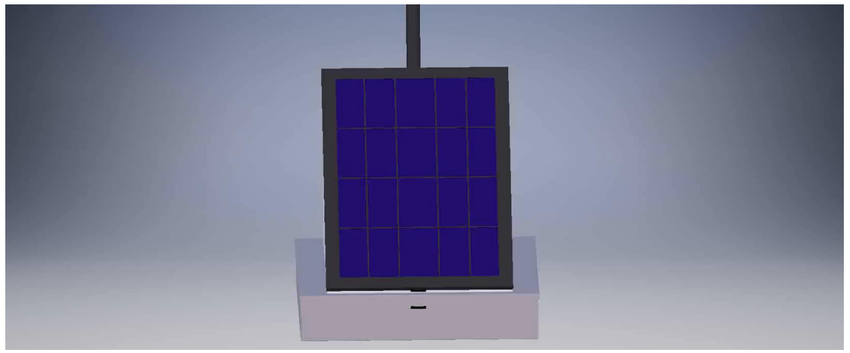
# Antenna simulations and front-end measurements





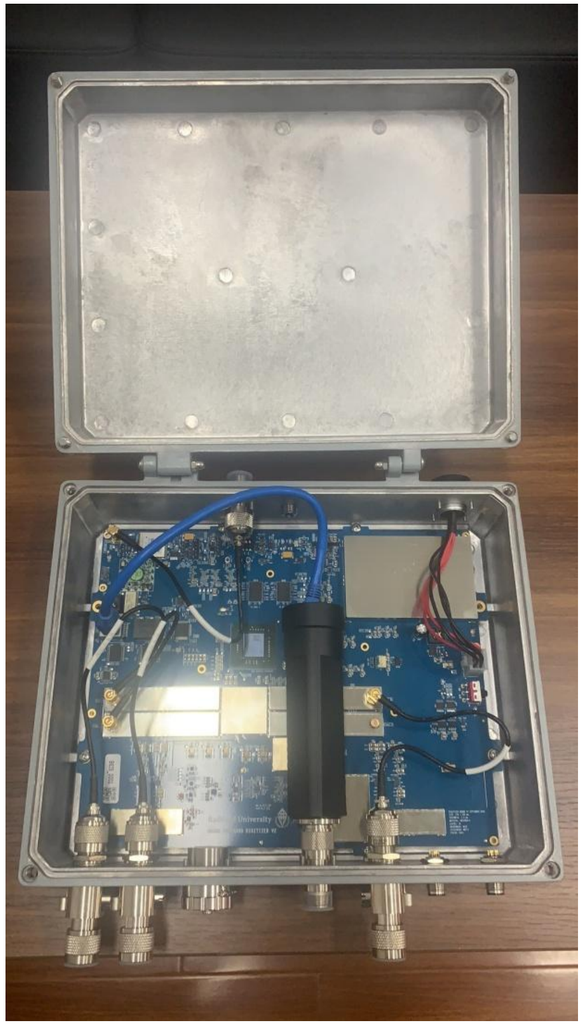
# Increase the environmental monitoring: added sensors


Environmental sensors in the top of the 3 m high pole for:
- Movement
- Air pressure
- Temperature
- Relative Humidity



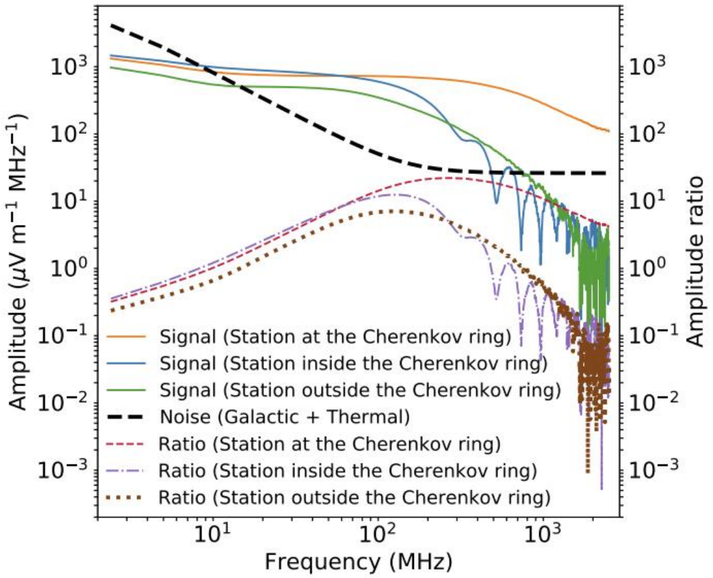
Robust mechanical design: In strong winds (wind force 11) the movement of the top is below 0.5 degrees

# RF tight enclosure

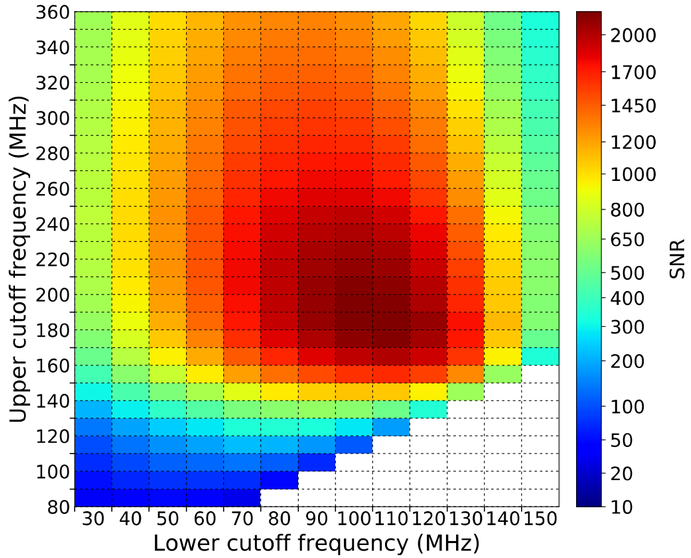



# How does this result in new physics?

- Moving the measurement bandwidth up to 200MHz results in a higher SNR, allowing a lower measurement threshold and increases the overall sensitivity of the radio array. Maximizing the chance of detecting neutrino's
- Maintaining a low group delay in the measurement band results a better pulse shape. This allows for a better characterization of the Cherenkov cone.
- A larger bandwidth prepares us for timing resolution below 10ns.




(a) Thermal noise = 300 K

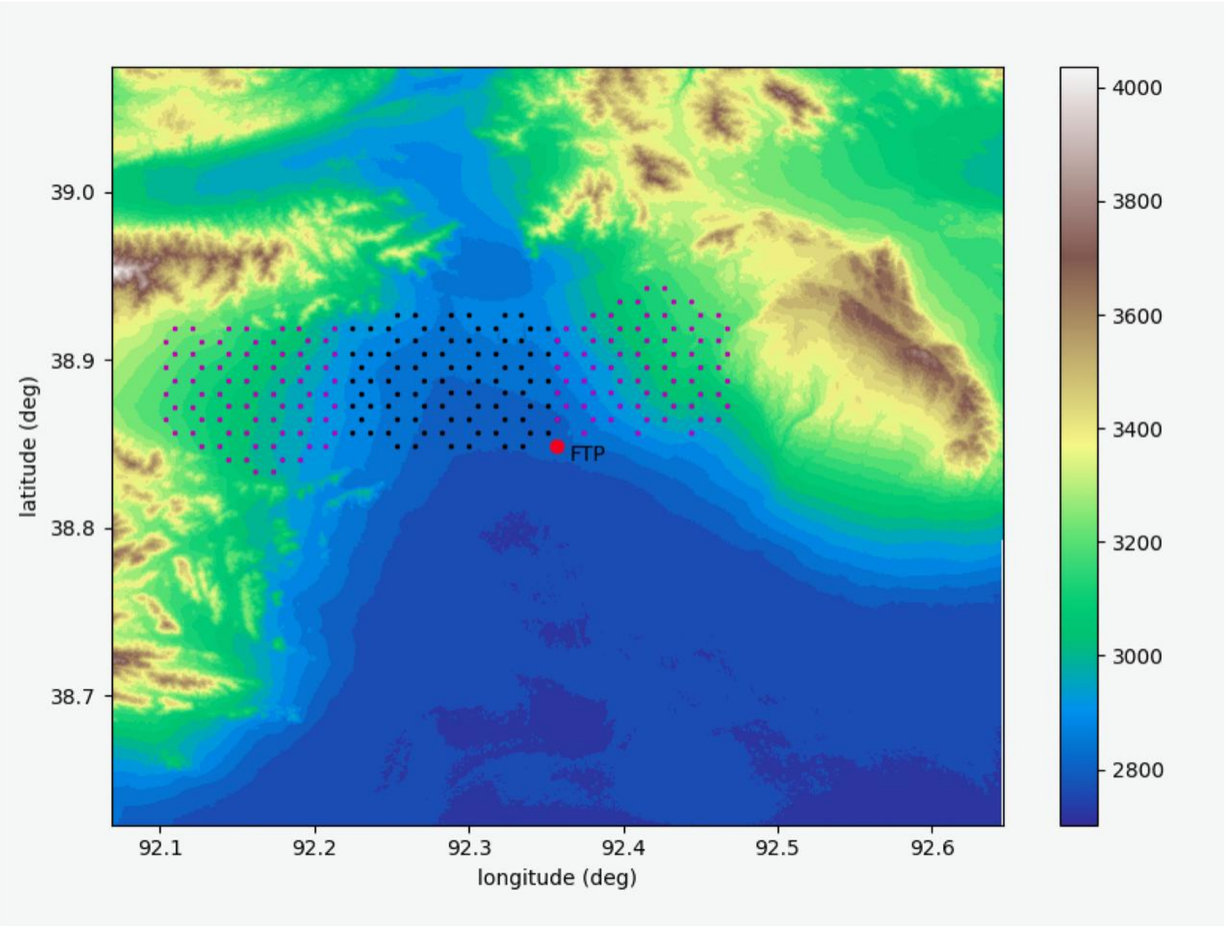



(a) IceTop: Thermal noise = 300 K
Balagopal et al PoS ICRC2019 (2020) 184

## Near future:

- Test and assembly of the first 100 antenna stations.
- Installment of 100 antennas in a remote area in the Qinghai province (west-central China)
- Trigger implementation in firmware
- Continuous FFT in FPGA

Then there is a lot of work to do to go to 1000, 10.000 and 200.000.




Layout antenna array GRANDProto300

# Next version of the board | Future

- Cost reduction (electronics board, connectors)
- Improve scalability of the antenna array.
- Lower power consumption by improving LNA design and changing the communication to the central DAQ.

**Meet physics goals with a minimum impact on the environment.**

**→ First analysis of the environmental impact of our activities: arXiv:2101.02049**

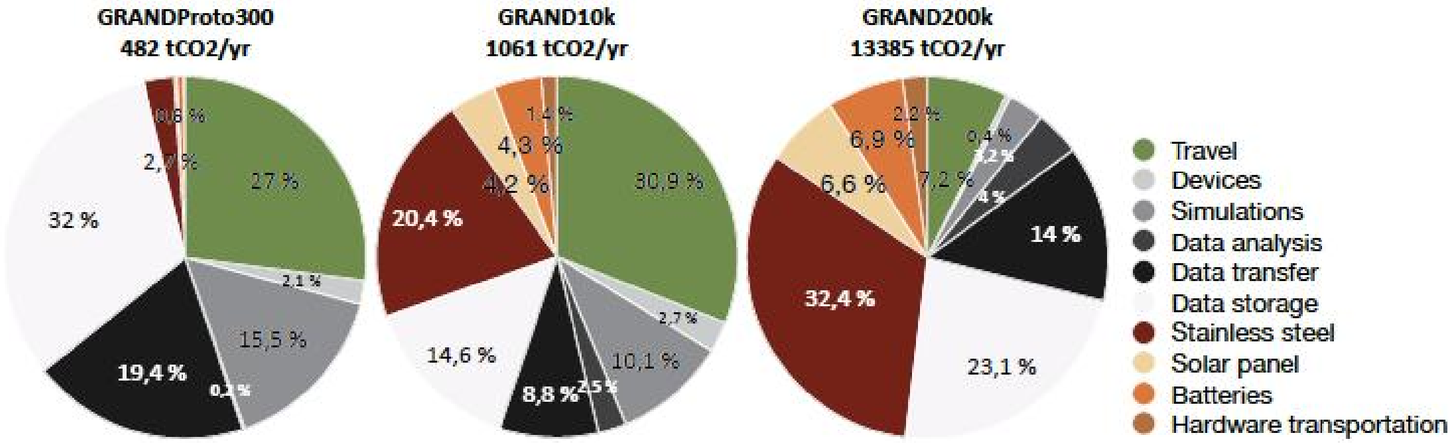



Figure 11: Projected distribution of GHG emissions for all sources for GRANDProto300, GRAND10k and the full GRAND array. The title indicates the total amount of emissions per year due to each source at each experimental stage.

# Thanks!