Development of a hybrid single-photon imaging detector with embedded CMOS pixelated anode

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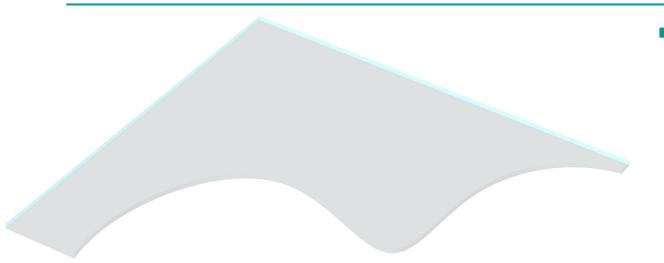




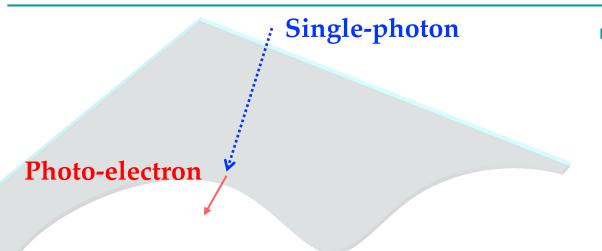


- A detector was proposed based on a "hybrid" concept:
 - Vacuum detector
 - Photocathode with high QE in the spectral region of interest
 - Proximity-focusing geometry
 - Micro-channel plate (MCP) amplification
 - Silicon ASIC embedded inside vacuum tube
 - Reference:
 - JINST 13 C12005 2018

Timing resolution	A few 10s ps
Position resolution	5-10 μm
High rate capability	$10^9\mathrm{hits/s}$
Very low dark count rate at room T	10^2 counts/s
Large active area	7 cm ²
High channel density	0.23 millions

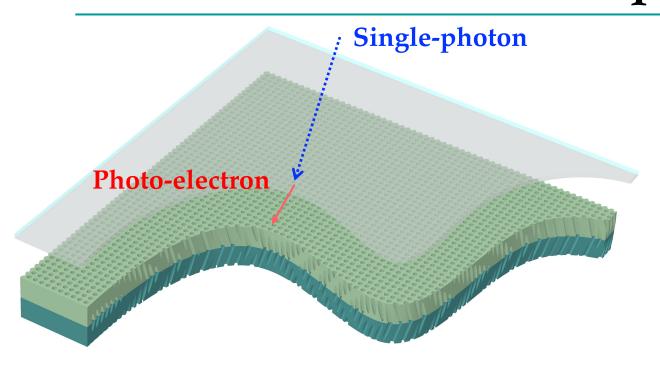


Entrance window + photocathode

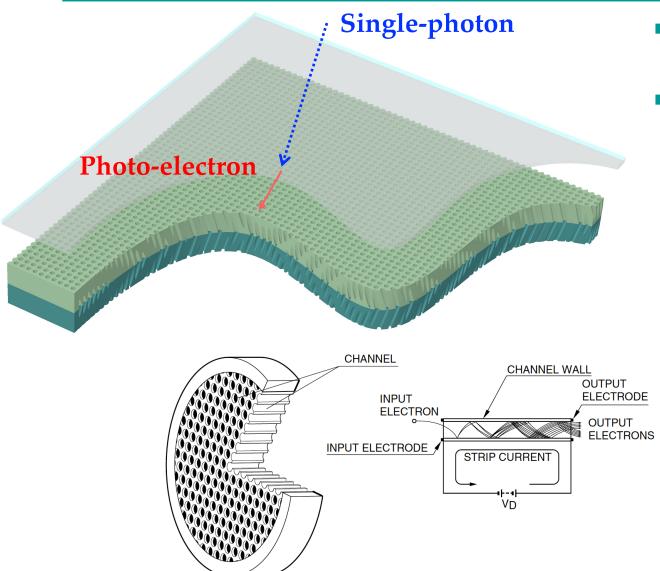


- Entrance window + photocathode
 - Photon conversion
 - E.g. bialkali photocathode
 - 40-50% QE (Quantum Efficiency)
 - 10² Hz dark count rate at room temperature
 - Best for timing
 - Flexible design allows to use different photocathodes

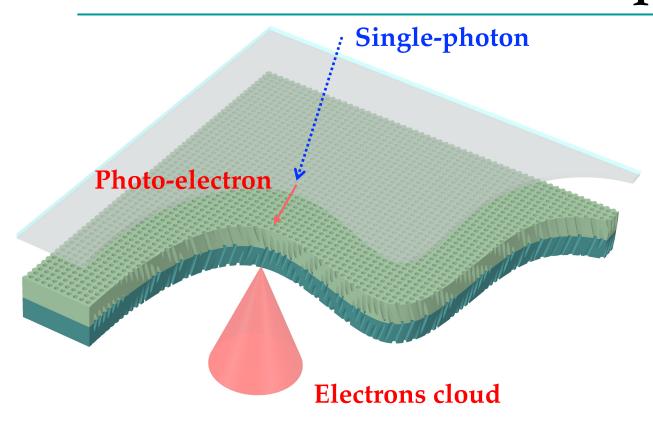
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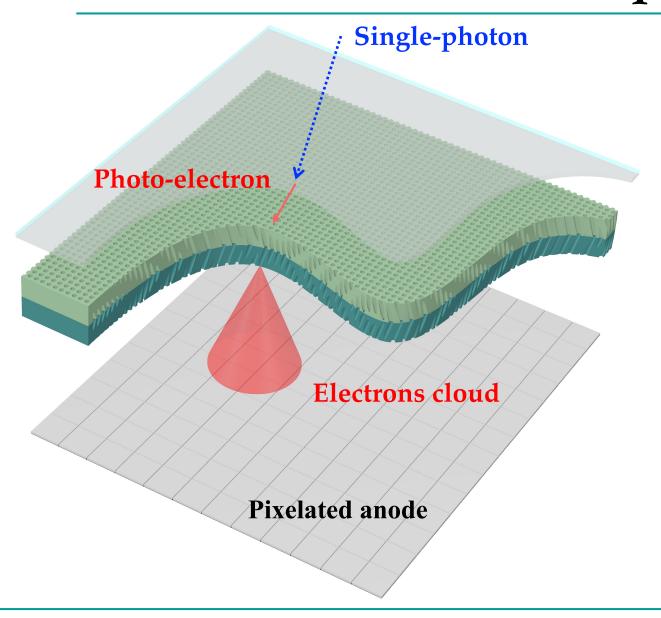
- Entrance window + photocathode
- Microchannel plate stack (chevron)
 - □ A few 10⁴ gain
 - 5 μm pore size
 - Atomic layer
 deposition for
 increased lifetime
 >20 C/cm²
 - Short distance from MCP to cathode and anode for best time and position resolution



- Entrance window + photocathode
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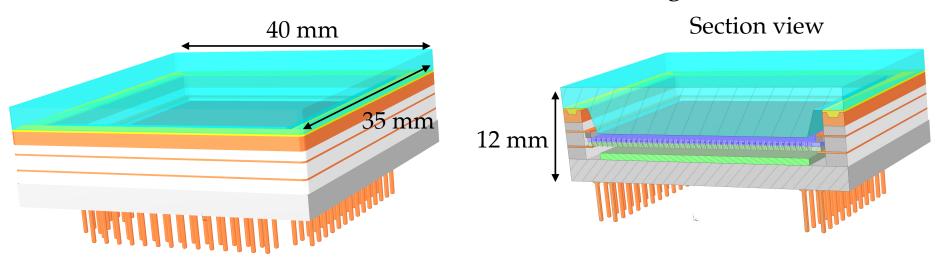
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- Entrance window + photocathode
- Microchannel plate stack (chevron)
- Pixelated anode
 - Electron cloud spread over a number of pixels
 - 55μm × 55μm pixel size
 - 0.23 M pixels
 measuring arrival
 time and duration
 of input signals
 - □ 7 cm² active area
 - □ Up to 2.5 Ghits/s
 - Local signal processing

Photodetector assembly

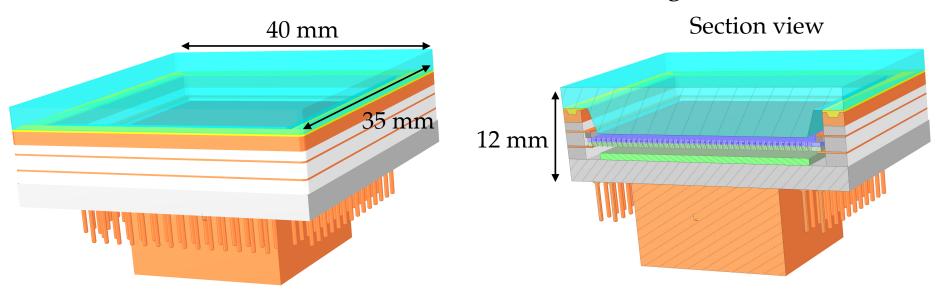
3D structure: detector rendering



- Vacuum-based detector
 - Assembly of many components under high vacuum (10⁻¹⁰ mbar)
 - High-speed connections through pins in ceramic carrier board

Photodetector assembly

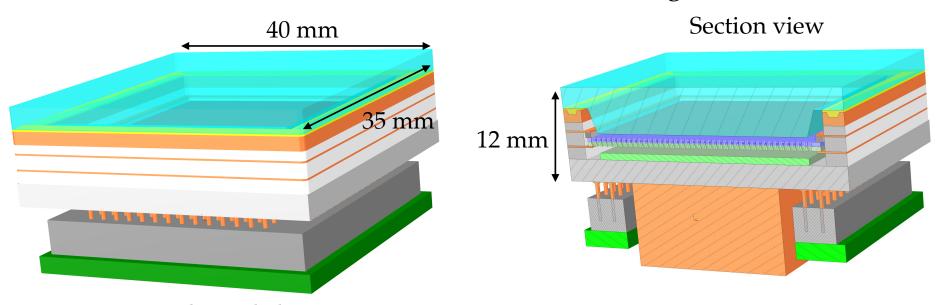
3D structure: detector rendering



- Vacuum-based detector
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- Heat sink for stable detector operation (heat removal)

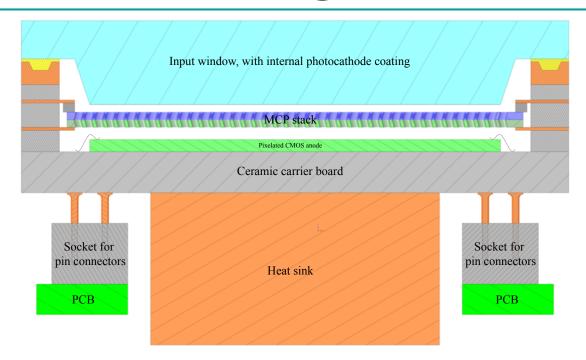
Photodetector assembly

3D structure: detector rendering



- Vacuum-based detector
 - Assembly of many components under high vacuum (10⁻¹⁰ mbar)
 - High-speed connections through pins in ceramic carrier board
- Heat sink for stable detector operation (heat removal)
- Carrier printed circuit board (PCB)
 - Socket for detector pins, regulators and high voltage
 - Connected to FPGA-based read-out and DAQ via 16 × 10Gbps links

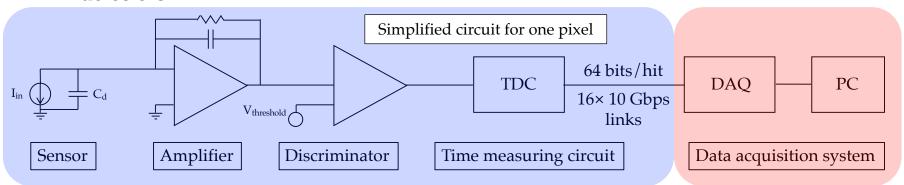
Detector geometry



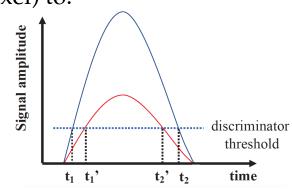
- Shortest photocathode-to-MCP distance preserves impact position information
- Optimized MCP-to-anode distance spreads the electron cloud over a number of pixels

Pixelated anode

- Timepix4 ASIC in 65nm CMOS silicon pixel technology
 - Cutting-edge development funded by the Medipix4 Collaboration for hybrid pixel detectors



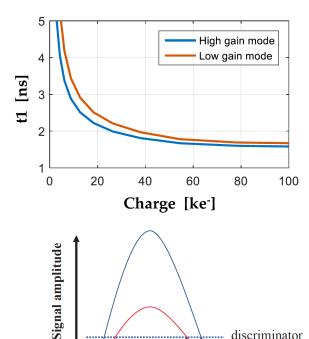
- Measures arrival time (t_1) and Time-over-Threshold $(ToT=t_2-t_1)$ in every pixel
 - □ Time-to-Digital Converter (TDC) bin size: 195 ps (56 ps rms resolution per pixel)
- Electron cloud spread over a number of pixels → cluster
- Use ToT information (proportional to the charge in a pixel) to:
 - Correct for time-walk effect in every pixel
 - Improve position resolution by centroid algorithm
 - Go from $55\mu\text{m}/\sqrt{12}\sim16\mu\text{m}$ down to $5\mu\text{m}$
 - Improve timing resolution by multiple sampling
 - Many time measurements for the same photon \rightarrow few 10s ps
- High data rate capability (up to 160 Gbps)



The Timepix4 ASIC (1)

- Charge amplifier, single threshold discriminator and TDC based on Voltage Controlled Oscillator
 - 5 ns peaking time, ToT ~200 ns for 10 ke⁻ charge, 175 ns digitization time → total dead time per pixel <400 ns
 - Data driven architecture: 2.5 Ghits/s maximum rate

Technology			CMOS 65 nm	
Pixel Size			55 μm × 55 μm	
Pixel arrangement			4-side buttable 512×448 (0.23 Mpixels)	
Sensitive area			$6.94 \text{ cm}^2 (2.82 \text{ cm} \times 2.46 \text{ cm})$	
Read-out Modes	Data driven	Mode	TOT and TOA	
		Event Packet	64-bit	
		Max rate	358 Mhits/cm ² /s	
TDC bin size			195 ps	
Readout bandwidth		th	≤163.84 Gbps (16× @10.24 Gbps)	
Equivalent noise charge		harge	50-70 e⁻	
Target global minimum threshold		mum threshold	<500 e⁻	



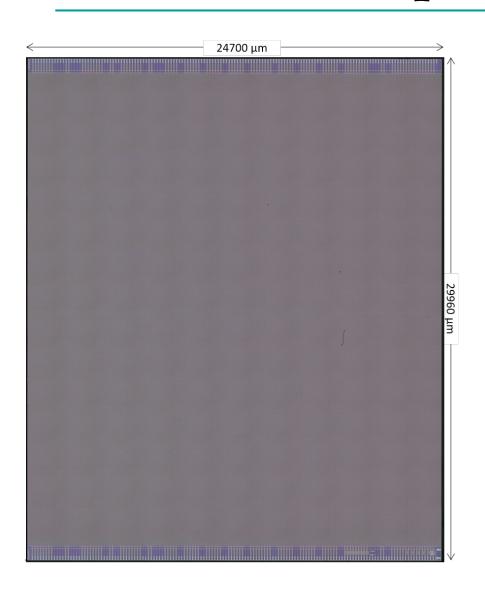
 t_1 t_1

 t_2 , t_2

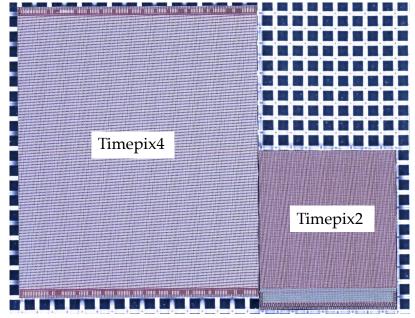
discriminator threshold

time

The Timepix4 ASIC (2)



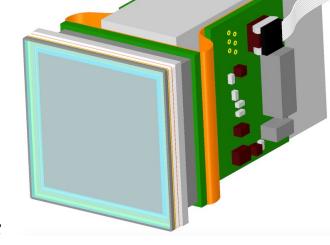
- 65 nm CMOS (TSMC)
- ASIC productions:
 - □ Timepix4_v0 (Q1 2020)
 - □ Timepix4_v1 (Q4 2020)
 - ☐ Timepix4_v2 (expected production Q3 2021)



Courtesy X. Llopart (CERN)

Electronics and DAQ

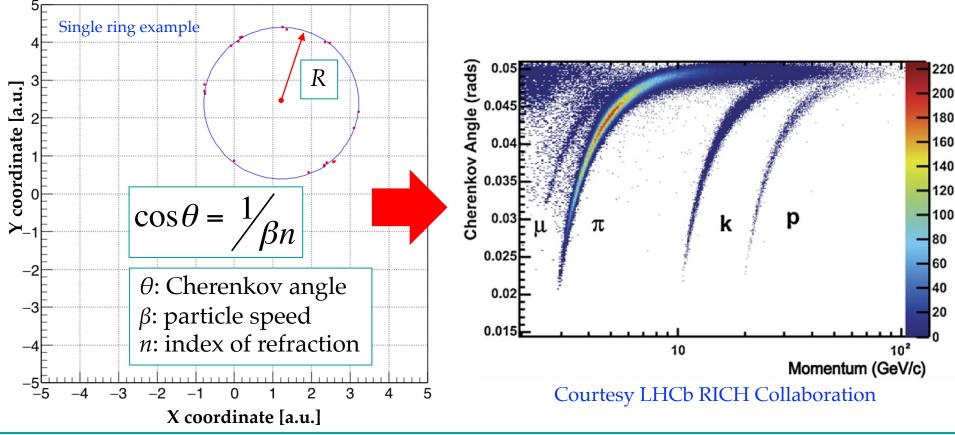
- Front-end electronics architecture is data driven
 - 64 bit for each pixel hit
 - 160 Gbps maximum data rate for a total rate of 2.5 Ghits/s
- Flexible design: electro-optical transceivers will link the ASIC to an FPGA-based board for the exchange of configuration and the collection of event data



- FPGA far from detector
- The FPGA will perform serial decoding and send the data directly to a PC for storage using fast serial data links

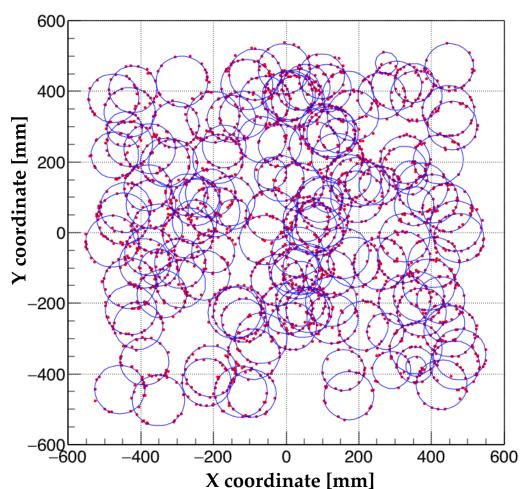
One possible application

- PID using Ring Imaging Cherenkov (RICH) detectors
 - □ Identify ring-shaped pattern of single photons, fit ring radius R (proportional to Cherenkov angle θ), combine with particle momentum \rightarrow particle ID in High Energy Physics experiments



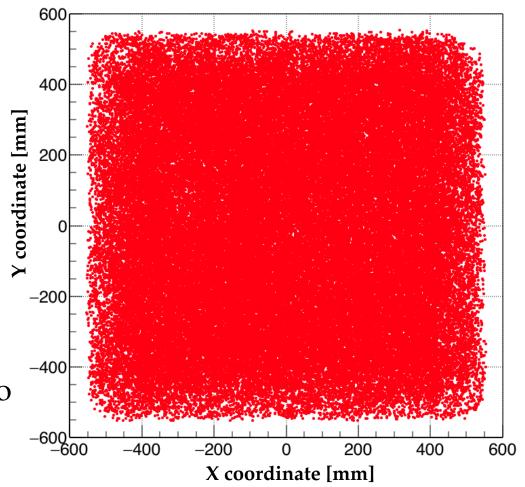
One possible application

- Rings do overlap in high multiplicity environments
- Case study: LHCb experiment in Run 1-2 (2010-2018)
- 4×10^{32} cm⁻²s⁻¹ luminosity
- ~2 k photons in 25 ns bunch-crossing time window (~100 rings)
- Seed information needed from tracking detectors to search for ring center
- Global fitting: maximum likelihood algorithm to extract PID with excellent performance



One possible application

- In the High Luminosity LHC (HL-LHC) environment the situation will not be manageable with state-of-the-art detectors
- e.g. simulation for a HL upgrade of LHCb
- $\sim 2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1} \text{ luminosity}$
- □ ~100 k photons in 25 ns (~5 k rings)
- Rings cannot be resolved
 - No PID information
- Need for a detector with fine granularity and excellent time resolution to separate photons within the same 25 ns bunch



Future RICH detectors

- A RICH detector equipped with such device could deliver unprecedented information and allow efficient PID in the High Luminosity phase of the LHC:
 - Few microns will allow to greatly improve the Cherenkov angle resolution (pixel size contribution becomes negligible)
 - High granularity and rate capabilities are crucial in applications with large detector occupancies
 - Few tens of picosecond timing resolution per single photon will greatly simplify pattern recognition empowering the Maximum Likelihood algorithm with timing (or exploiting time-association of the individual photons)
 - □ Very small DCR (10¹-10² Hz/cm² at room temperature) allows negligible detector-related background
 - Robust in magnetic fields (thanks to MCP and proximity focusing geometry)

Summary

- A detector for visible single photons, based on a bare Timepix4 CMOS ASIC embedded in a vacuum tube with a MCP is under development for the detection of up to 10⁹ photons/s with simultaneous measurement of time and position with excellent resolutions
 - Fully exploit both timing and position resolutions of a MCP
 - High-performance data acquisition (up to 160 Gbps)
- The presented single-photon imaging technology could enable discovery in different fields of science
 - High-energy physics, life sciences, quantum optics, etc.

This project has received funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme (grant agreement No. 819627)

