16th (Virtual) “Trento” workshop on Advanced Silicon Radiation Detectors
16-18 February 2021

3D integration technologies at FBK for Radiation and Optical Sensors

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Project GOAL

Important Projects of Common European Interest

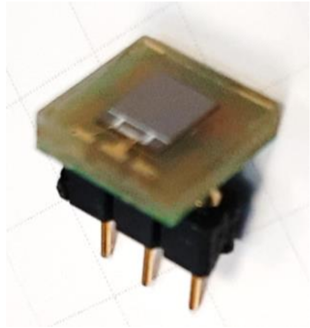
New EU platform to promote innovation in microelectronics up to the first industrial deployment

FBK project GOALS:

- Developing new SiPM technologies for **high-density 3d-integration** with CMOS electronics or photonics components (including BSI technology)
- Improving the FBK-SiPM technology integrating **Through Silicon Vias (TSV)**

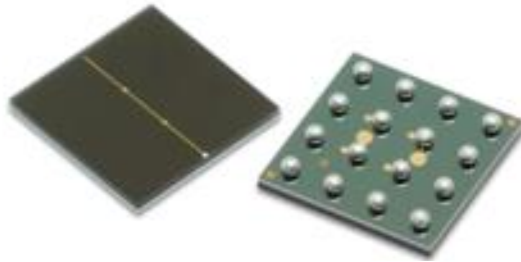
Project GOAL

- Standard FBK SiPM



1 channel

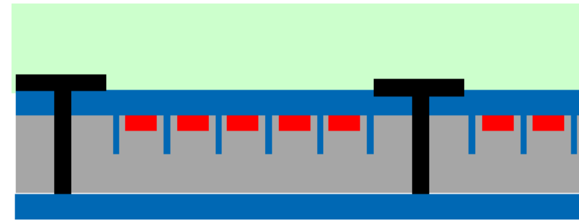
- TSV SiPM



(Based on FBK technology)

1 channel

- Segmented SiPM



Tens of channels

- 3D-integrated SiPM

Thousands of channels
(1 chn per pixel)

Facility Upgrade

Cleanroom Detectors

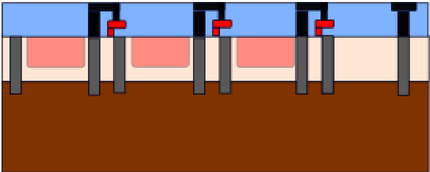
1. Sensor FEOL production

Already existing Detector CR at FBK

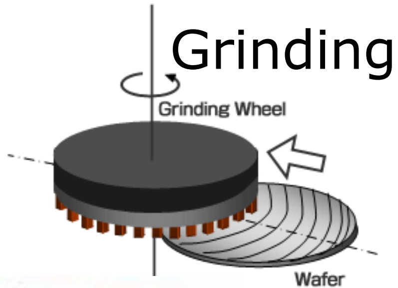
Come back to FEOL & BEOL

3D int. Clean Room

2. TSV and Wafer preparation for 3D integration



u-TSV



Wafer Bonding

Under commissioning (2022)

3. Sensor integration to electronics

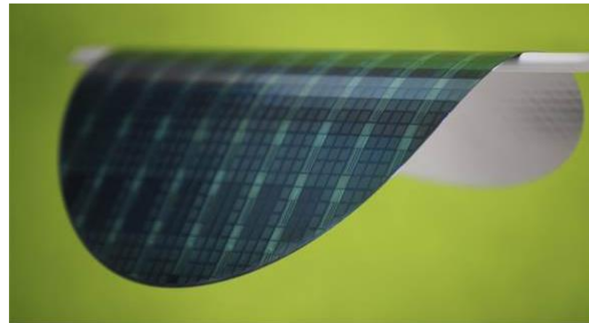
Facility upgrade

The new lab will be equipped with state-of-the-art equipment for both 6″ and 8″ wafer processing

1. Wafer Bonding

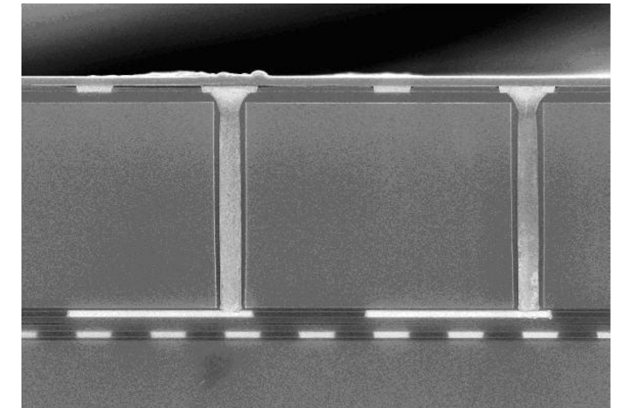
- Temporary Bonding/Debonding
- Permanent Bonding
- Bond Alignment
- Fusion Bonding
- Metal Bonding

3. Wafer Thinning and Grinding



- Wafer grinding
- Chemical Mechanical Polishing
- Pre-grinding dicing

2. Through Silicon Vias and interconnections

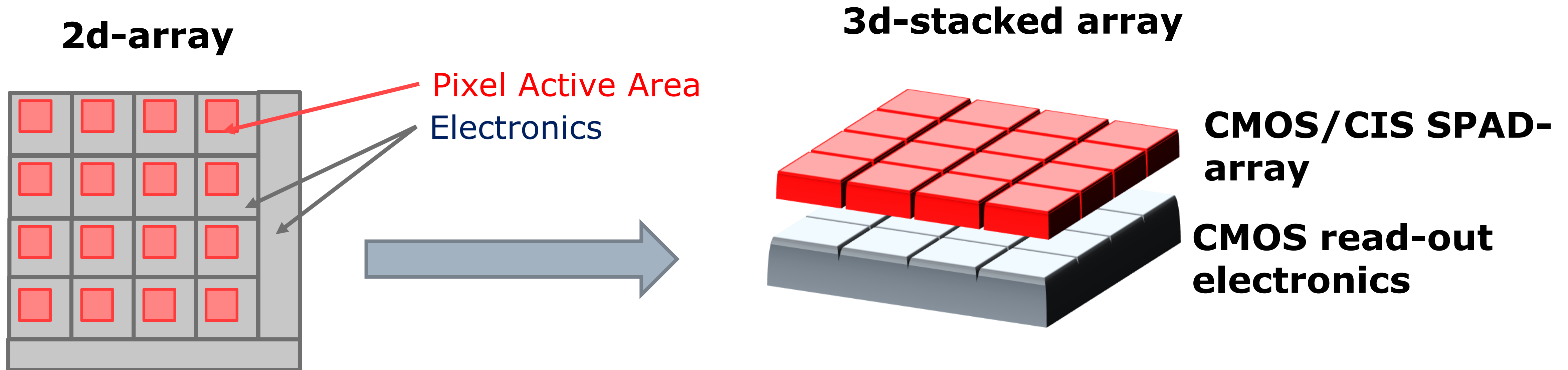


- Via formation
- Via metal filling

New developments in Back Side Illuminated (BSI) SiPM technology for 3d-integration

3D stacked SPAD/SiPM: State of the Art

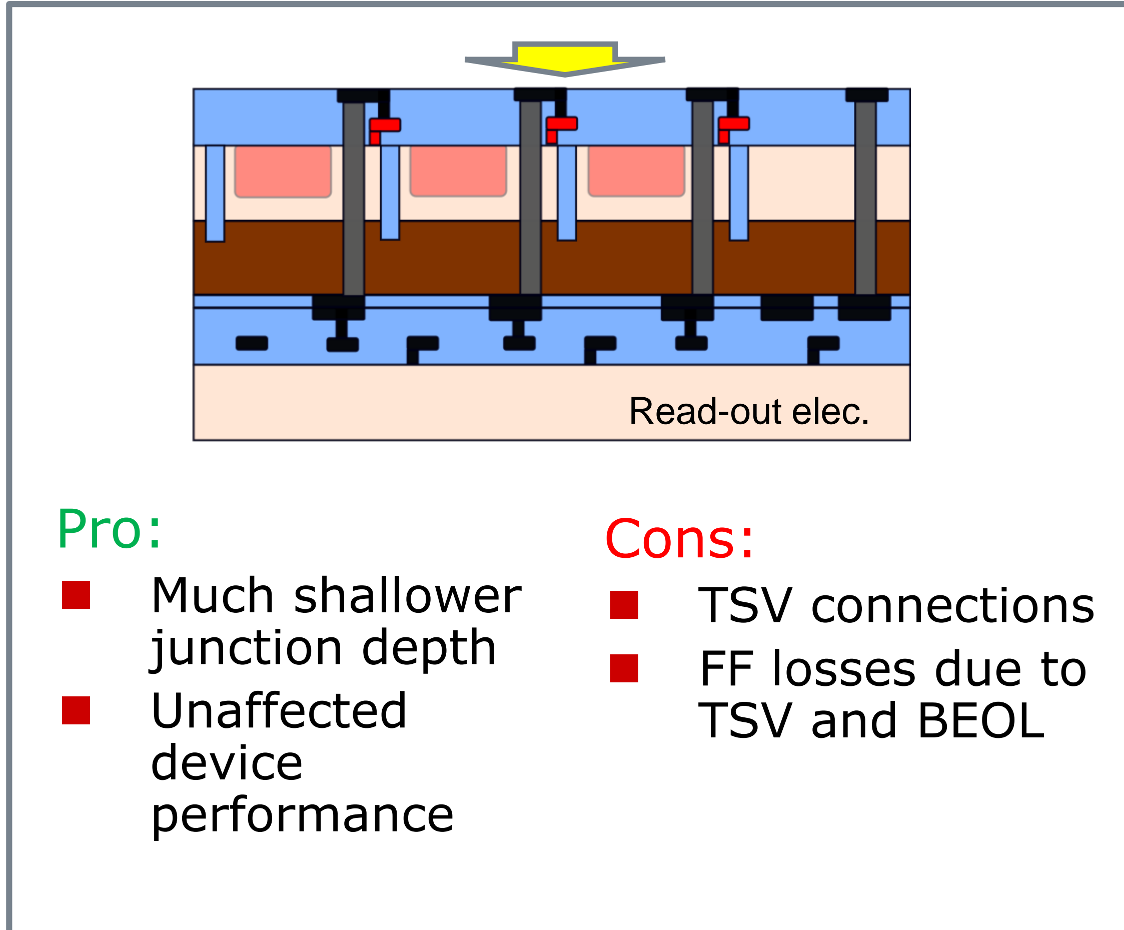
- **The CMOS example**: A few attempts of 3d integrated CMOS SPAD have been done in past years

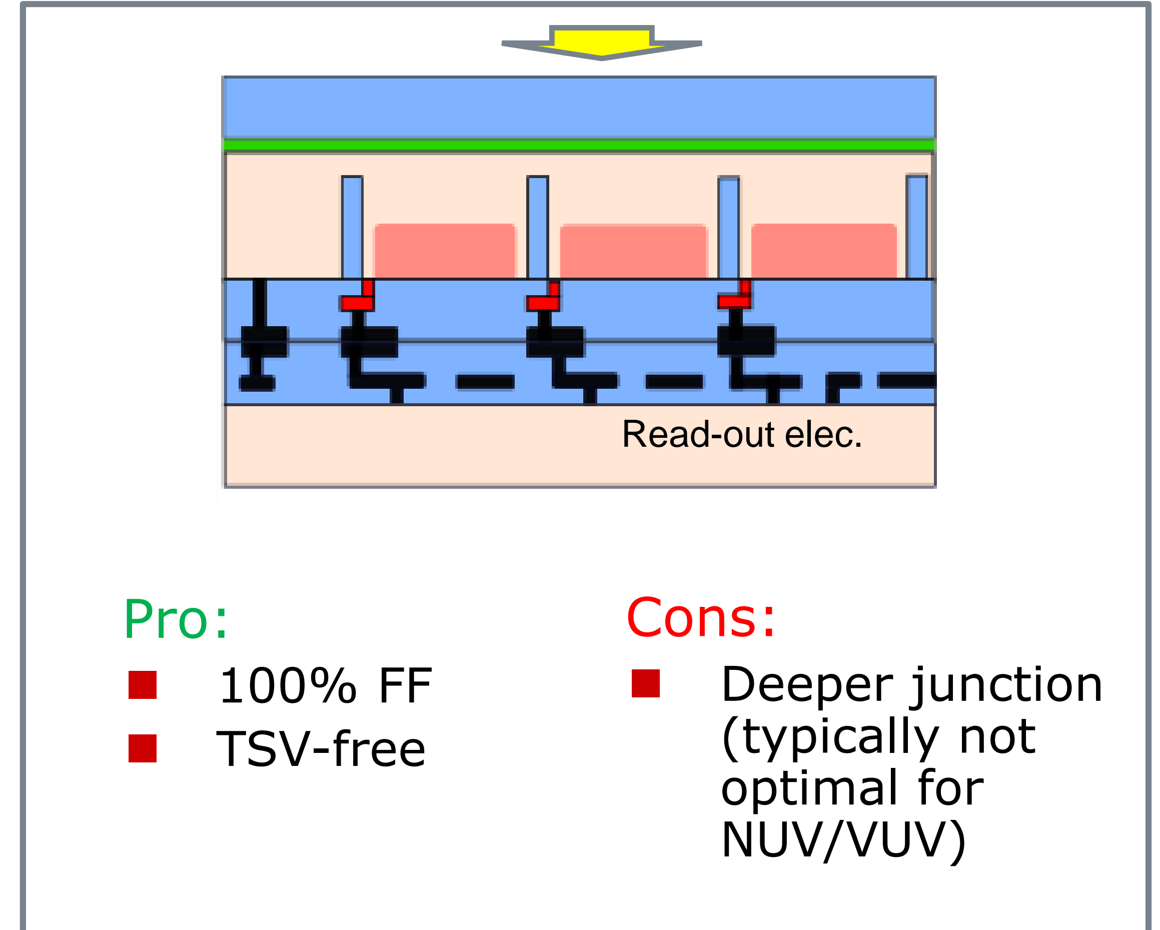


- The promise of 3d integrated SPADs:
  - Higher efficiency (higher FF)
  - More functionality per pixel
  - Each tier can be independently optimized using dedicated process

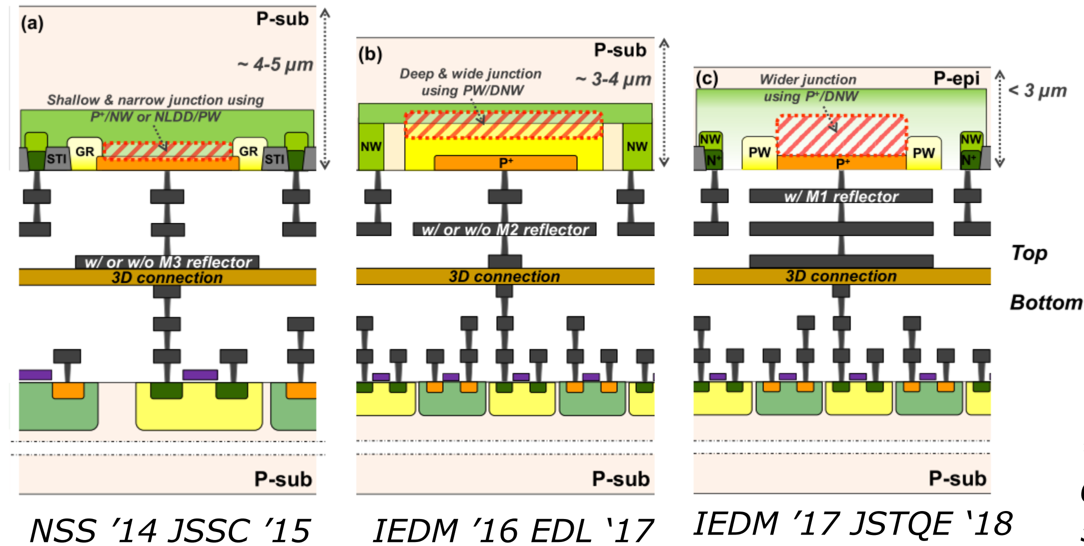
3D stacked SPAD/SiPM: State of the Art

- Front Side Illumination FSI
- Back Side illumination BSI





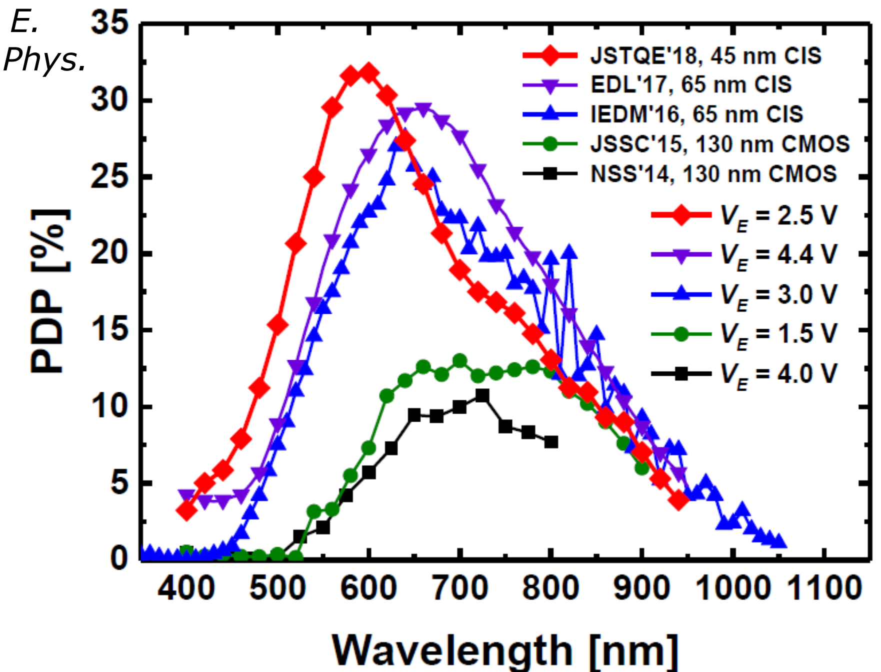
3D stacked SPAD/SiPM: State of the Art



NSS '14 JSSC '15 *IEDM '16 EDL '17* *IEDM '17 JSTQE '18*

**Taken from M.-J. Lee and E. Charbon 2018 Jpn J. Appl. Phys. 57*

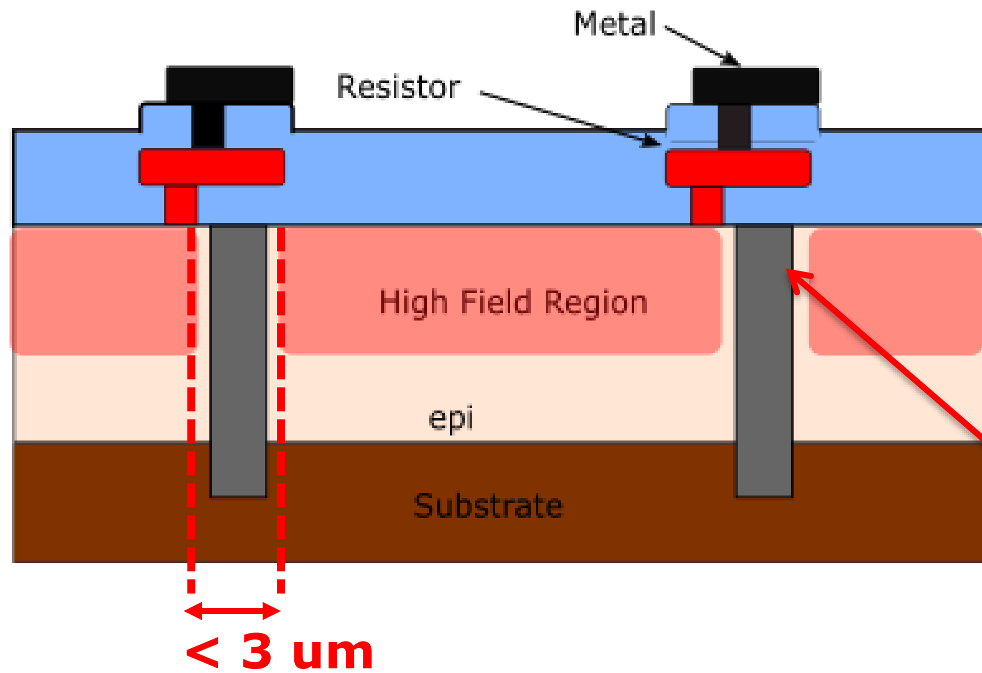
- Back side Illuminated (BSI) SPAD design evolution in the last years: modification of the multiplication junction scheme and reduction of the residual substrate thickness lead to important improvements in PDE



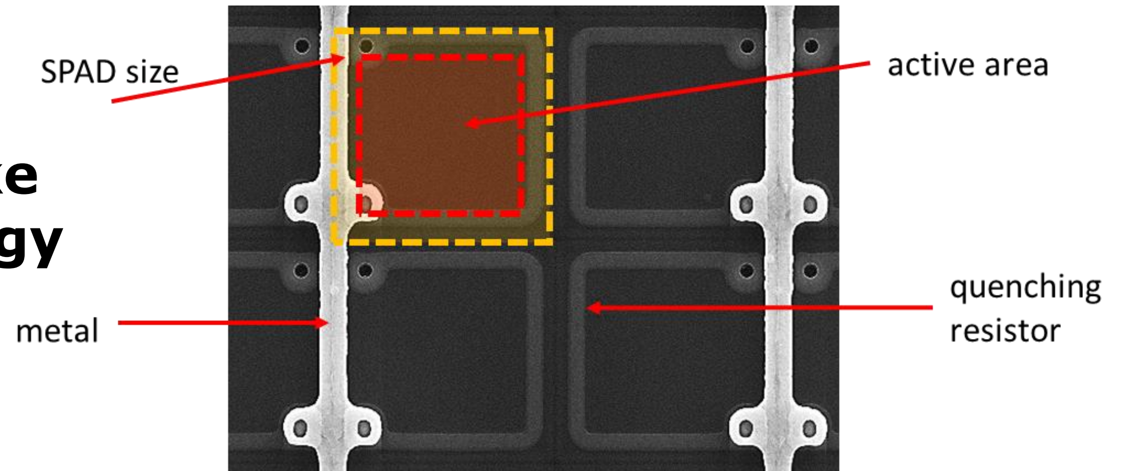
- Typical FoM:
  - PDP peaked at 500-600 nm wavelength
  - PDP at NUV < 5% (20% at 400nm has been recently demonstrated with SOI BSI SPAD)
  - DCR ~ 100-1000 cps/μm^2

**Taken from Lee, M.-J., Sun, "First Near-Ultraviolet- and Blue-Enhanced Backside-Illuminated Single-Photon Avalanche Diode Based on Standard SOI CMOS Technology". IEEE Journal of Selected Topics in Quantum Electronics 2019*

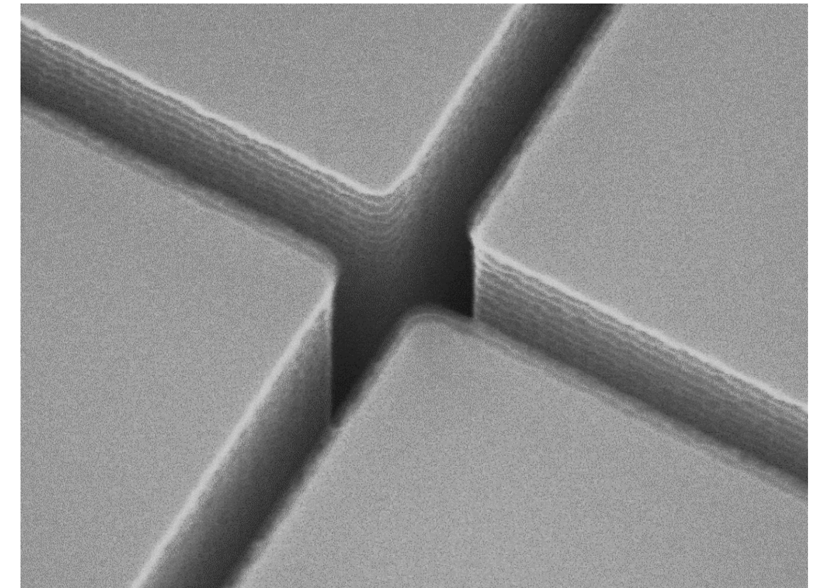
FBK High Density SiPM Technology



Custom CMOS-like technology



Deep Trench

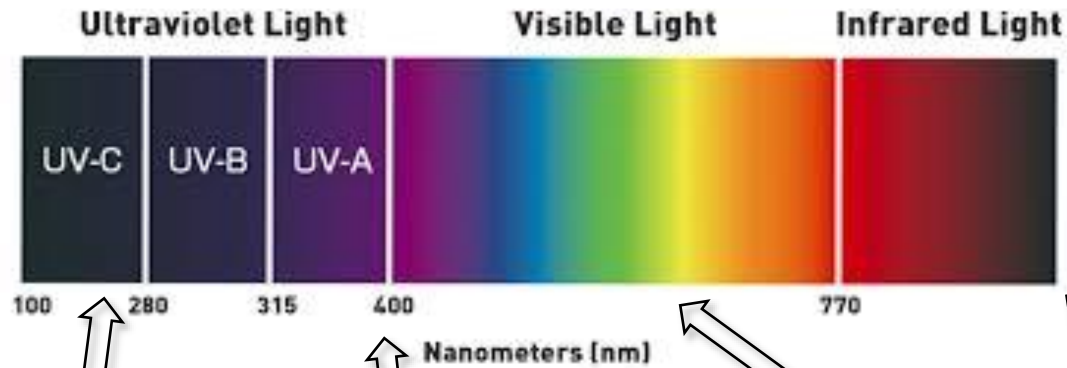


- Trenches between cells → Lower Cross-Talk
- Cell pitch: 15 – 40 um
- Narrow dead border region → Higher Fill Factor (>80%)
- Make it simple: 9 lithographic steps

FBK High Density SiPM Technology

- HD-SiPM is a versatile technology platform that could evolve in different specific technologies to cope with specific requirements

Light spectrum



Working Temperature

VUV-HD

extended sensitivity in the VUV region

NUV-HD

Near ultra-violet

RGB-HD

Broad red-green blue sensitivity

NIR-HD

extended sensitivity in the NIR region

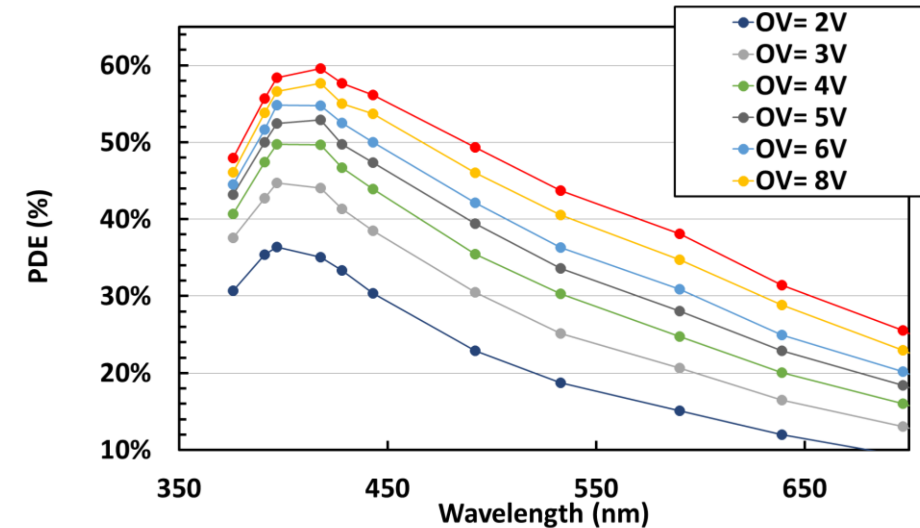
NUV-HD-Cryo

Optimized NUV-HD for cryogenic applications

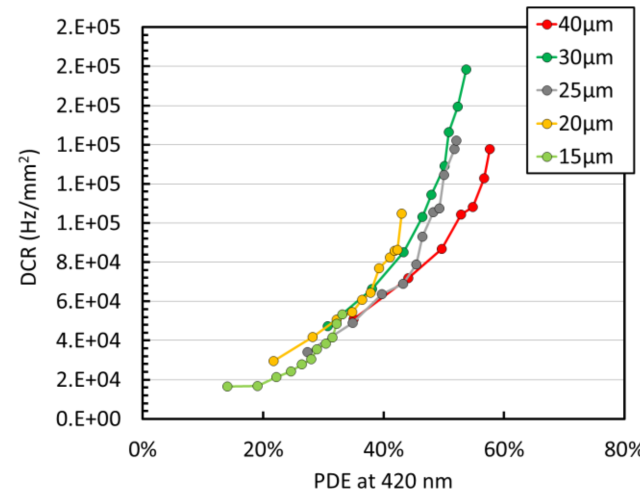
NUV-HD SiPM: main FoM

- Specifically designed to match the LYSO emission peak at 420nm (ToF-PET applications)
- Performance at the state of-the-art:
  - PDE approach 60% (CS=40um)
  - DCR = 100 kHz/mm^2 (0.1 cps um^2)
  - Cross-talk = 20%

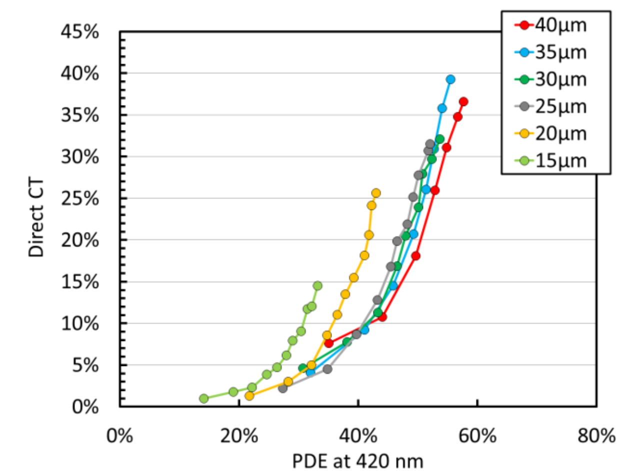
- **Photo Detection Efficiency**



- **Dark Count Rate**



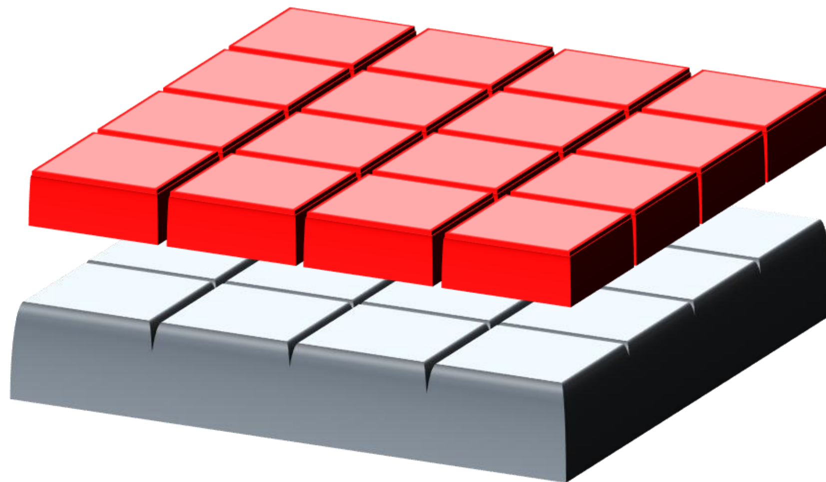
- **Direct Cross-talk**



3D Integration Roadmap at FBK

- In the Framework of IPCEI project, FBK proposed an R&D aimed at developing hybrid sensors integrating:
  - SPAD in Custom Technology
  - CMOS read-out electronics

- Main Wishes:
  - Preserving the performance in terms of PDE and DCR of SPADs in custom technology
  - Adding some functionality at pixel level and further electronics at chip level

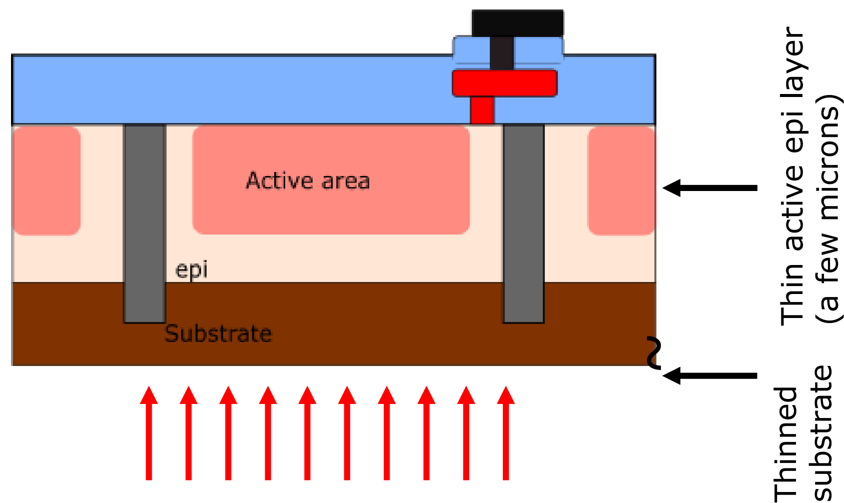


CUSTOM SPAD-array

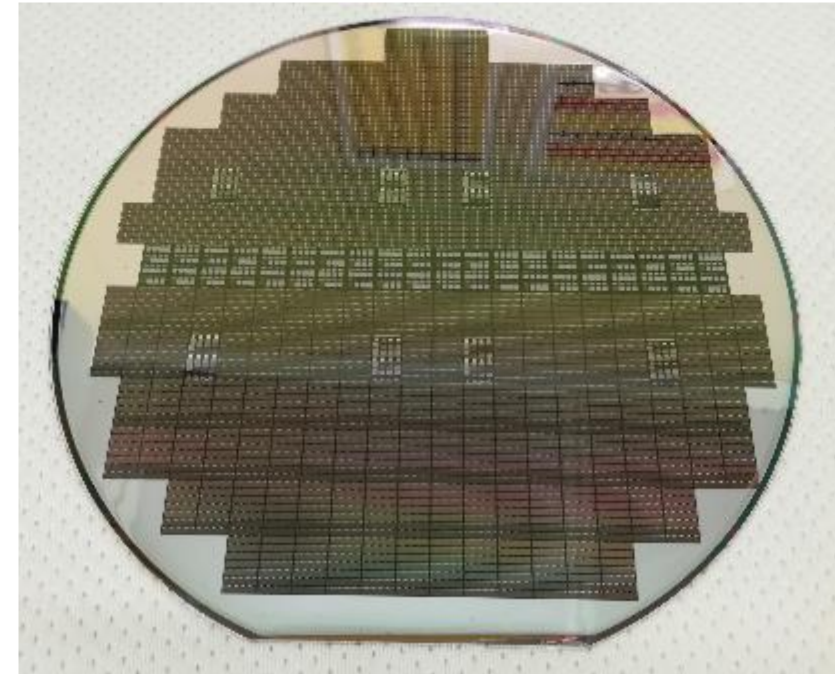
CMOS read-out electronics

BackSide Illuminated NIR SiPMs

- First Test in fabricating BSI SiPM for NIR light detection ready for 3d integration



We started from a standard FBK NIR-HD SiPM Wafer



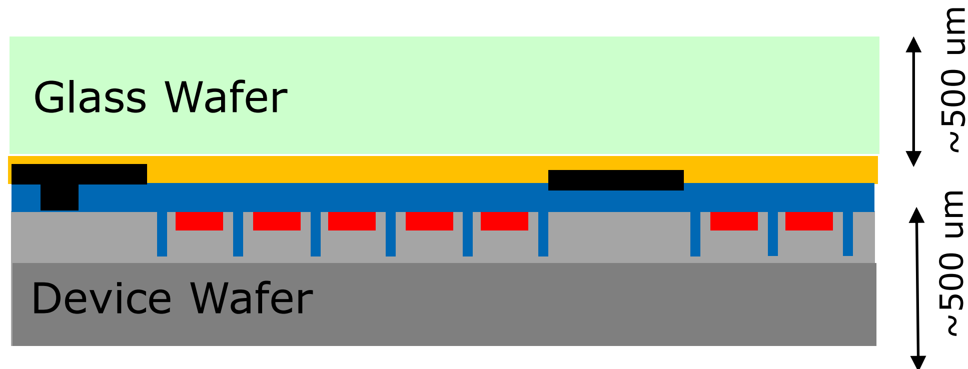
First results on BSI SiPM for Near Infrared

Device Layer-transfer Process flow 1/2

1. SiPM Wafer

- Standard FSI SiPM wafer after BEOL. Both anode and cathode contacts are available on the front. No bulk contact on the back. Starting wafer thickness: 500-700 um

2. Temporary Bonding



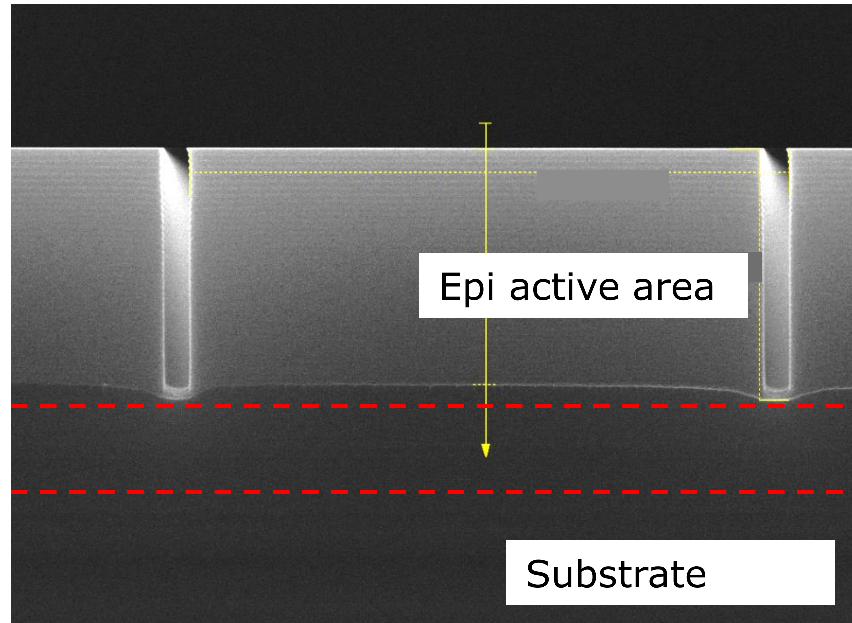
- Temporary bonding to glass carrier wafer by means of adhesive bonding. The adhesive planarize the surface and reduce the wafer topography. Total stack thickness: ~ 1 mm

3. Grinding & Polishing

- Substrate removal by means of grinding and subsequent polishing. The remaining device wafer thickness is ~ 10 um. Total stack thickness: ~ 500 um

First results on BSI SiPM for Near Infrared

Device wafer uniformity after grinding



Ideal target

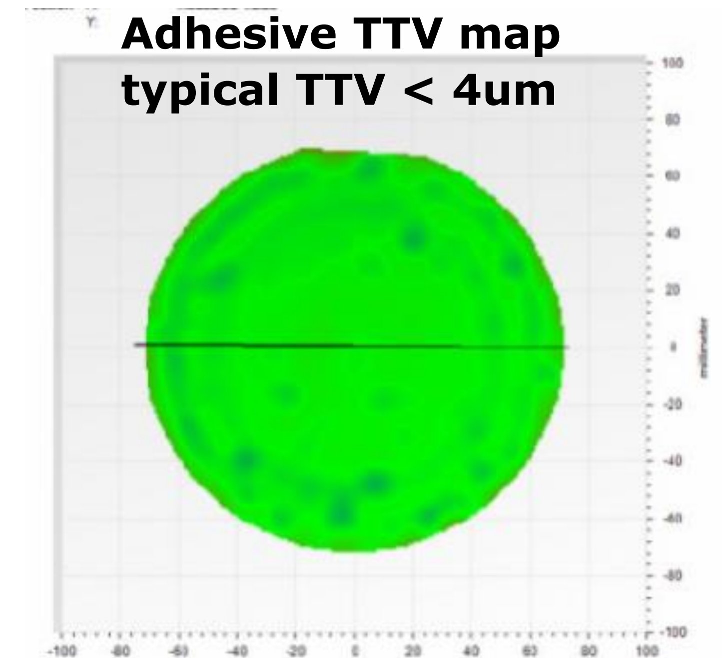
Buffer to take into account TTV

Grinding target

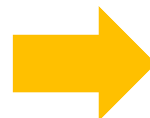
Key parameter

TTV = Total Thickness Variation = max – min thickness at wafer level

Adhesive TTV map typical TTV < 4um



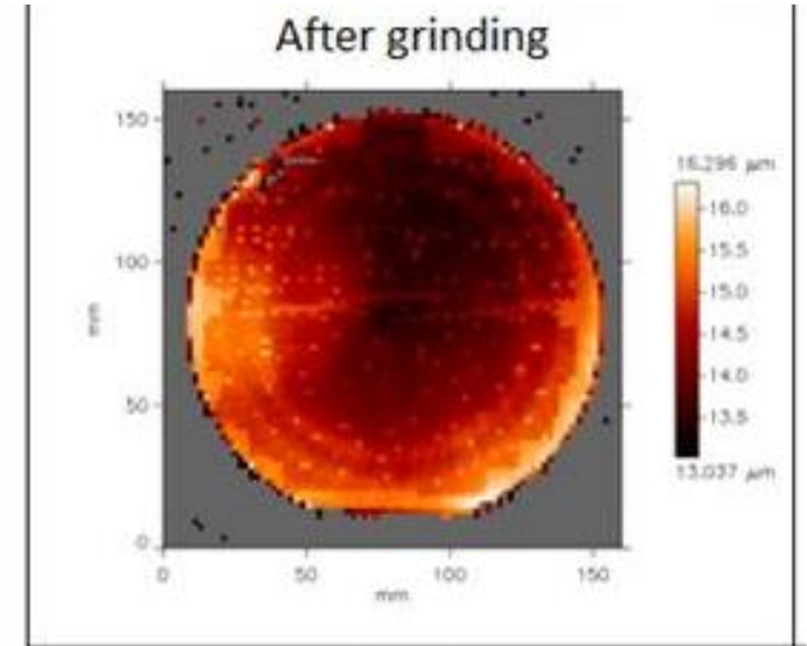
- TTV of both initial wafer and of the adhesive are two key aspects to optimize the TTV of the final device wafer



First results on BSI SiPM for Near Infrared

Device wafer uniformity after grinding

- TTV map of the final device wafer
- We processed 6 SiPM wafers obtaining **final TTV in the range 3–4 um**

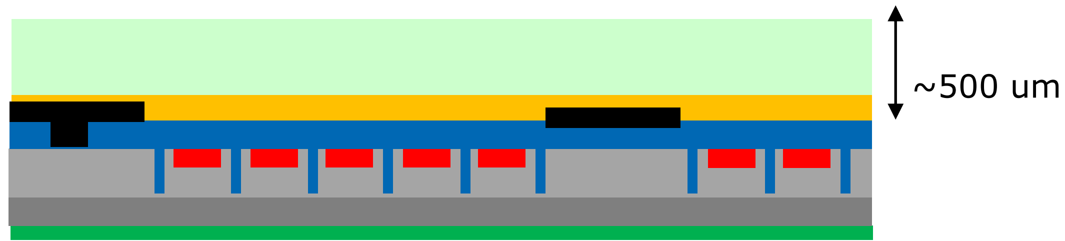


Avg.	14.40
Min.	13.04
Max.	16.30
TTV	3.26

First results on BSI SiPM for Near Infrared

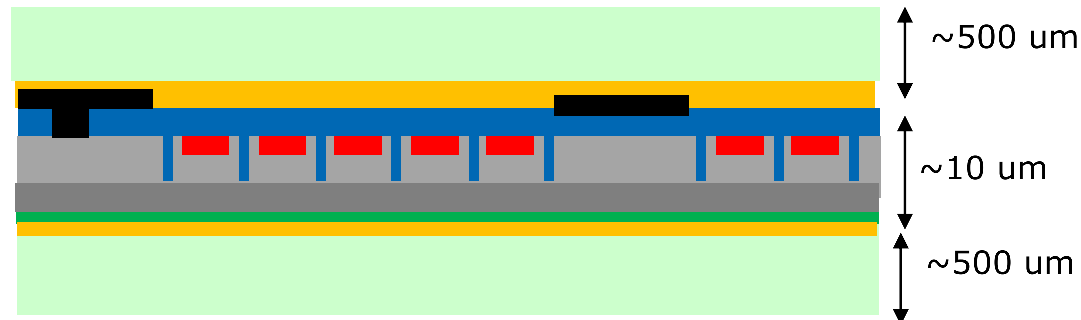
Layer-transfer Process flow 2/2

4. Backside processing



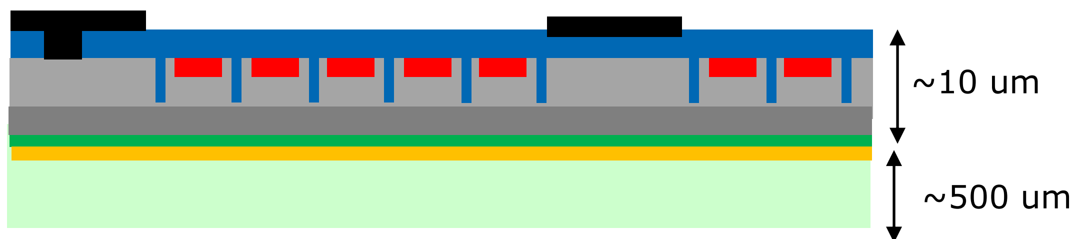
- Anti-reflective coating & passivation layer deposition (limited thermal budget)

5. Permanent Wafer Bonding



- Permanent bonding to a second glass carrier wafer by means of adhesive bonding. The adhesive is transparent to the visible light. Total stack thickness: ~ 1 mm

6. Wafer Debonding



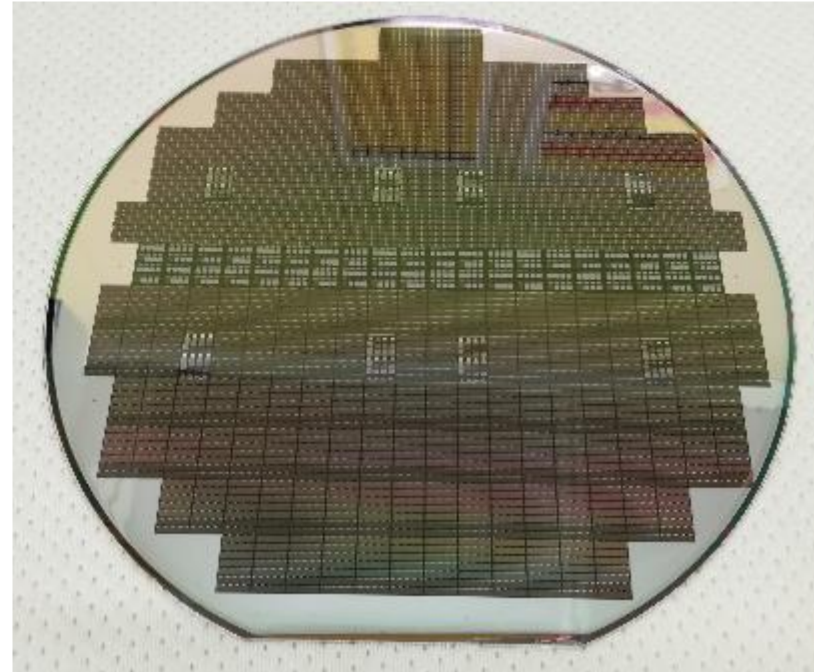
- The first carrier is debonded. The top side of the device wafer is exposed again

First results on BSI SiPM for Near Infrared

Process results

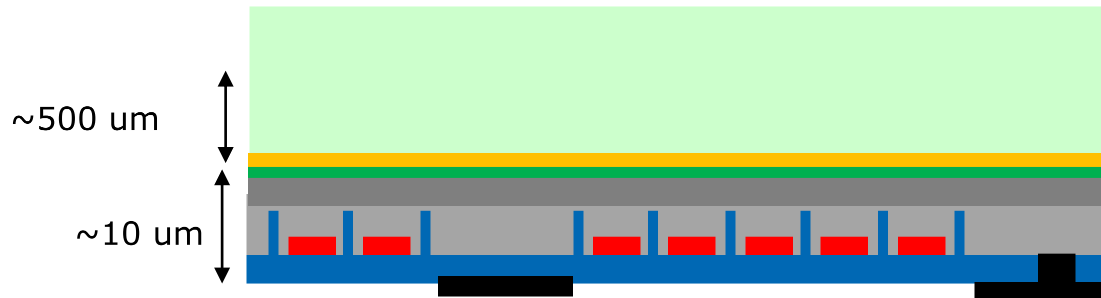
- 6 wafers have been processed with ultra-thinning and transfer-layer.
- 5/6 of the wafers resulted not-damaged at the end of the process
- The temporary Bonding-debonding and thinning both resulted very promising.

Front: device side



Rear: glass side

Final wafer

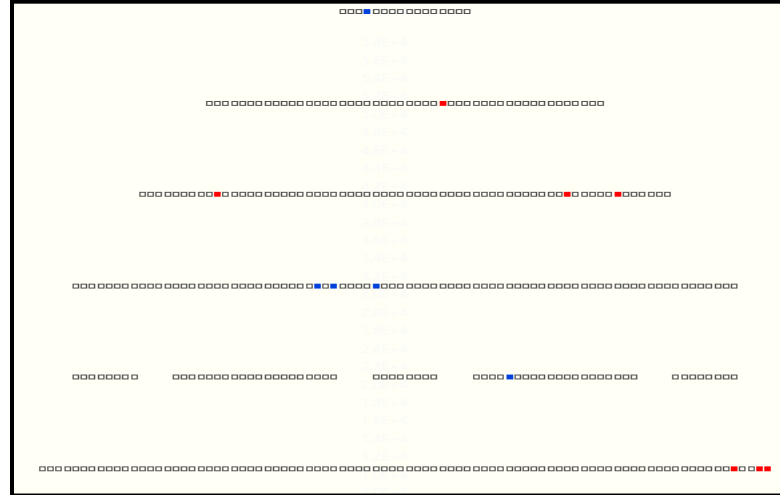


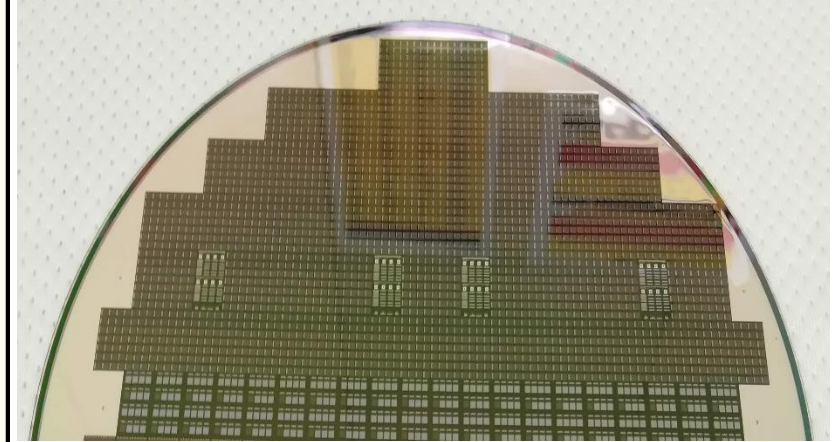
Ready to be 3d-stacked with the readout electronics…

High connection density is possible up to singe-pixel connection

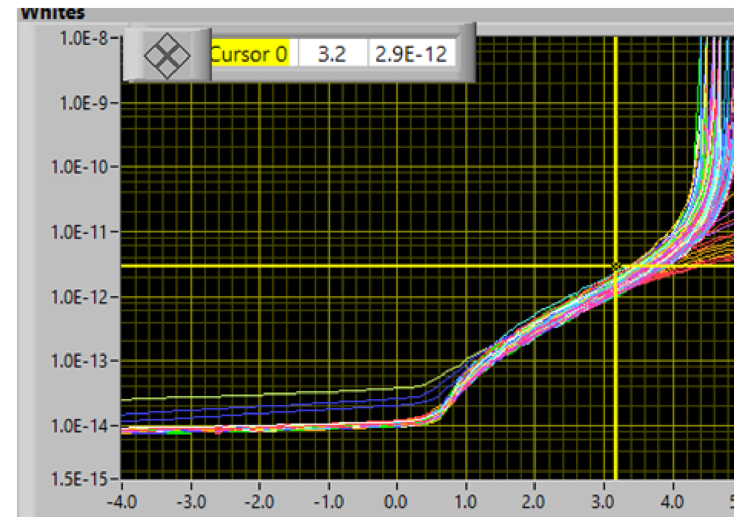
First results on BSI SiPM for Near Infrared

- **Electrical characterization**





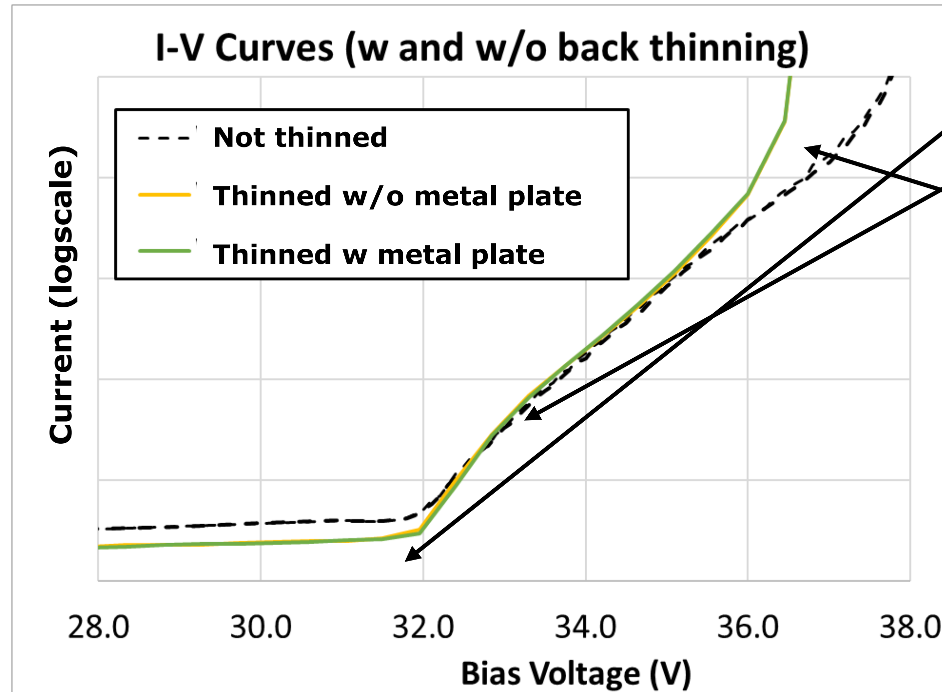
- Automatic I-V measurements after ultra-thinning
- 180 SiPMs (1 mm^2) have been measured on a 6'' wafer
- 169 working SiPMs (~95% yield).



- Compilation of I-V curves from a single back thinned wafer
- Breakdown voltage and current behavior are similar to not-thinned devices

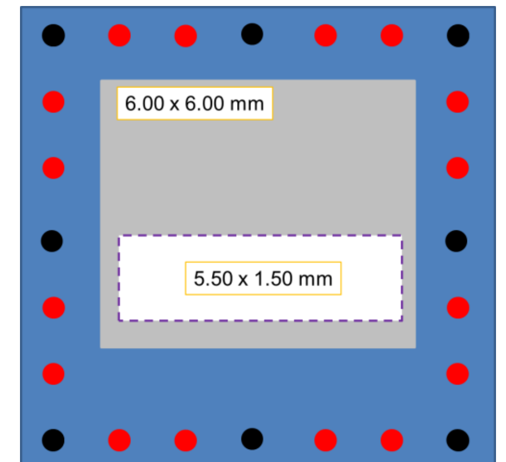
First results on BSI SiPM for Near Infrared

Electrical characterization



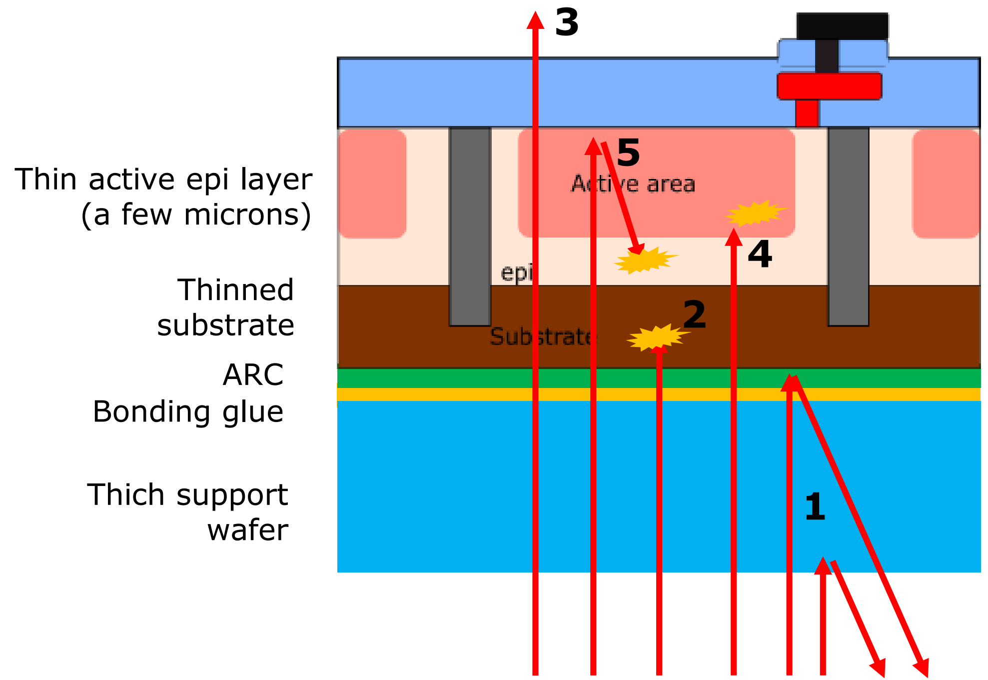
- Same BD voltage and same dark current w/o and with thinning
- The thinning process does not degrade the electrical and noise performance of the device at low excess bias voltage
- At higher excess bias voltage the thinned devices show premature divergence (correlated noise? Defects at the grinded surface?)

PCB with open window for both FSI and BSI measurements



BackSide Illuminated NIR SiPMs

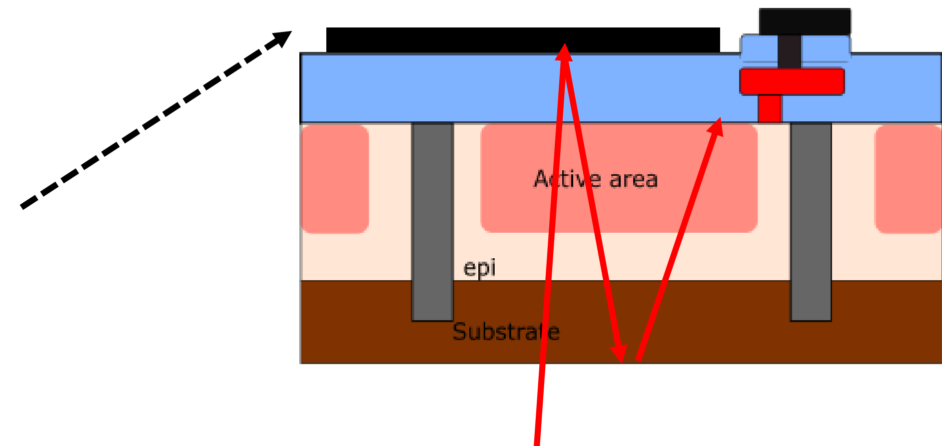
NIR Photon absorption in BSI SiPM



1. Photons reflected at the entrance surface
2. Photons absorbed in the residual substrate
3. Photons escaping from the front surface
4. Photons absorbed in the active area
5. Photons back reflected at the front surface (light trapping)

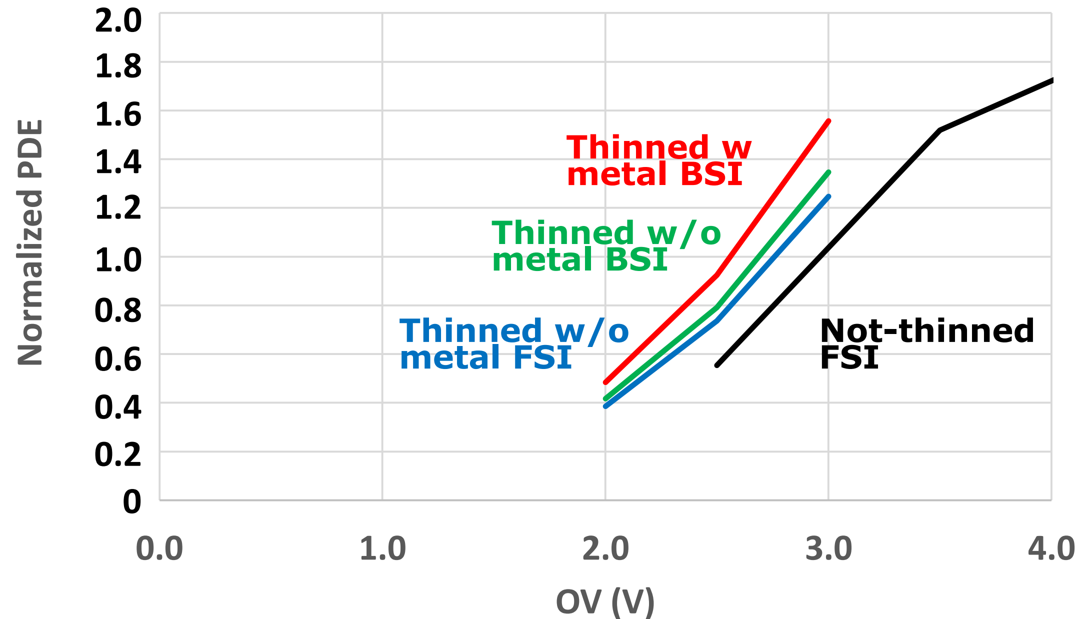
lost (1–3); counted (4–5)

- Including metal plate on the top surface can enhance the light trapping



First results on BSI SiPM for Near Infrared

PDE measurements @ 905 nm (very preliminary)

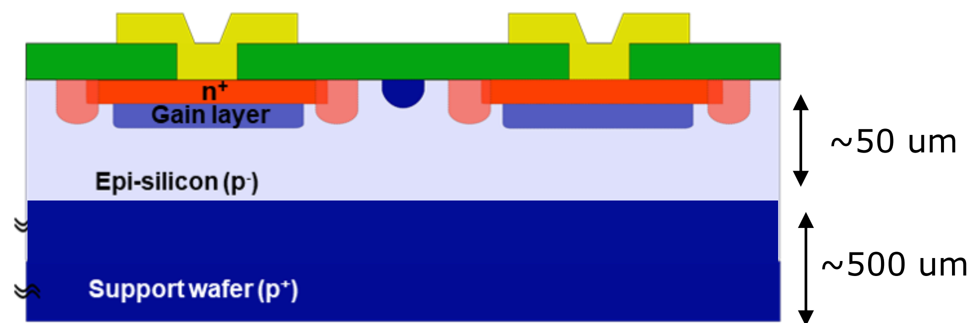


Type	Normalized PDE @ 905 nm 3V OV
Ref. not thinned	1 (normalized)
Thinned no metal FSI	+ 24%
Thinned no metal BSI	+ 34%
Thinned metal BSI	+ 50%

- Many investigations and measurements are still ongoing:
  - Role of destructive/constructive interference in the silicon slab (full spectrum is going to be measured)
  - Enhanced NIR absorption in the high-doped substrate
  - ARC optimization for light trapping

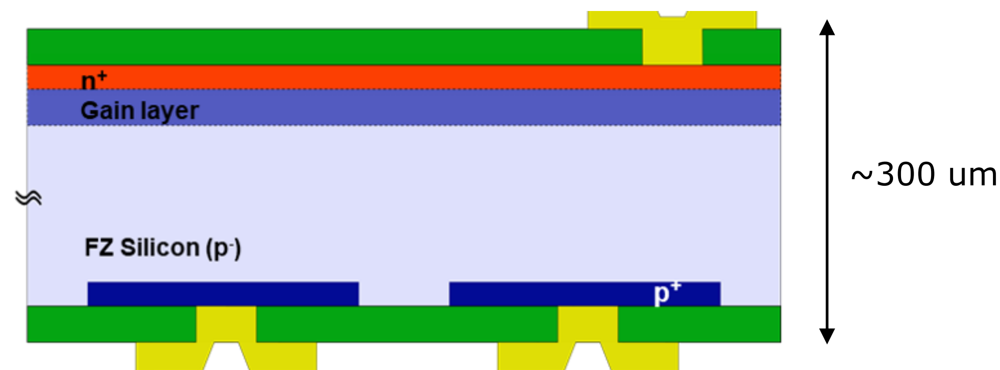
Technology exploitation for LGAD

Standard segmented LGAD



- Internal Gain and thin active substrate give **High Time Resolution**
- **Limited spatial resolution** (presence of a wide inter-pixel dead border due to gain segmentation)

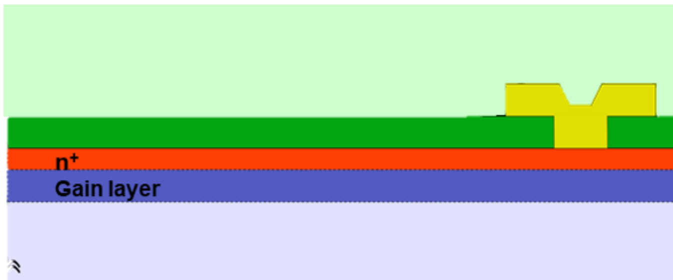
Double-sided LGAD (or iLGAD)



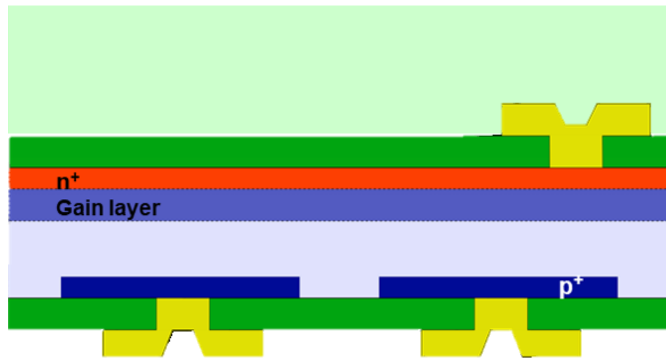
- **High Spatial resolution** (no gain segmentation)
- **Limited time resolution** (thick substrate limited by wafer handling)

Technology exploitation for LGAD

- Front-side (LGAD-side) processing
- Temporary Bonding to carrier wafer

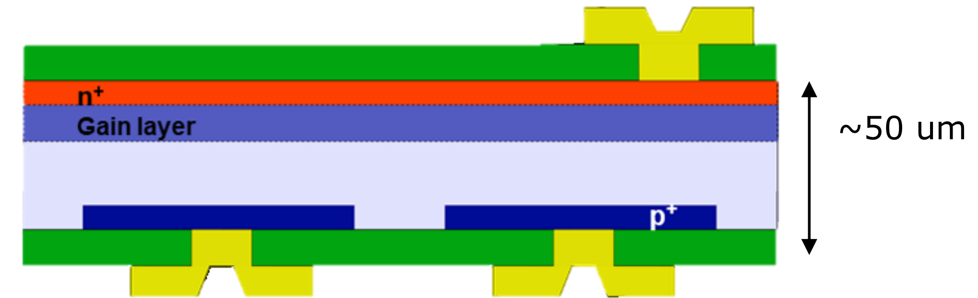


- Wafer Grinding down to 50-100 um



- Back Side contact formation (low thermal budget)

- Tape attaching and debonding
- Dicing



Thin double-side LGAD

Other interesting applications of 3d-integration technologies for LGADs are in: "LGAD for 5D Tracking" by R. Lipton, Fermilab, presented at 37th RD50 Workshop, 2020

Conclusions

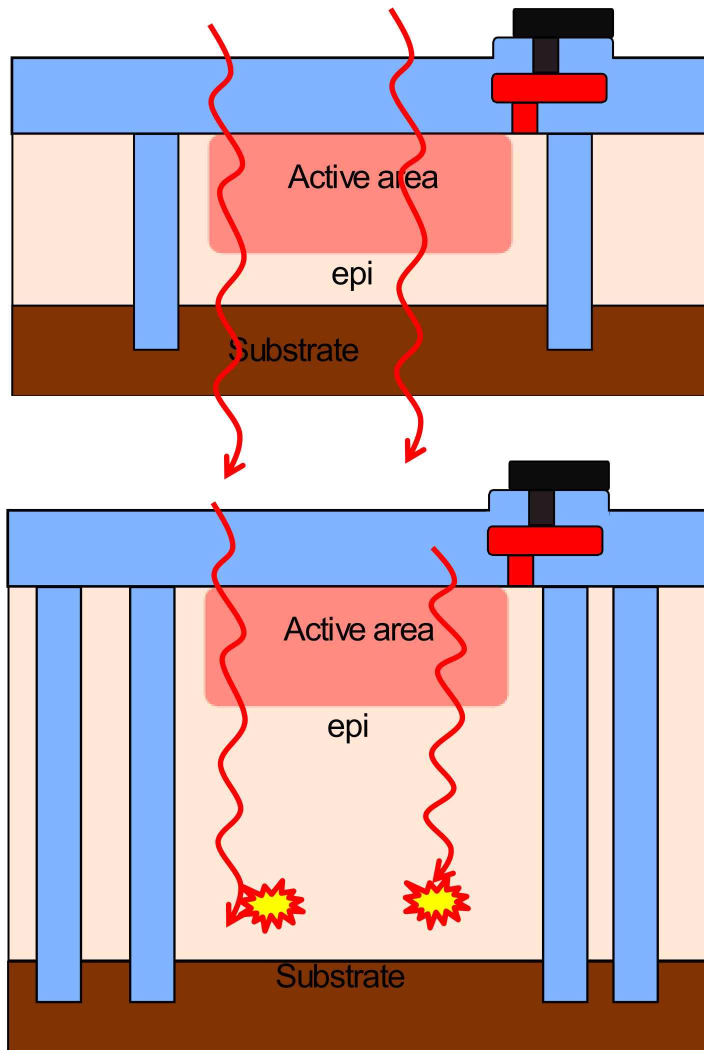
- FBK is working at development of new optical/radiation sensor technologies for 3d-integration applications in the framework of IPCEI Microelectronic project.
- A new laboratory with state-of-the-art equipment (wafer bonding, grinding, TSV) is under commissioning.
- First results on BSI SiPM for Near Infra Red have been presented. Promising results with PDE enhancement at 905 nm up to 50%.
- Future possible developments on other radiation sensors have been discussed

Acknowledgements

- This work is funded by the Italian Ministery "Ministero dello sviluppo economico" (MISE) in the frame of the "Important Project of Common European Interest (IPCEI)".

Thank you for your attention

FBK NIR-HD SiPMs

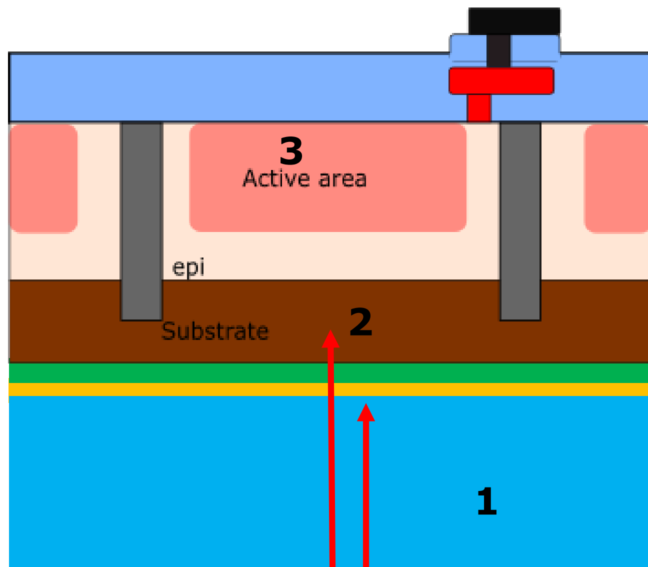


- NIR light with energy close to the Si bandgap interacts deeper in the substrate
- Thicker epi-Silicon is used to increase absorption
- Multiple trenches for CT mitigation
- Electrical Field re-design for better lateral charge collection.

NIR-HD technology

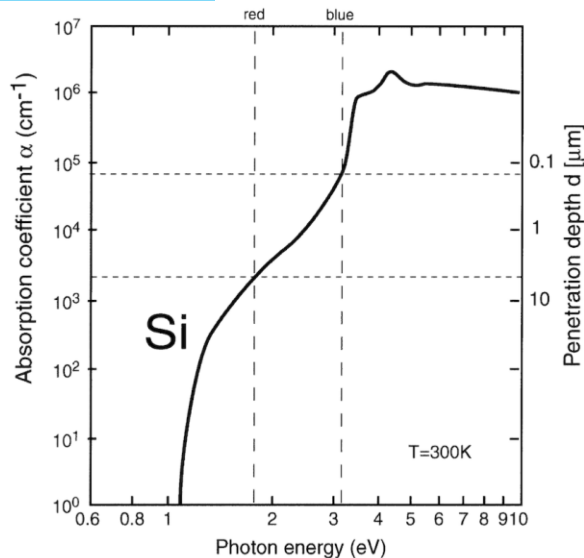
- Primary DCR in the order of ~1Mcps/mm2
- Direct CT: ~10÷20%
- PDE:
  - **17% ÷ 20% @850nm**
  - **11% ÷ 13% @900nm**

Future developments for NUV/VUV BSI SiPM

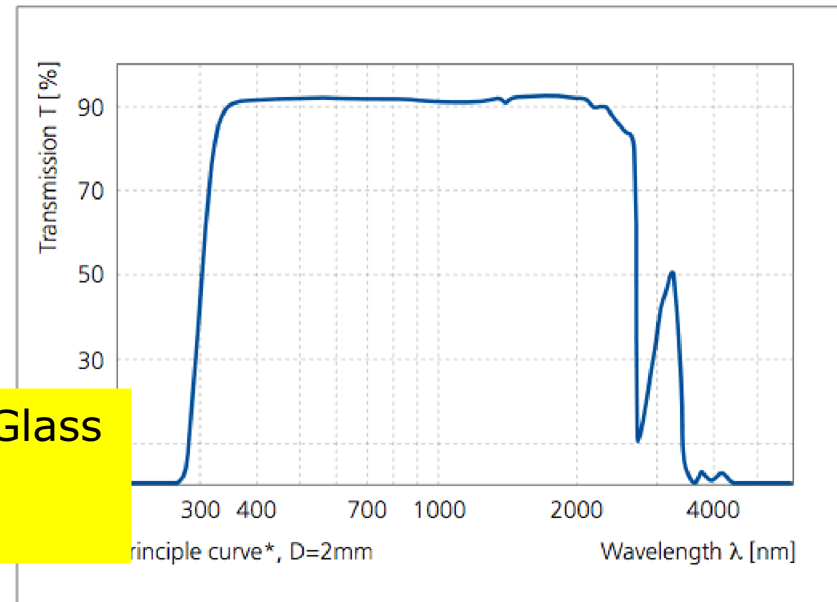


Challenges in BSI NUV/VUV SiPM

1. Glass carrier and bonding glue typically absorb light at wavelengths < 350 nm => **necessity to remove the glass from the backside**
2. Photons interaction depth in Si is < 100nm at lambda < 450 nm. All the photons are absorbed close to the back surface. => **Necessity to completely remove the substrate.**
3. The multiplying junction is far away the absorbing area. Recombination losses could be high.



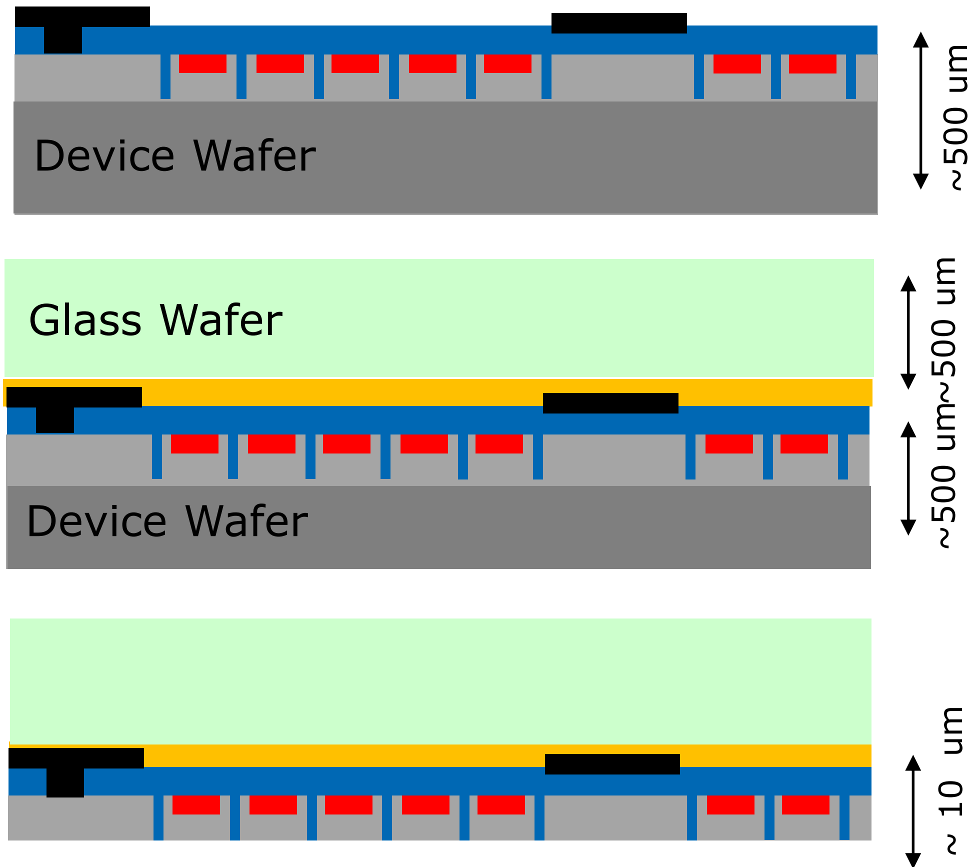
Si absorption depth vs wavelenght



Borosilicate Glass Transmission Spectrum

Future developments for NUV/VUV BSI SiPM

Process flow



1. SiPM Wafer

- Standard FSI SiPM wafer after BEOL.

2. Permanent Bonding

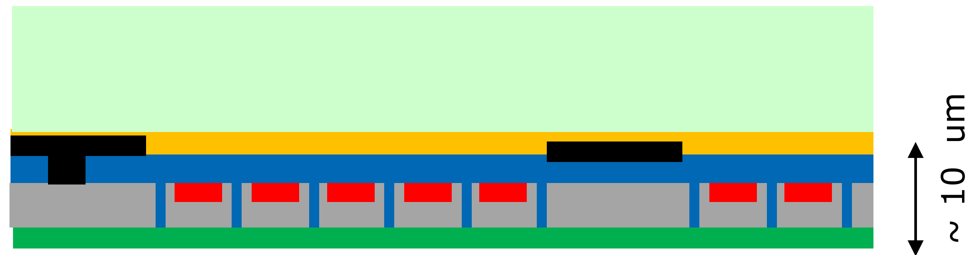
- Permanent bonding to glass/silicon carrier wafer by means of adhesive bonding.

3. Grinding & Polishing

- Substrate removal by means of grinding.
  Complete removal of the support wafers
  Required TTV < 1 um

BackSide Illuminated NUV/VUV SiPMs

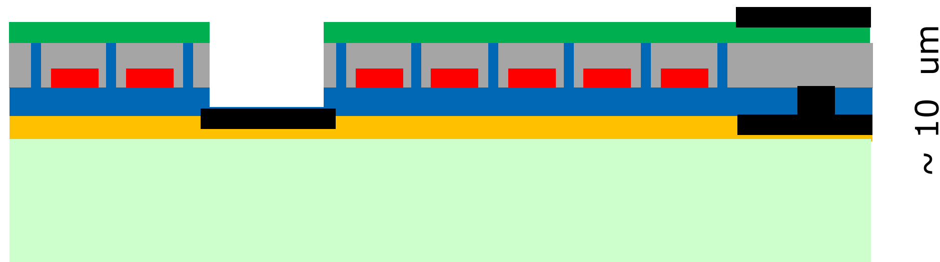
Process flow



4. Backside processing

- **New junction formation** (collection junction) with low thermal budget:
  - implantation + laser annealing
  - Molecular beam epitaxy
  - Other…

Wire-bonding



TSV