Prospects for 3D integration in pixel detectors and readout chips

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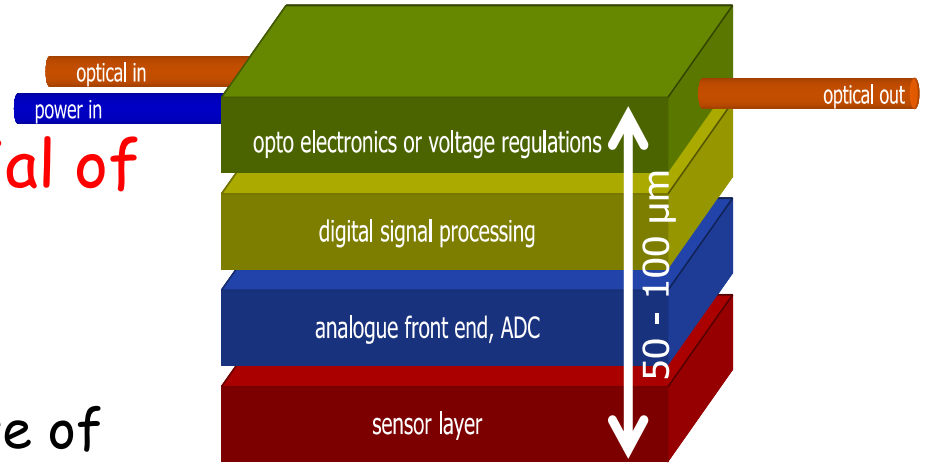
What is 3D integration?

- 3D electronics: "integration of thinned and bonded silicon integrated circuits with vertical interconnects between the IC layers."[1]



- 3D electronics has the potential of being:
  - Denser (smaller form factor)
  - Faster (reduced delay because of shorter interconnects)
  - Lower power (smaller interconnect capacitance)
  - Lower cost (sizably less expensive than aggressive CMOS scaling)
  - Integration of dissimilar technologies (sensor, analog, digital, optical)

1) Philip Garrou, Christopher Bower, Peter Ramm, Handbook of 3D Integration Technology and Applications of 3D Integrated Circuits,Wiley-VCH, 2008.

R&D on 3D integration: results, present work, plans in the HEP community

- About 15 years ago, 3D integration aroused a lot of interest in our community in view of the design of a new generation of silicon vertex detectors and readout electronics
- The pixel sensors community has been working with several companies providing 3D integration technologies (Through-Silicon Vias, low-mass bonding,…)
- There is a lot of obvious synergy between photon science and particle tracking in 3D integration projects for new pixel detectors
- Recent developments associated with industrial and scientific applications of CMOS image sensors and SPADs show that three-dimensional pixelated systems can achieve outstanding performance
- Status and prospects of 3D integration for detectors and electronics in HEP: ideas, technologies, projects,… (I cannot cover everything, I'll discuss a few examples showing the great potential of 3D technology)

3D integration as a tool to advance the state of the art of pixel sensors

- **Improve resolution ⇒ shrink pixel size and pitch**,
  down to about 20 μm or even less

- **Preserve or even increase pixel-level electronic functions**
  handling of high data rates, large dynamic range, high resolution analog-to digital conversion and timing, sparsification, large memory capacity, intelligent data processing, independent analog and digital substrates: the limit to the minimum size of pixel readout cells can be overcome with multiple tiers of electronics

- **4-side buttable tiles**
  large area detector with minimum or no dead area, thanks to TSV and backside metallization and patterning (RDL)

- **Decrease amount of material ⇒ thin sensor and electronics**
  reduce errors in track reconstruction due to multiple scattering of particles in the detector system (thinning to a 50 -100 μm total thickness, needed to optimize TSV geometry)

3D integration in our community

- 3D integration for pixel detectors and readout integrated circuits was first proposed in our community by the Fermilab group, which has been a major driving force

(R. Yarema, Development of 3D integrated circuits for HEP, LECC 2006; R. Yarema, VERTEX2007; at VERTEX2006, talk on 3D electronics by MIT LL)

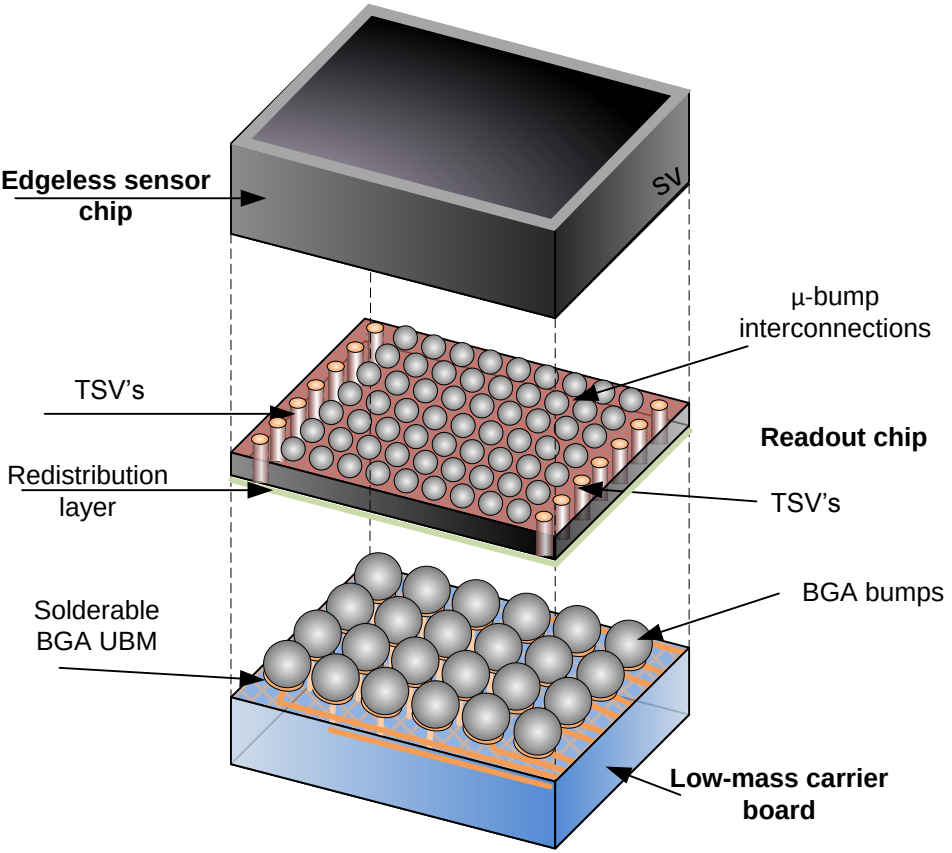
- Groups in Japan and Europe have been also very active, forming research networks (in Europe: AIDA WP3 and AIDA-2020 WP4)

- After initial exciting prospects associated with high density TSV and interconnections, technologies for low density peripheral TSV were then explored

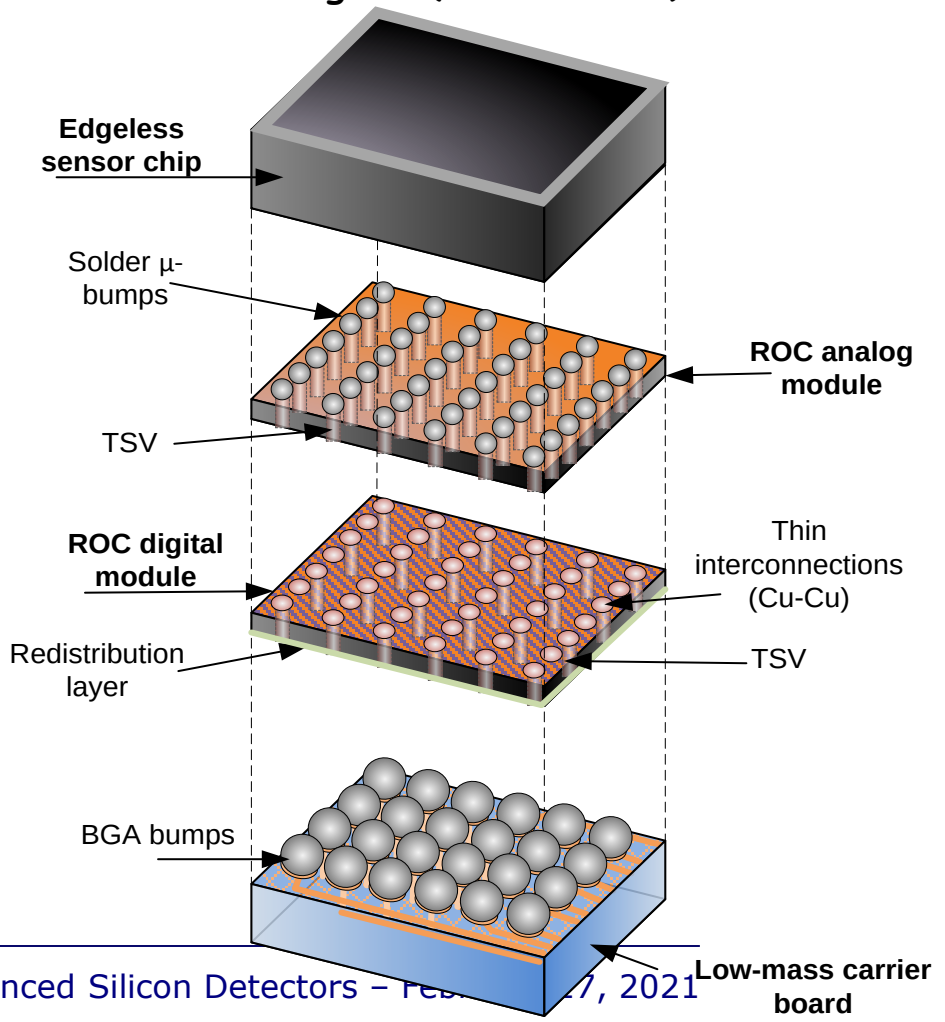
- Results on functional vertically integrated systems in various technologies are now available, and provide the basis of plans for a new generation of 3D devices

Pixel sensor tiles

Peripheral TSV (via last)
Single layer readout chip
TSV carry I/O to backside
Pixelated ASIC layout with I/O, control and other functions in the periphery



Small pitch TSV (via middle)
Double layer readout electronics
Signal exchange through dense inter-tier bonding interfaces
Separate functions of analog (pixelated) and digital (distributed) tiers



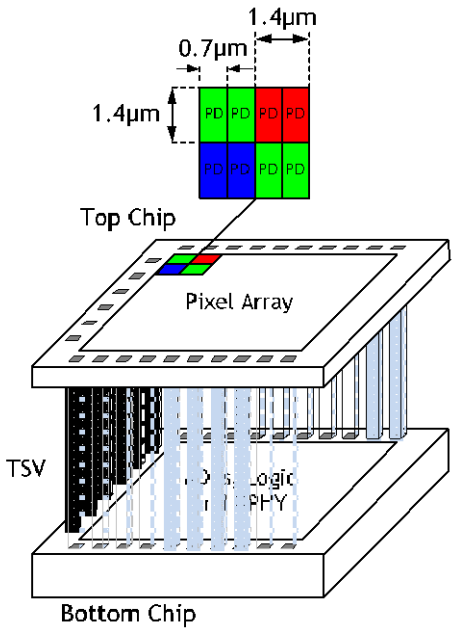
MUX 2010 WORKSHOP,
SAMI VÄHÄNEN – CERN PH-ESE

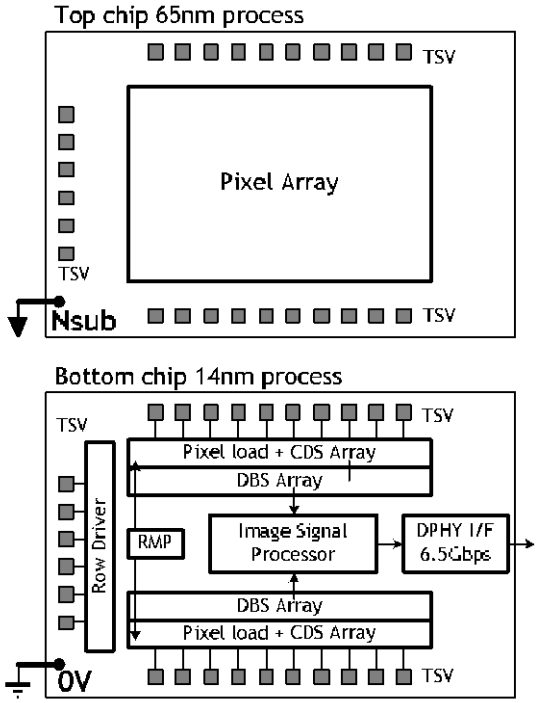
3D in commercial microelectronics: imagers

- "BSI and 3D-stacked processing continue to offer improved performance with increased on-chip functionality and new features being integrated at the pixel level" (from the ISSCC 2020 report)
- A clear industrial technology trend is based on the stacking of CMOS image sensors with a CMOS mixed-signal readout chip, both in decananometer technologies (see also ISSCC2021)
- sub-μm pixel CMOS image sensors have been fabricated thanks to small pitch bonding interfaces and wafer stacking
- 3-layer devices with image sensor, RAM, and logic are available thanks to high-density TSV, opening the way to event-based imaging, to AI processing and machine learning
- The resulting architectures may stimulate interesting ideas for particle tracking detectors

Image sensor 3D-stacked with a FinFET readout

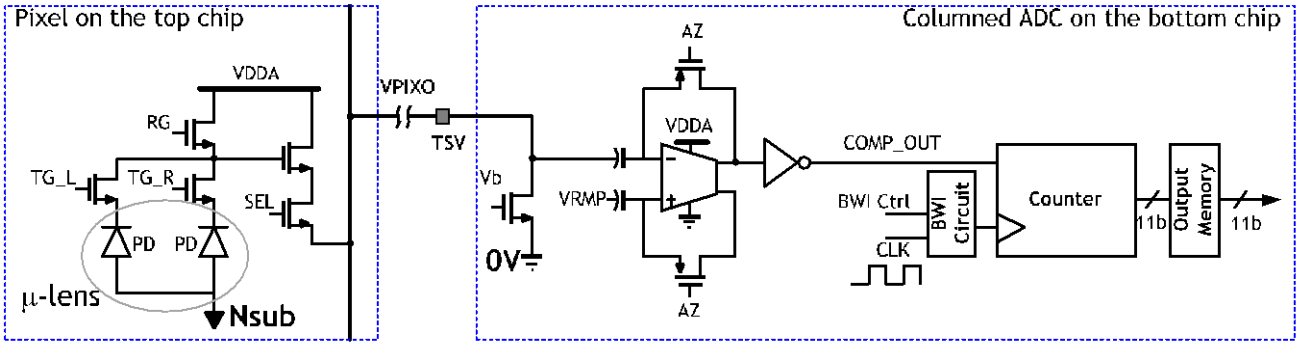
M. Kwon et al., A Low-Power 65/14nm Stacked CMOS Image Sensor", Samsung, ISCAS 2020





65 nm backside illuminated CMOS Image Sensor
output signal from pixels on the top chip is transferred to correlated double sampling (CDS) circuits on the bottom chip throughout TSV

14 nm CMOS readout chip (with 3D FinFET transistors)
single-slope ADCs, row driver to control pixels on the top chip, image signal processor (ISP) and mobile industry processor interface

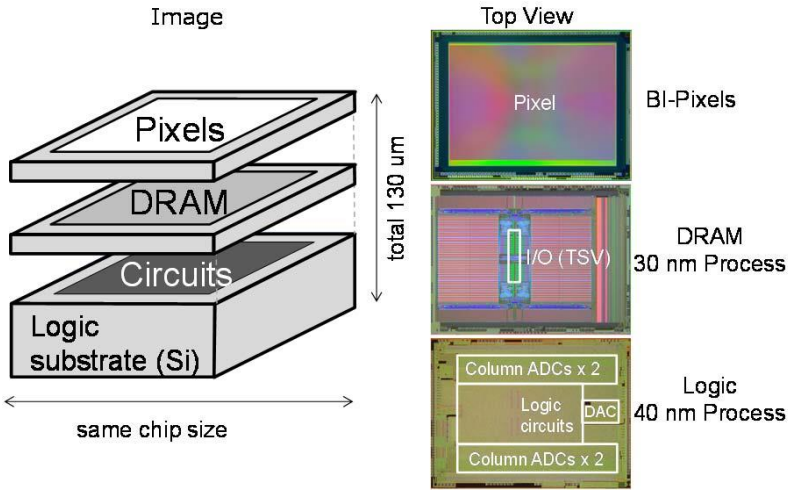


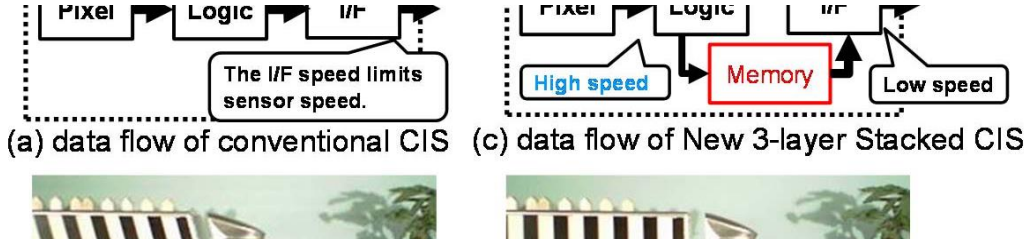
Wafer level stacking
pixel pitch 1.4 µm,
12 Mpixel
11-bit column parallel ADC

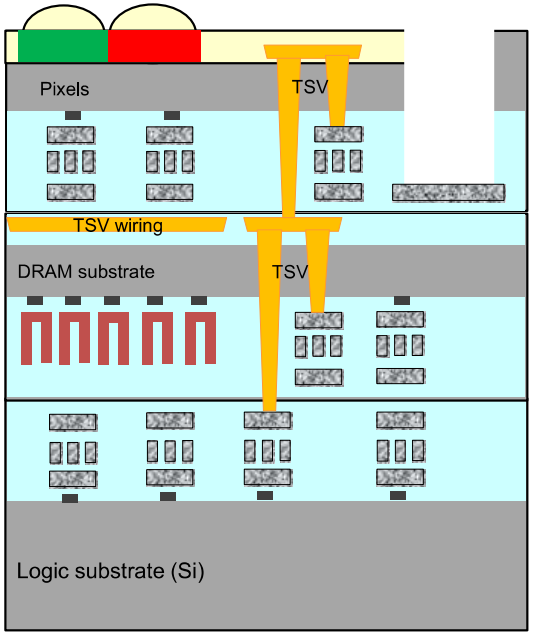
CMOS image sensors with 3 device layers: pixels, DRAM, logic

"Pixel/DRAM/logic 3-layer stacked CMOS image sensor technology" H. Tsugawa et al. Sony, 2017 IEEE IEDM

- Three bonded Si substrates, each electrically connected by TSVs through sensor or DRAM (thinned to 3 μm)
- Thanks to DRAM, readout speed from the pixel can be increased (960 fps super slow motion video) without being limited by the speed of the I/O interface







TSV have a minimum diameter of 2.5 μm and a pitch of 6.3 μm (35000 TSV ≅ number of row and columns)

19.3 Mpixel, 1.22 μm x 1.22 μm pixels

Samsung version with 28 nm logic and 20 nm DRAM

3D stacked CMOS sensors and advanced functionalities

- Event-based sensors respond to brightness changes asynchronously and independently for every pixel (high temporal resolution and low latency, very high dynamic range, and low power consumption)

- In these data-driven devices, each pixel continuously monitors for a change of sufficient magnitude from a memorized value. When the change exceeds a threshold, the camera sends an event, transmitted from the chip with x-y location, time-stamp, and polarity of the change

- 3D stacking allows for higher complexity of pixel electronics at small pitch without degrading fill factor

- Architectures moving closer to pixel sensors for particle detection

3D integration developments for pixel detector in HEP and photon science

- 3D chip stacking and high density bonding are being successfully used for industrial image and TOF high performance sensors based on advanced CMOS ≤ 65 nm
- These technologies can be very interesting also for new detectors in our field, e.g. for high resistivity CMOS sensors, LGAD, SiPM,...
- As for CMOS IC design, we are lagging behind the more advanced developments: we should try to catch up with what industry is doing, but we can also design high performance devices without going to very aggressive technologies
- Along the last decade, several projects were carried out with different technologies; new projects are about to start

3D heterogeneous integration and "via last": AIDA and AIDA2020

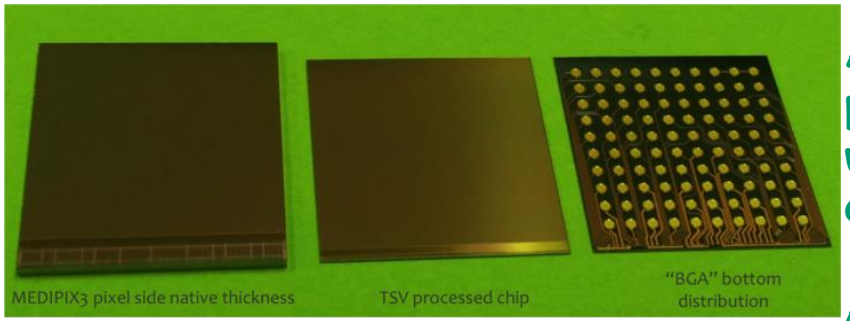
- Even with low-density 3D technologies, sizable performance improvements might be gained by fabricating devices with 2 layers, each optimized for its functions (particle sensing, readout electronics), with additional advantages such as removing dead areas.
- Low-density peripheral TSVs on fully processed CMOS wafers reach backside bonding pads for external connection.
- The **"via last"** approach and **3D heterogeneous integration** were tested both for HEP and imaging applications with support from the AIDA FP7 project and the AIDA2020 H2020 project

Two highlights of AIDA and AIDA2020:

- A demonstrator module with MEDIPIX chips with TSVs bonded to sensors
- TSV processing on ATLAS pixel readout chips

Low-density peripheral TSVs in the MEDIPIX chip

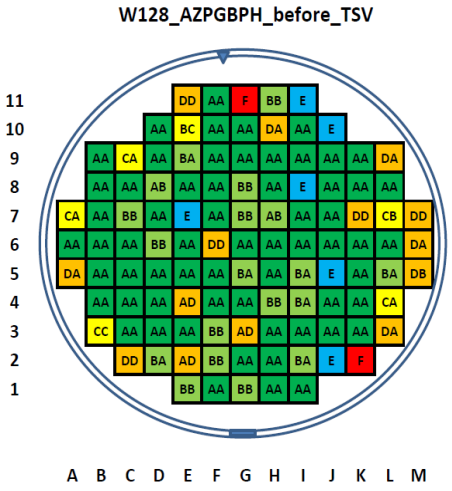
- MEDIPIX3: 130 nm CMOS chip for high resolution X-ray spectral imagers with hybrid pixel detectors (256x256 square pixels of 55 μm size)

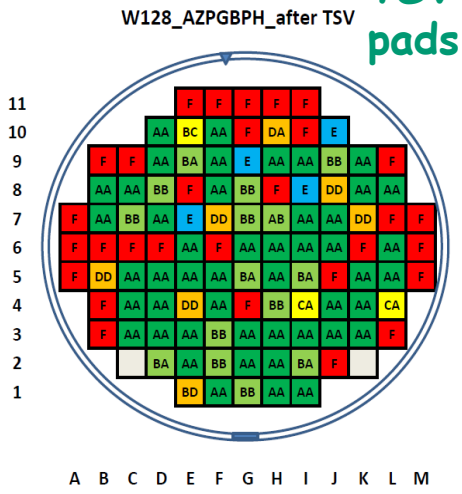


All IO logic and pads contained within one strip of 800μm width

All IO´s have TSV landing pads in place

- For 4-side buttable imaging tiles, remove periphery with I/O pads, insert TSVs and backside redistribution layer with BGA pads (CEA-LETI process)





The TSV diameter was 60 μm (to match a wire bond pad pitch of roughly 100 μm) and the wafers were thinned to 120 μm for an optimized aspect ratio of 2.

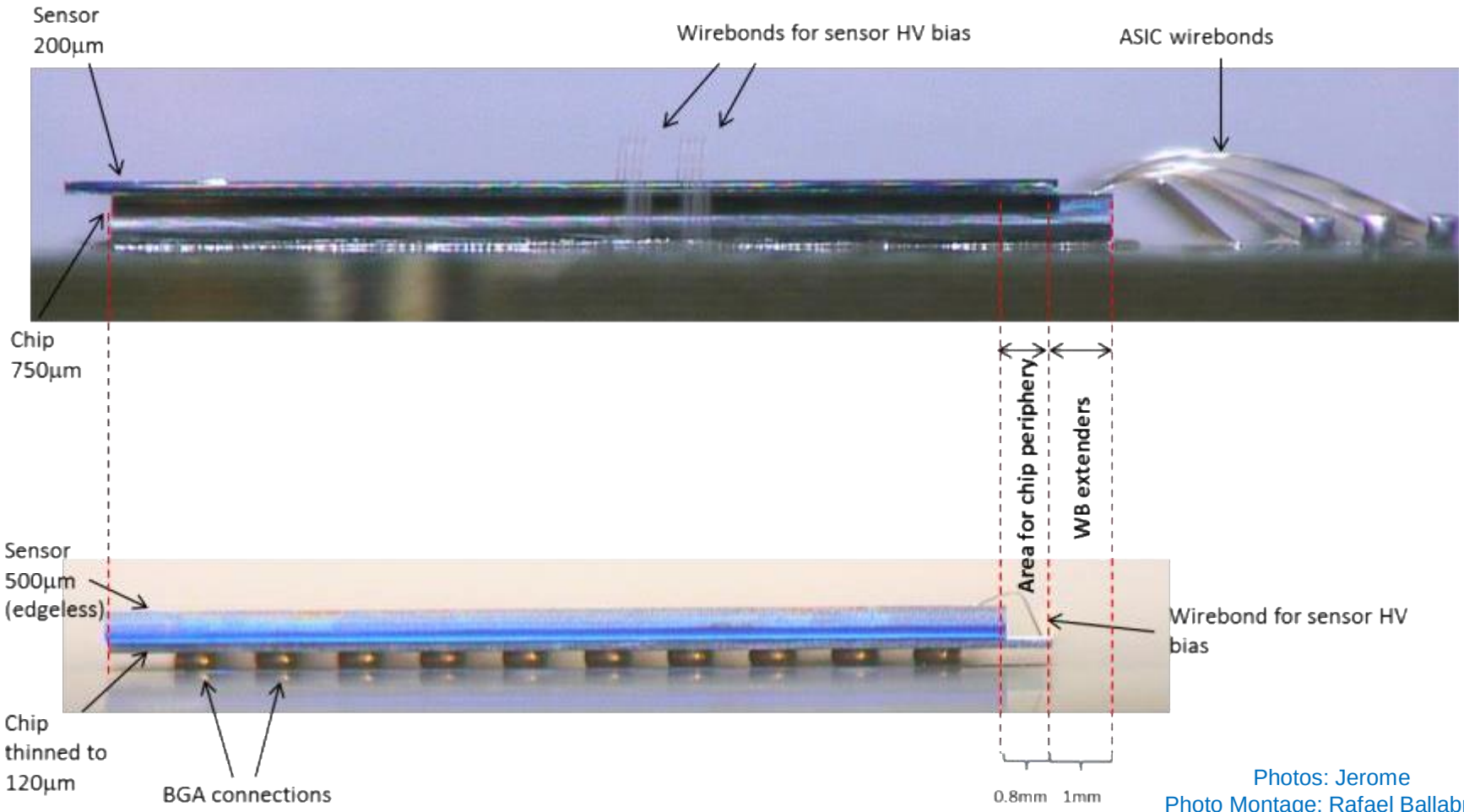
TSV yield is adequate for small scale production; chip performance is preserved

D. Henry et al., TSV Last for Hybrid Pixel Detectors: Application to Particle Physics and Imaging Experiments , in proceedings of the 63rd IEEE Electronic Components and Technology Conference (ECTC) (2013), p. 568.

Hybridization of TSV processed MEDIPIX chips

Towards a new generation of pixel detector readout chips, M Campbell et al, IWORID 2015

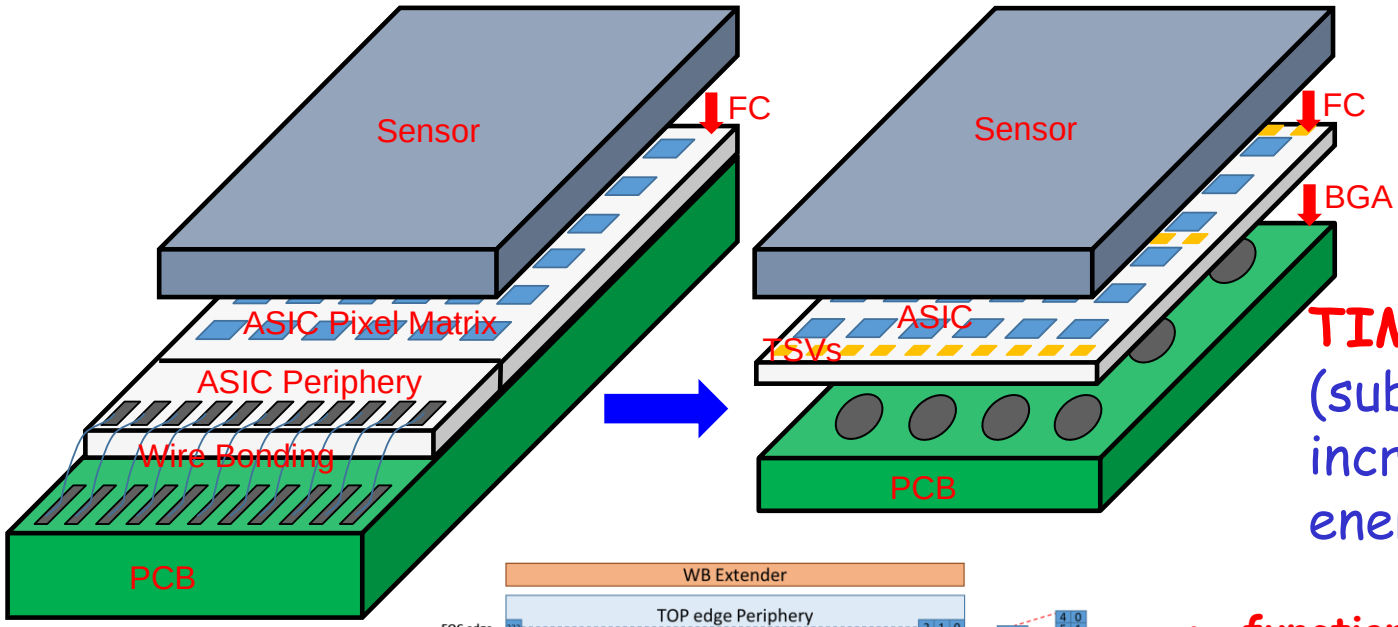
- Comparison between WB and TSV on board integration



Photos: Jerome
Photo Montage: Rafael Ballabriga

Flip chip interconnection to sensors: assemblies by VTT/ADVACAM

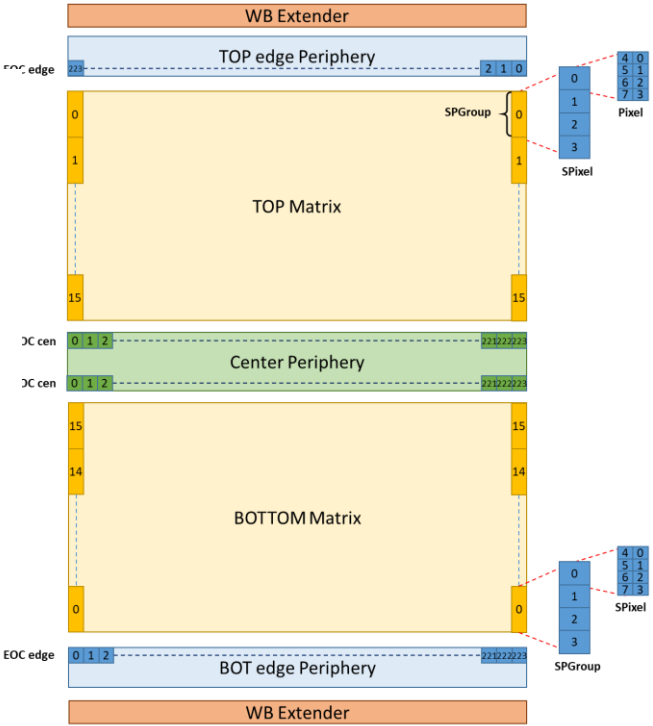
3D integration for the next generation of TIMEPIX



TIMEPIX4 chip (sub-ns time stamping, increased rate and energy resolution):

3 "hidden" peripheries with TSV:

- TOP, BOTTOM Edge: Data Readout (8x 10 Gbps Serializers)
- CENTER: SC, Analog Blocks (DACs, ADC, Band-Gaps…)



- **functions normally associated with the chip periphery will be located throughout the pixel matrix** (digital-on-top design)
- **more flexibility in the choice of readout architectures.**
- The chips should be abuttable on 4 sides.

X. Llopart, "The Timepix4 chip and its design approach ", VERTEX2019, Lopud, Croatia

Advanced through silicon vias for hybrid pixel detector modules (AIDA-2020)

In AIDA-2020 WP4, the Bonn group has driven a successful effort for processing **Through-Silicon Vias in 130 nm CMOS FE-I4 pixel readout chips.** AIDA2020 WP2 also financed a Proof-of Concept project to develop a reliable TSV technology with Fraunhofer IZM.

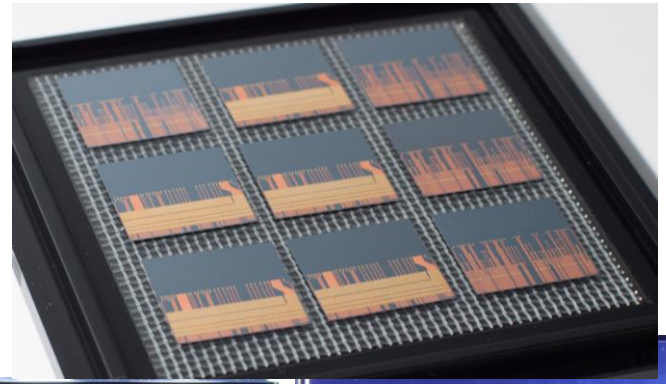
- Produce through-silicon vias (TSV) on wafers with 100-nm scale pixel readout chips
- Connect chips with TSV "via last" to detectors
- Open the way to the adoption of 3D integration technologies in the design of pixel detector systems, with important advantages in terms of pixel form factor, readout speed, reduction of dead areas and of material budget.
  - Allow for 4 side buttable modules
  - Enable wafer-to-wafer assembly
  - Remove wirebonds for greater module robustness
  - large length and relatively large aspect ratio (length/diameter) TSVs with reliable fabrication yield

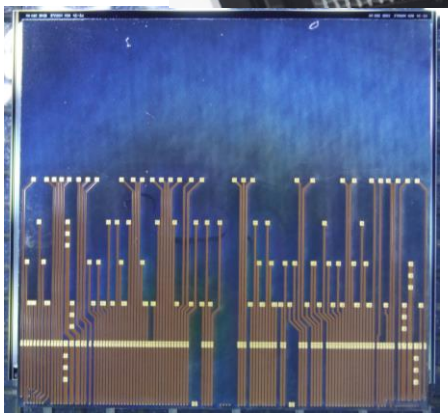
FE-I4 pixel readout chips with via-last TSV in AIDA2020

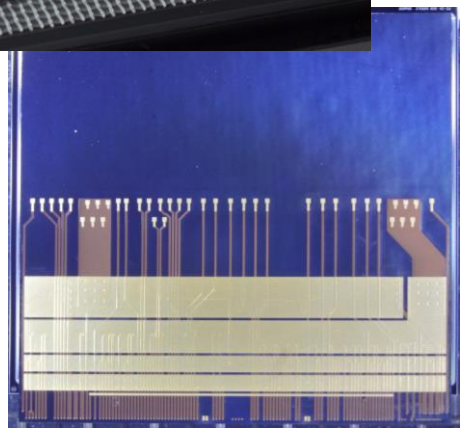
On test wafers, measured values of TSV resistance (about 15 mΩ for individual TSV) and capacitance (about 40 fF in a first wafer and about 120 fF in a second one) appear adequate for peripheral TSV, also in the case of I/O digital lines operated at a moderate frequency (160 Mb/s).

- 3 FE-I4 Wafers have been successfully processed by IZM with TSV and 2 different RDL types:
  - Simple 1 layer RDL just copying the WB pad frame with the Cu used for the TSV filling
  - 2 layer RDL connecting all WB pads for the power nets: VDDD, DGND, VDDA, AGND. Used the Ni/Au layer for the pads
- Performance in terms of noise, threshold dispersion and data transmission similar to standard FE-I4 chips.

Courtesy: N. Wermes, Bonn

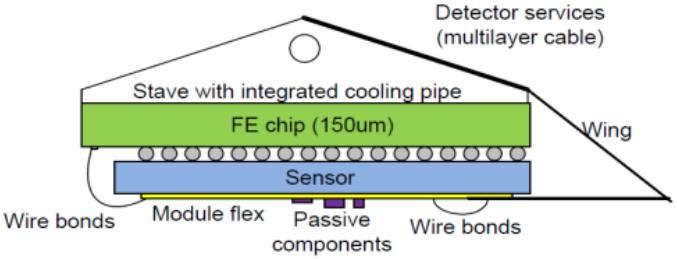


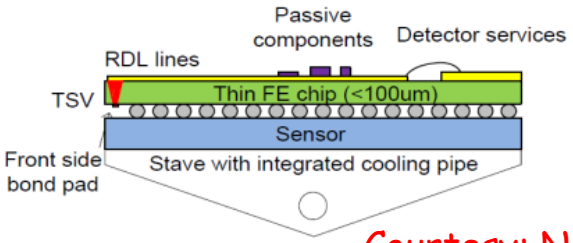




Advanced TSV for Pixel Detectors - F. Hügging - AIDA-2020 4th Annual Meeting, Oxford, UK

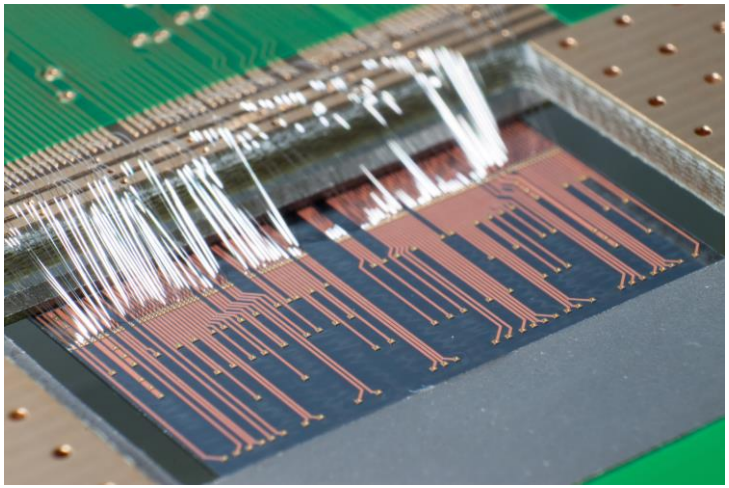
Pixel modules with TSVs (Bonn, IZM)

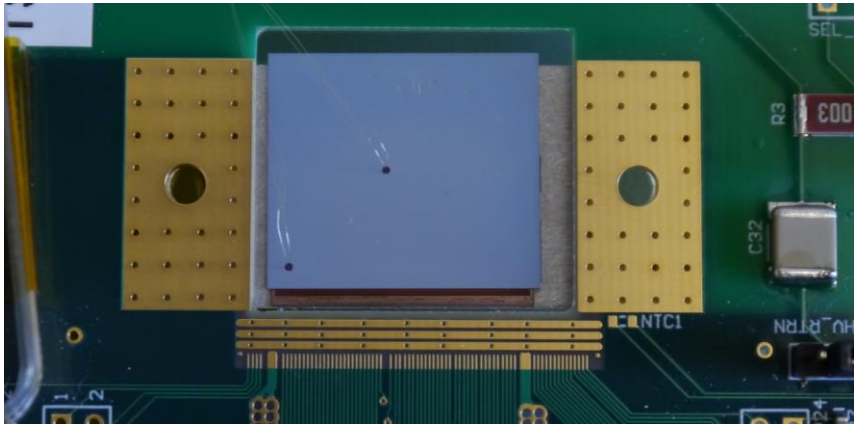




Courtesy: N. Wermes, Bonn

- 8 modules with sensors have been built:
  - Assembly onto MPG HLL planar sensor (thanks to A. Macchiolo)
  - Sensor wafers were deposited with SnAg solder bumps



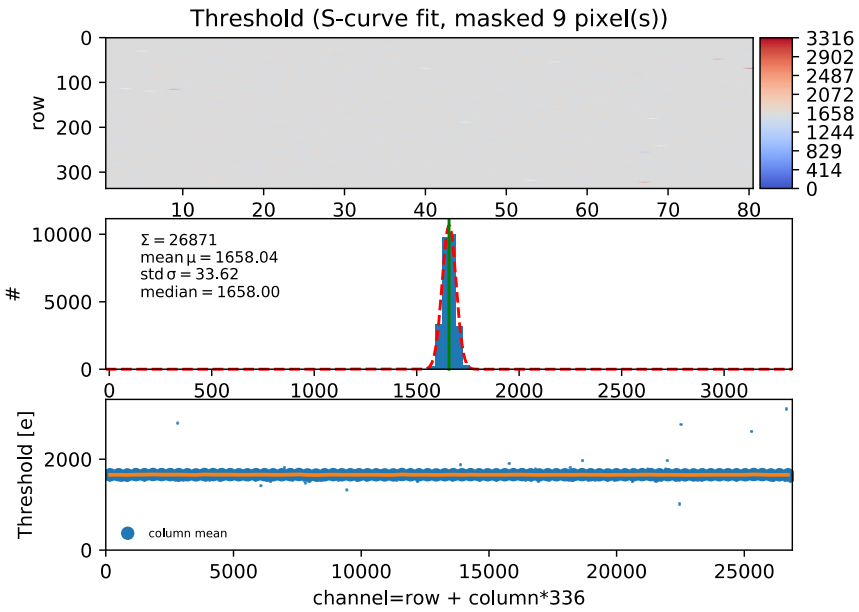


Cross section of module with 80μm thick ATLAS FE-I4 backside TSV ROC

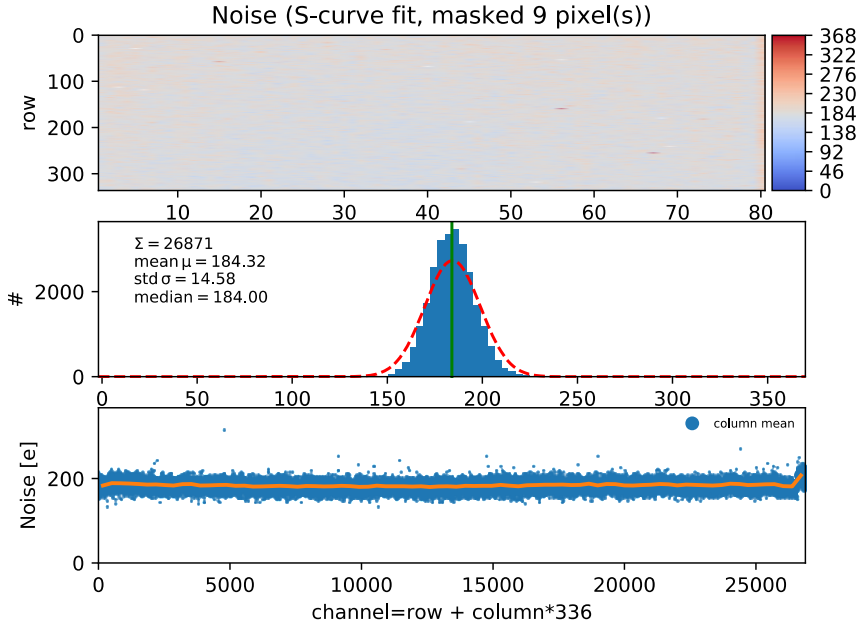
Modules with TSVs: Results

- 2 modules have been tested, both working nicely
  - Very good bump connectivity, one module shows a few disconnected pixel at one edge (maybe handling issues during BB)
  - Noise is about 180e⁻ at 1650e⁻ threshold with a dispersion below 40e⁻

Tuned threshold, 60V



Noise, 60V



Advanced TSV for Pixel Detectors - F. Hügging - AIDA-2020 4th Annual Meeting, Oxford, UK

The excellent outcome of this activity provides a **demonstration of the feasibility of pixel modules where TSV technology is used to improve the detector performance** in terms of reduced material budget, increased active area, and improvement of assembly and handling.

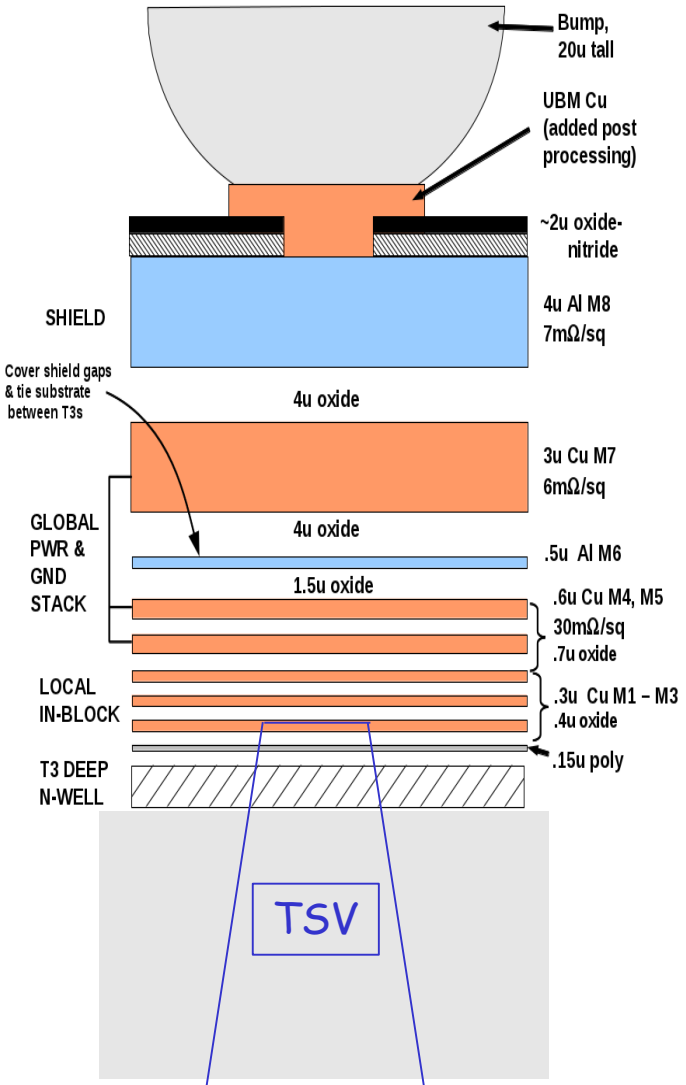
Prospects: TSV in the next generation (65nm) of pixel readout chips

The original plan of AIDA2020 envisaged to apply TSV processing to 65 nm CMOS wafers with the RD53A pixel readout chip.

Wire bonding pads in RD53A are compatible with TSV fabricated with a backside etching process, such as the one already successfully tested in 130 nm FE-I4 CMOS wafers.

130 nm and 65 nm CMOS nodes share similar process features as far as TSV processing is concerned.

Peripheral wire bonding pads have all metal layers from M1 to the actual aluminum pad. Peripheral TSV for I/O interconnection can be etched across the silicon substrate reaching the lowest metal levels (M1-M3) in the stack, which are then internally connected to the thicker upper metals and finally to the bonding pad



It is then reasonable to assume that TSV processing in a 65 nm wafer will give the same results that were found in 130 nm wafers.

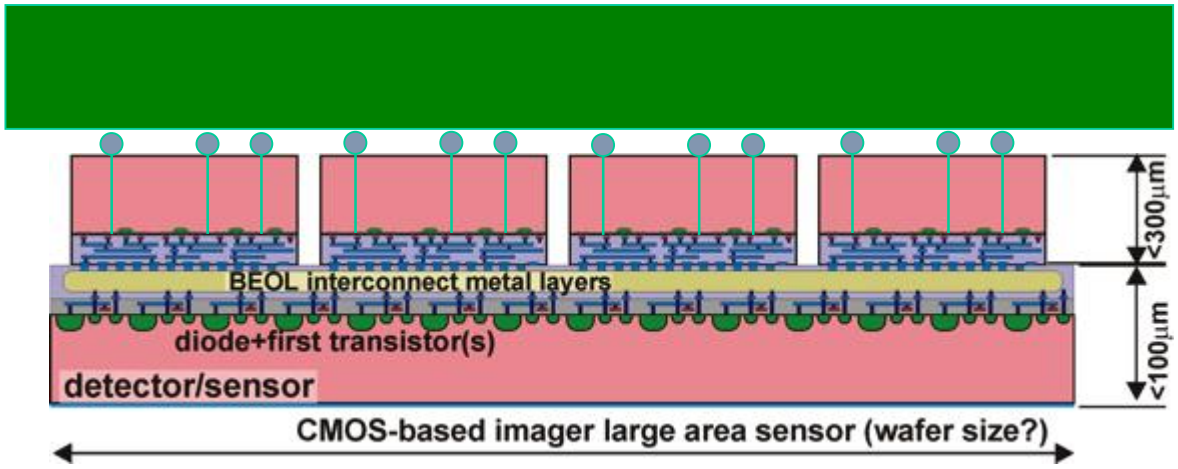
Prospects: CMOS sensors for X-ray imaging

A CMOS sensor for imaging or particle tracking can be augmented by an additional layer of dedicated high performance electronics, 3D integrated at the pixel level.

FLORA

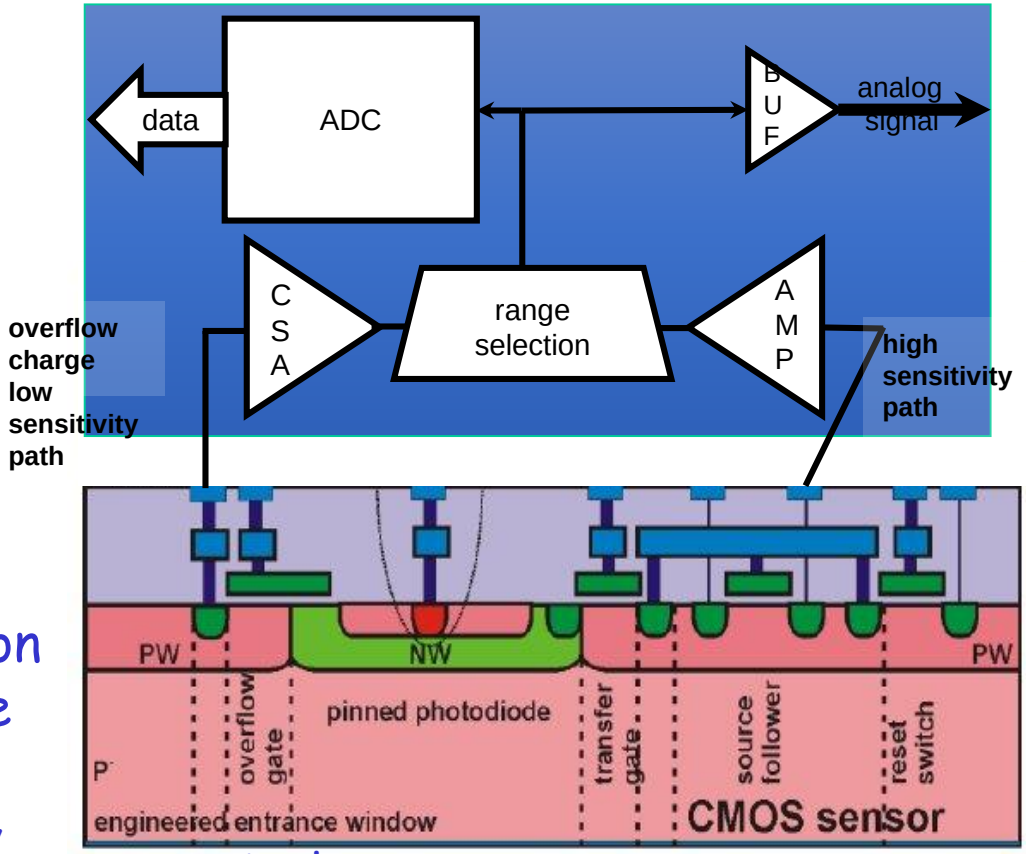
2M pixel 50 µm x 50 µm, soft 0.2-2 keV X-rays, continuous readout ≥ 40kfps, high dynamic range 10^4 photons per pixel per frame, camera for LCLS II, (P.I. G. Carini, G. Deptuch, BNL)

G. Carini et al, "Hybridized MAPS with an in-pixel A-to-D conversion readout ASIC", NIM A935, 2019



The FLORA approach: two *active* chips

Mixed-signal Readout ASIC
advanced process node (65 nm),
10-bit pixel-level SAR ADC



Monolithic Active Pixel Sensor
OPTO-type process
minimal circuitry for the conversion of the charge packet into voltage

two signal paths (high/low sensitivity), with a controlled charge overflow in the sensor pixel

Advanced interconnects: 3D assembly/interposer

exploiting good features of both technologies

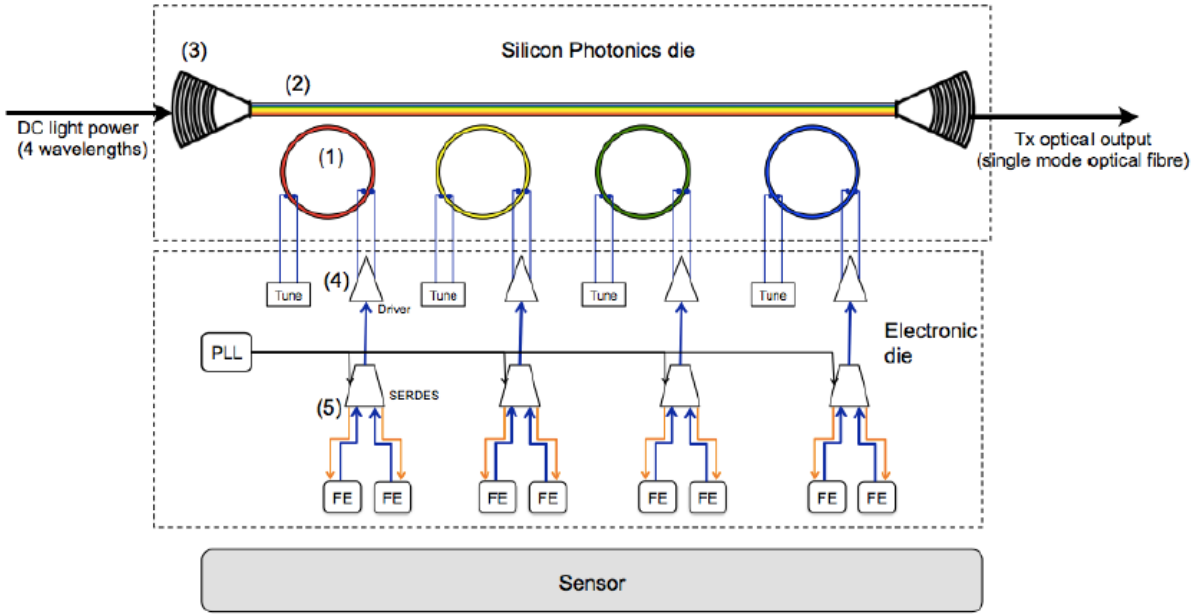
- multiple metal layers on sensor/interposer for routing
- yield-optimized size of ROIC ASICs

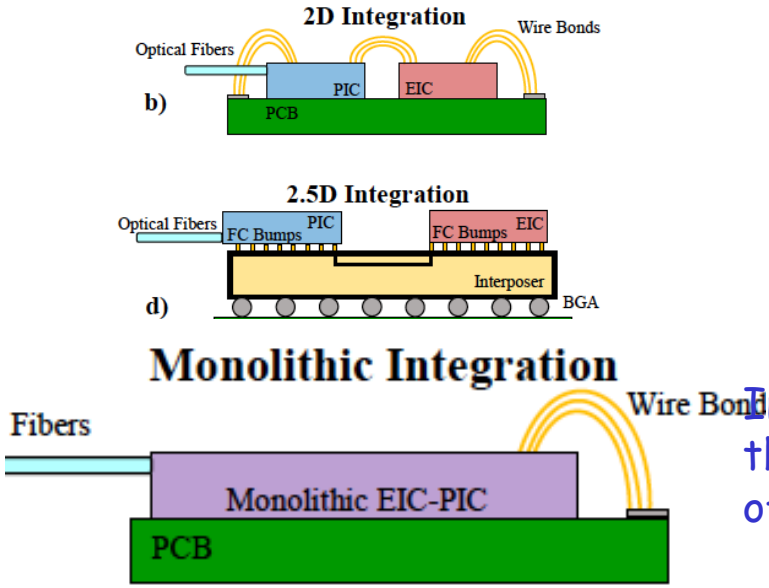
G. Carini et al, "Hybridized MAPS with in-pixel A-to-D conversion readout ASIC for high-throughput imaging", ULITIMA 2018, Argonne National Lab.

A potential application of 3D integration: the INFN FALAPHEL project

Integration of Silicon Photonics and high-speed microelectronics for high rate data transmission, operating at extremely high dose levels (≥ 1 Grad), and 100 Gb/s data rate, using wave/space division multiplexing techniques.

Hybrid (3D or 2.5D) integration of Silicon Photonics modulators with high speed radiation hard 28 nm pixel readout ASIC





In the more aggressive solution, based on 3D integration, the readout ASIC (bonded to a sensor) is flipped on top of the photonic chip

Journal of Lightwave Technology 2020
Silicon Photonic 2.5D Multi-Chip Module Transceiver for High-Performance Data Centers, N. C. Abrams, et al

(P.I. F. Palla; INFN Padova, INFN Pavia, INFN Pisa, Univ. Pisa, Univ. Bergamo, S.S. S.Anna, Pisa)

Conclusions: the prospects of 3D vertically integrated pixels

- Demonstrators of 3D integrated devices are available and confirm the potential advantages of this technology, both for HEP and imaging applications. The pixel sensors and front-end electronics community will definitely continue to use 3D integration as a way of devising (and dreaming) advanced detectors with advanced functions (picosecond timing and faster processing).

- TSV processing compatible with bump bonding exists already in 130nm technology (8" wafers): it will be developed for 65nm technology (12" wafers) in the context of the Timepix4 development
  A CERN R&D program plans to extend it to 28nm (or lower) technology

- Small size pixel-level TSVs will be a crucial ingredient to achieve the ultimate performance of the real 3D-IC technology.

- Our community has to establish and strengthen connections with 3D process providers and microelectronic companies, to gain a reliable access to industrial 3D integration technologies