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Interconnection studies for monolithic silicon pixel detector modules using the MALTA CMOS pixel chip

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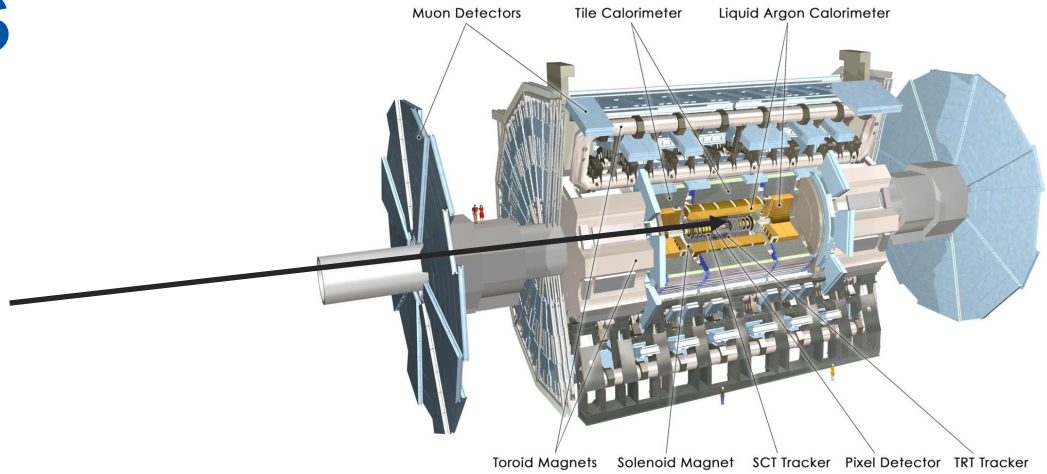
Outlook

- Introduction
- MALTA monolithic silicon pixel sensor
- Post processing and interconnection tests with multiple MALTA chips
- Outlook and summary

Silicon trackers

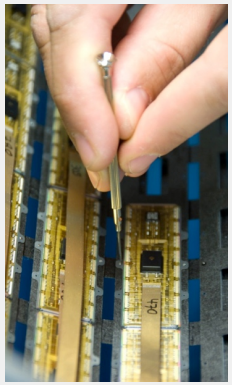


Silicon trackers are the covering the innermost regions in collider experiments.

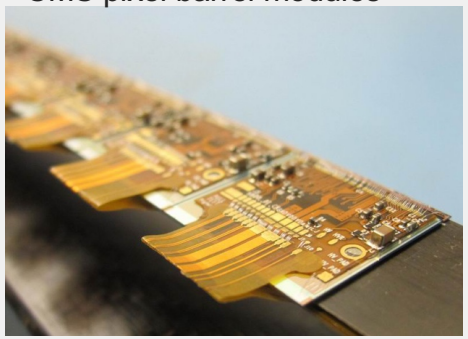
The first layers, closest to the interaction point, are formed by silicon pixel detectors.

Pixel detector modules form the basic building blocks of these layers

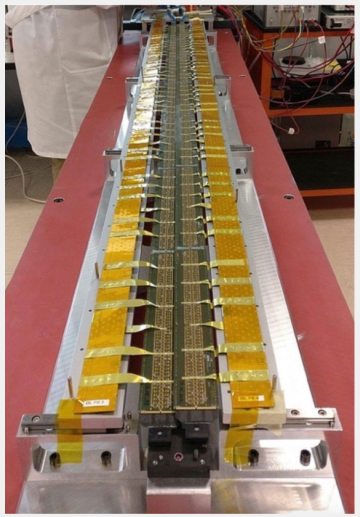
- Silicon sensors and frontend electronics
- Signal and power routing
- Mechanical support and cooling



CMS pixel barrel modules



ATLAS IBL pixel modules

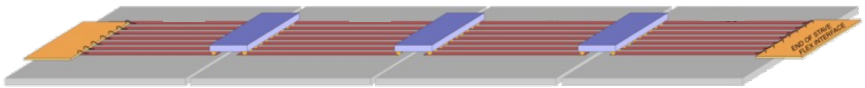


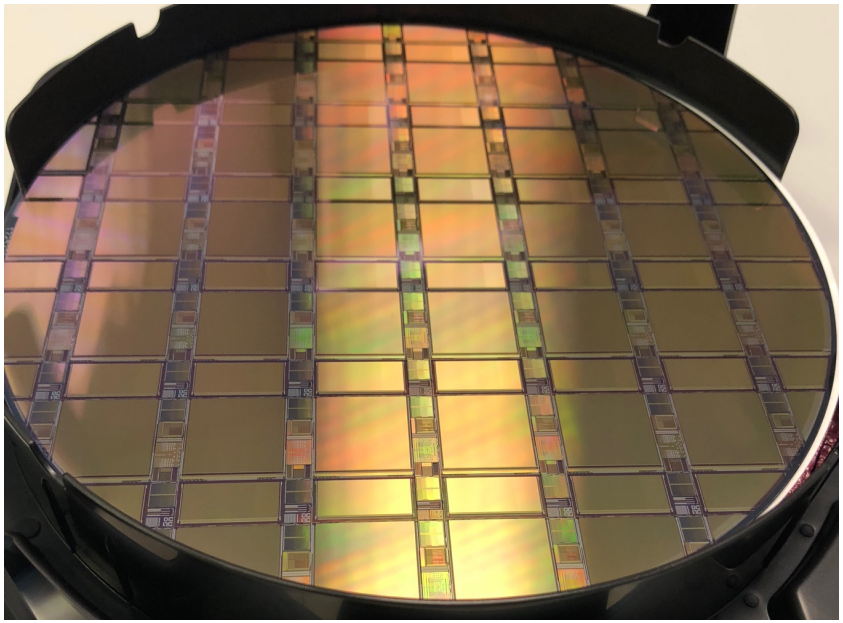
ALICE ITS upgrade Outer Barrel stave with pixel modules

MALTA silicon pixel sensor

MALTA is a monolithic silicon pixel sensor that was developed as part of the R&D on radiation hard monolithic sensors in ATLAS and the STREAM MC ITN. The module studies are now also followed within the CERN EP R&D work package 1.3 on pixel modules studies.

- MALTA was designed with built-in functionality (chip-to-chip transfers) to facilitate building large area pixel modules.
- The monolithic MALTA chips are thinned routinely to 100 µm (50 µm) to reduce the material contribution from silicon with the goal to build light-weight modules.
- The goal is to build a multi-chip MALTA module using interconnection technologies to minimize material while achieving large coverage.



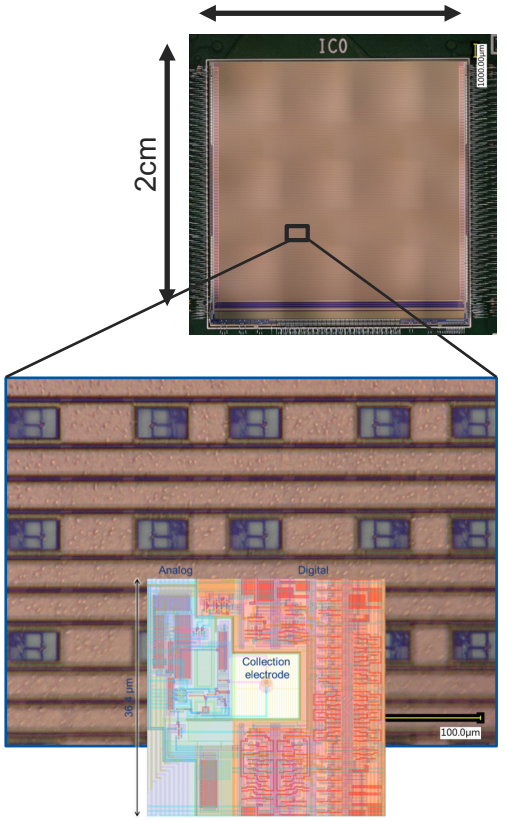


STREAM1 wafer with several chips per reticle. The MALTA chip is 2 cm x 2 cm large.

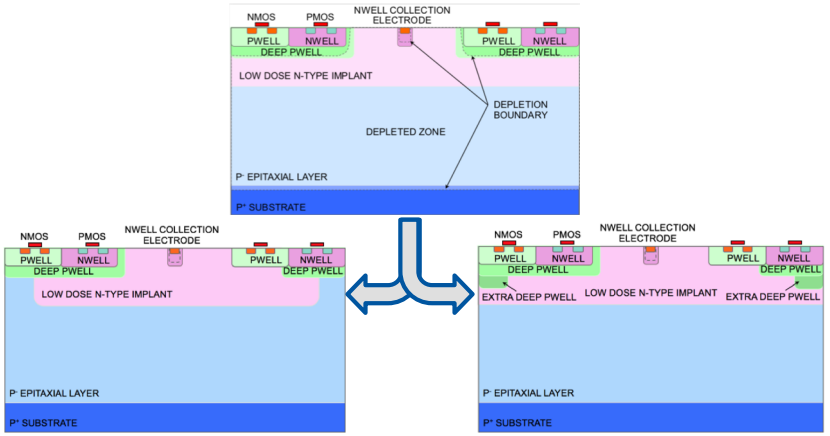
MALTA

Monolithic silicon pixel senor developed in **180 nm TowerJazz CMOS** imaging process on high resistivity epitaxial (ρ_{epi}~kΩcm, 25-30 µm) and CZ wafers:

- 25 ns shaping time
- Low power asynchronous readout and small collection electrode (~ 3 µm, <5 fF)
- No clock distribution over the active matrix.
- ~1 µW/pixel (75 mW/cm^2 in the matrix)



Process modifications improve **radiation hardness** by achieving large depleted volume (charge collection by drift) and a focused electric field (~ 2 x10^{15} n_{eq} cm^{-2})



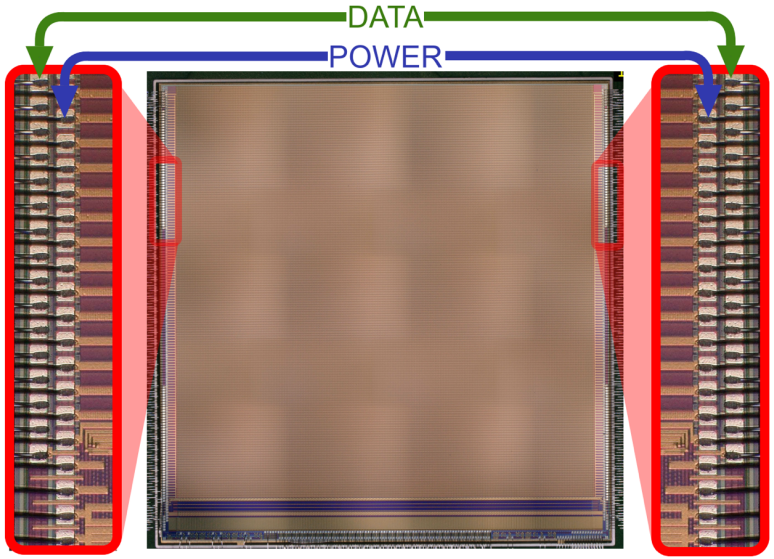
See presentation by F. Dachs on MALTA irradiation tests, this workshop

MALTA chip-to-chip communication

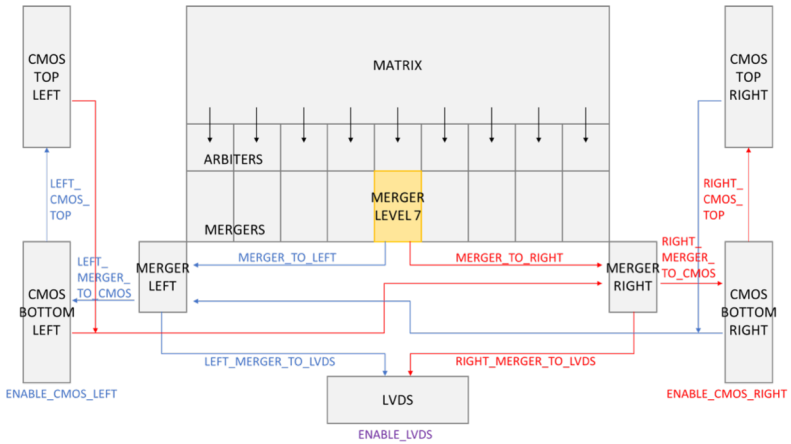
MALTA connection pads: data (CMOS transceivers) can be transmitted between neighboring sensors.

MALTA includes 40 **CMOS transceivers** on each corner which can be used for **chip-to-chip data transmission** (pulse width 1 ns) as well as **power pads** (analogue and digital) allow to transmit power from one chip to the next.

Data received via these pads can be combined in the chip using the asynchronous internal merger.



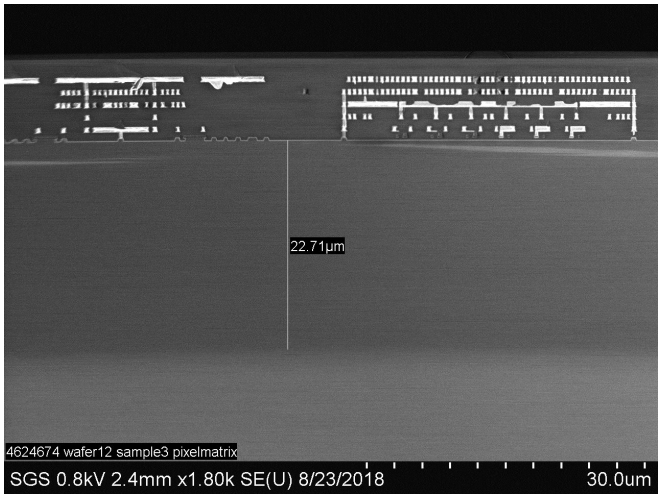
Data and power connection pads on the chip edges. In the MALTA1 version, each chip requires still a separate CTRL and CLK line.



MALTA module studies

Initial focus on four main topics as ingredients to build a low mass MALTA module:

- **Reduced silicon material contribution** by thinning the monolithic pixel sensor to 100 µm, further wafers thinned to 50 µm
  - Validated for MALTA chips on 25 and 30 µm high resistivity p-epi on substrate (sensing layer == epi layer)
  - Validated for MALTA chips on high resistivity p-type CZ (sensing layer == full wafer thickness)



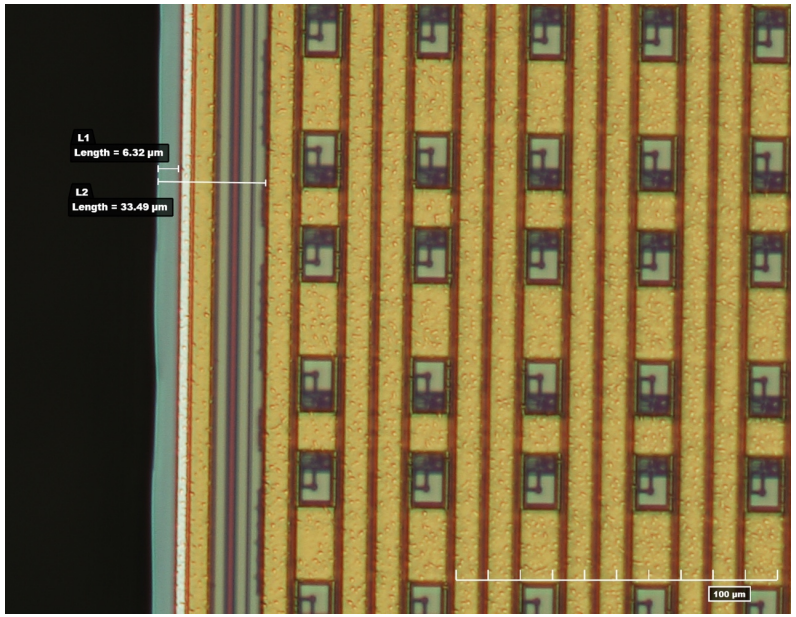
SEM cross section (epi- wafer)

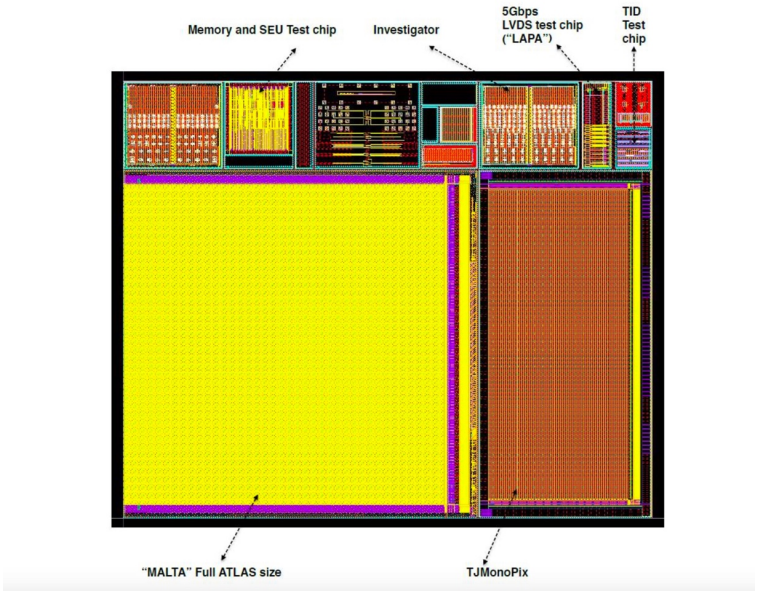
- **Reduce dead area at chip edges** as well as edge damage to place chips as closely together as possible;
- Validate **data and power transmission** using Al wedge wire bonding
- **Flip-chip bond interconnection chip** for data and power transmission

MALTA module studies - dicing

The MALTA chip has a 60 µm wide exclusion zone surrounding the chip seal ring to facilitate laser dicing.

- Typical cut distances are 3-7 µm from the sealring, thus allowing to place chips closer together in a module. Limitation of extending the active area to the edge is given by the electronics design.
- Laser dicing has been combined with thinning to 100 µm (and 50 µm).
- Additional benefit of the laser dicing was the possibility to extract the small test chips in the reticle in one step.

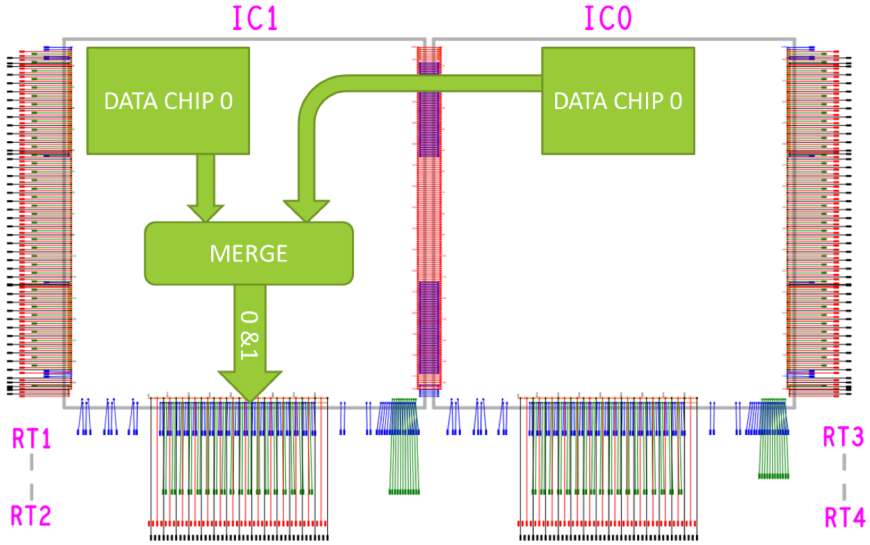


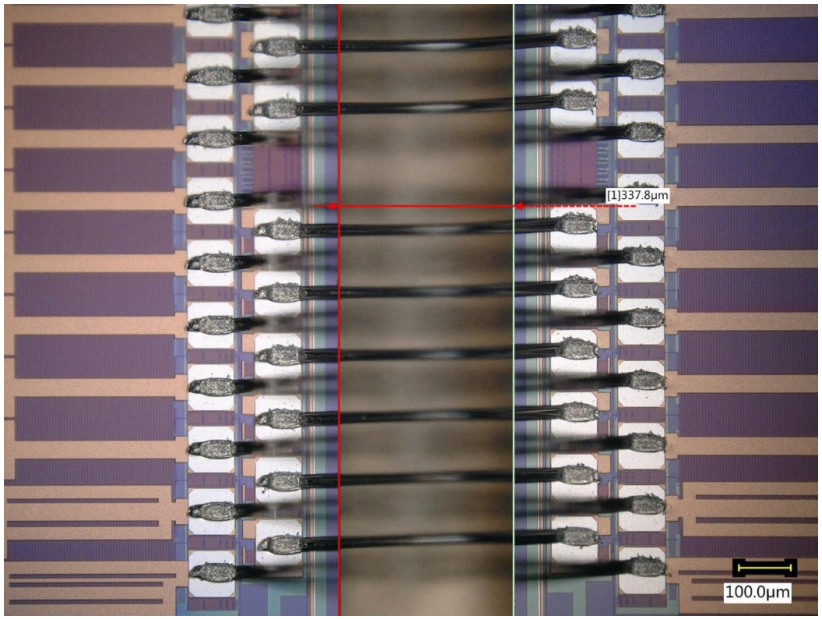


Chip-to-chip connections

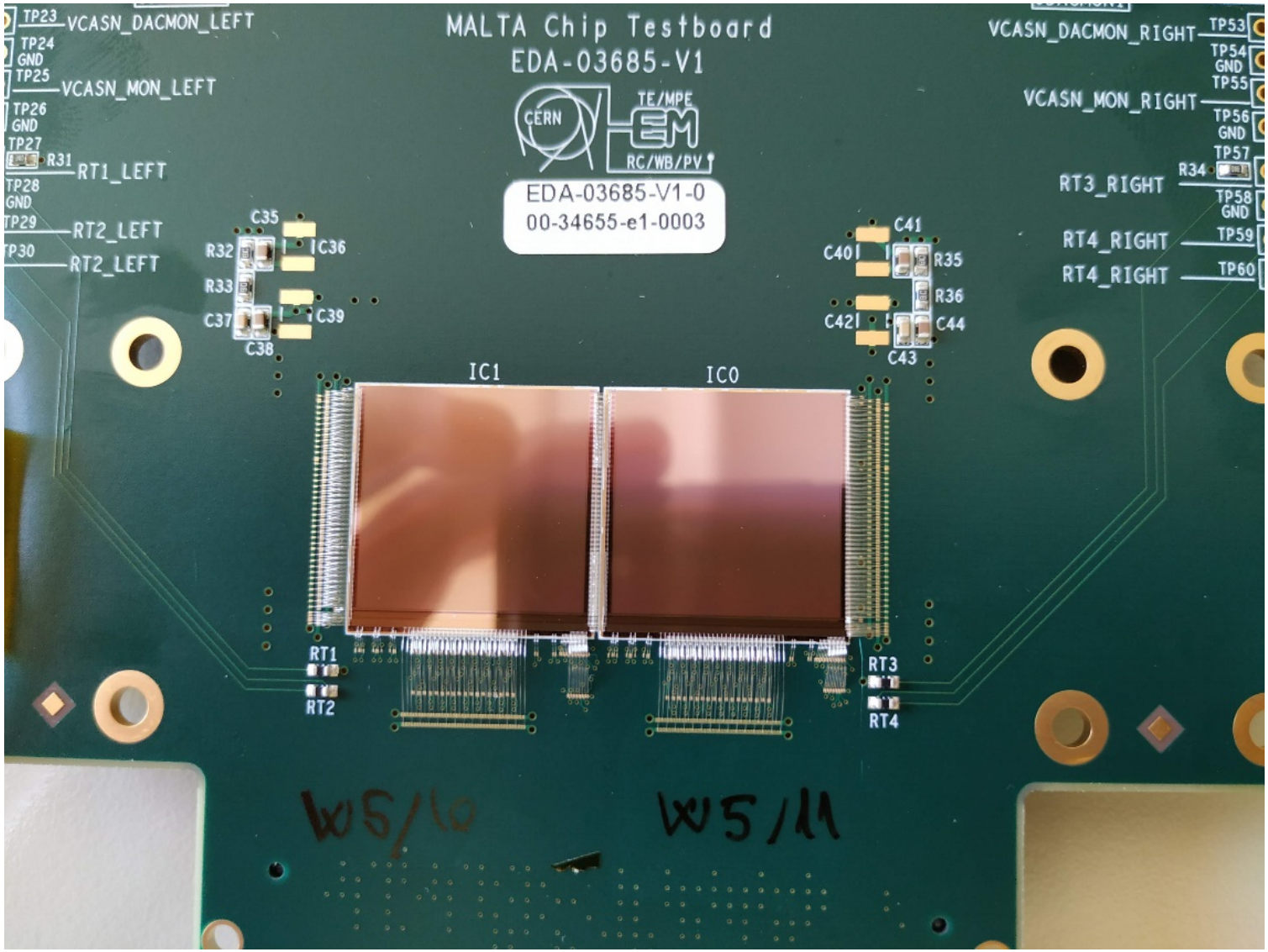
Test of data transfer from one MALTA chip to another using the CMOS transceivers on the chip edges

- 2 MALTA chips mounted on a dedicated PCB and connection between the chips realized using Al wedge wire bonding (master-slave connection)
- Chip distance (edge-to-edge) ~ 300 µm, limited by wire bonding requirements
- Separate lines for each chip for CLK, Reset, SlowControl and test pulse
- Data can be read from each chip via the LVDS outputs at the chip periphery



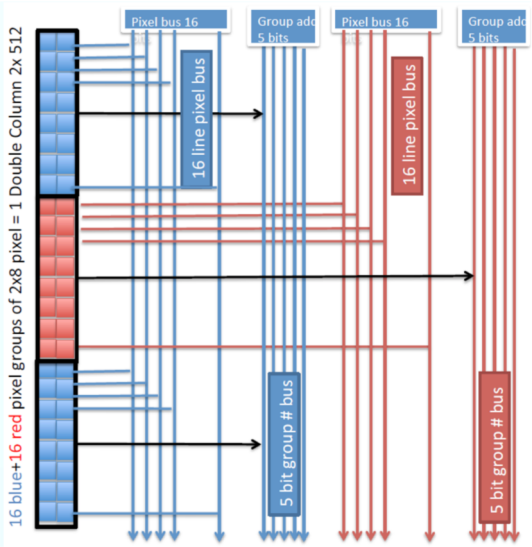


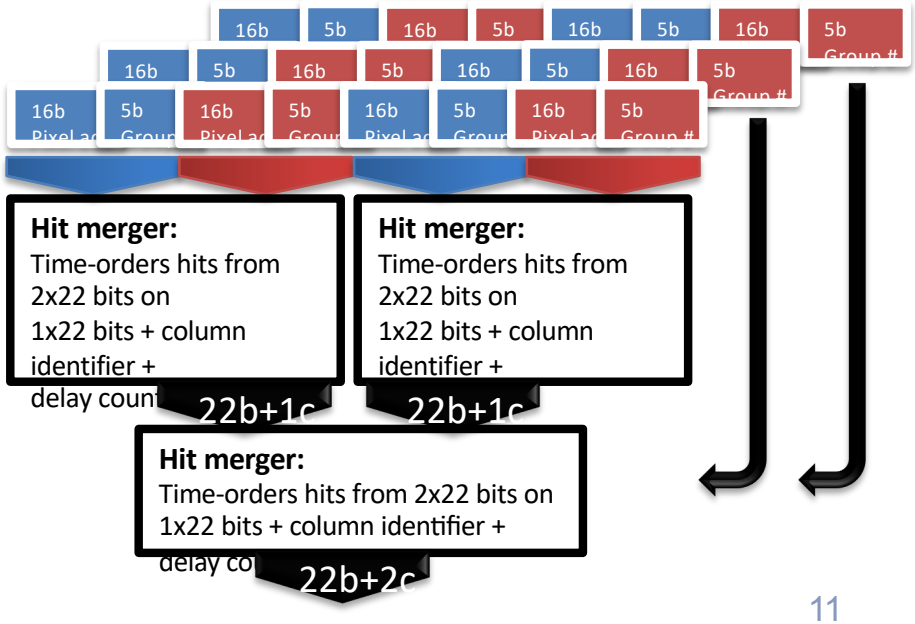
Chip-to-chip connections



Chip-to-chip connections

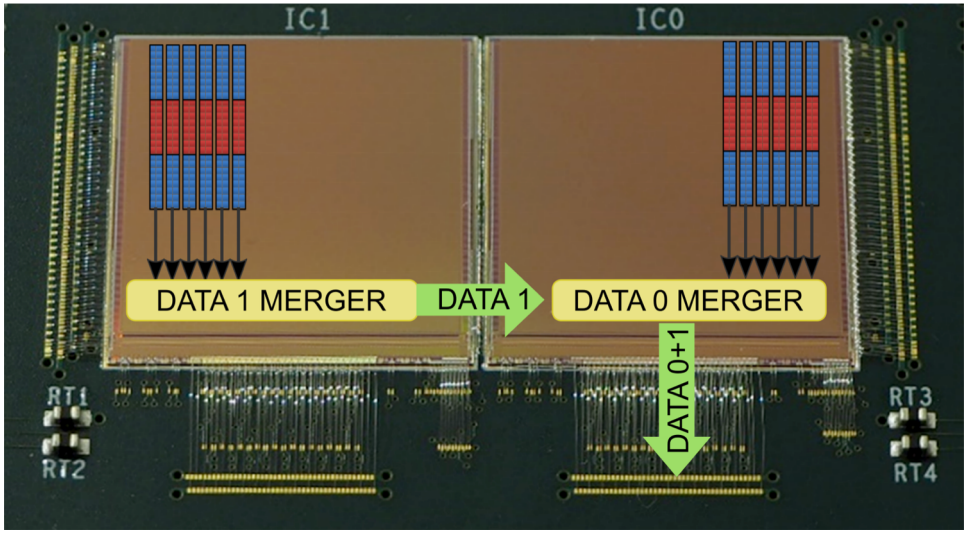
- In MALTA the front-end output is injected into a double-column digital readout logic. Hits are stored using in-pixel flip- flops and **transmitted asynchronously over high-speed buses to the end-of-column logic** (digital periphery)
- The double-columns divided into groups of 2x8 pixels (“red” and “blue”), buses are shared by all groups of the same colour in the double-column. The group number is encoded on 5-bit group address bus.
- Merger structure at the end of the columns - the last stage generates a 37-bit wide word for each hit.

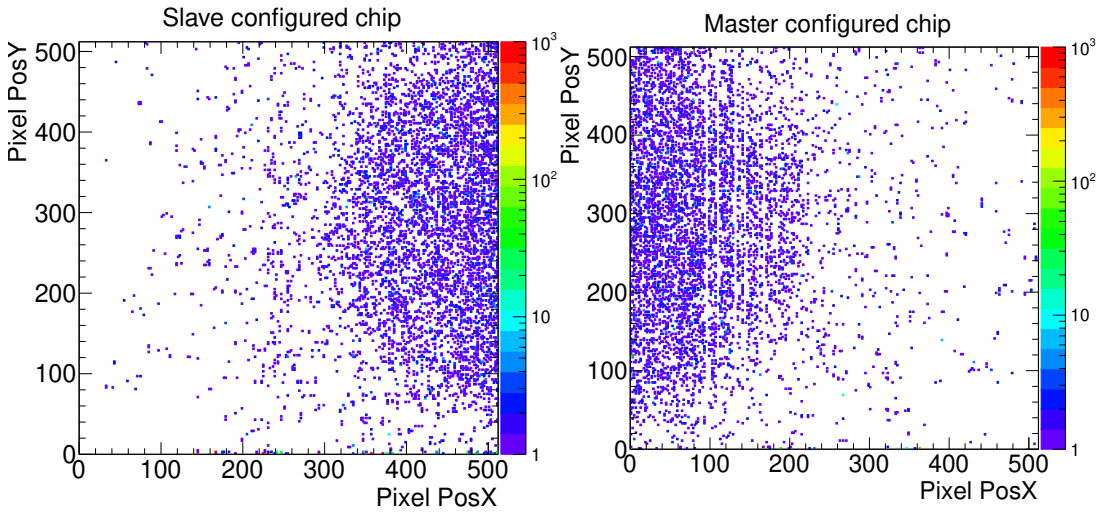




Chip-to-chip connections

- Source tests to validate data transfer from one chip to the other (Sr90 source)
- High speed signal routing from sensor to sensor via edge pads from (GHz)
- All measurements done with same exposure time; white lines are masked double columns

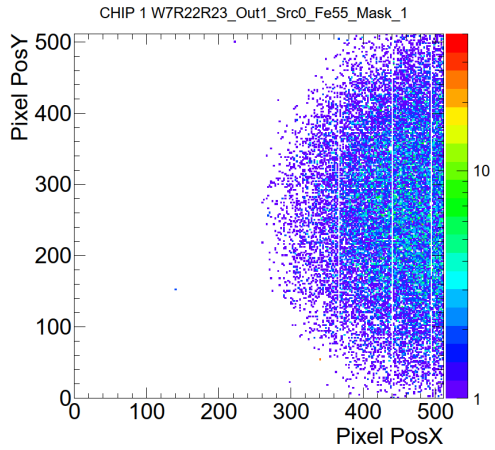


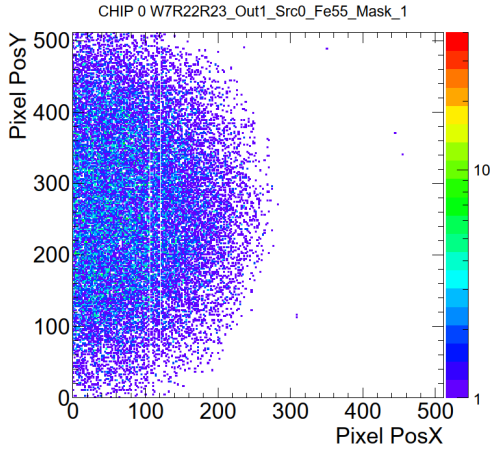


Chip-to-chip connections

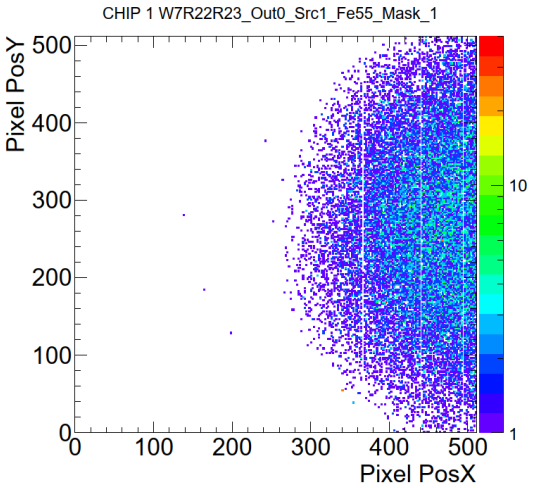
- Fe55 source test (threshold setting ~300 e^-), reading data from chip 0 via chip 1 and reverse

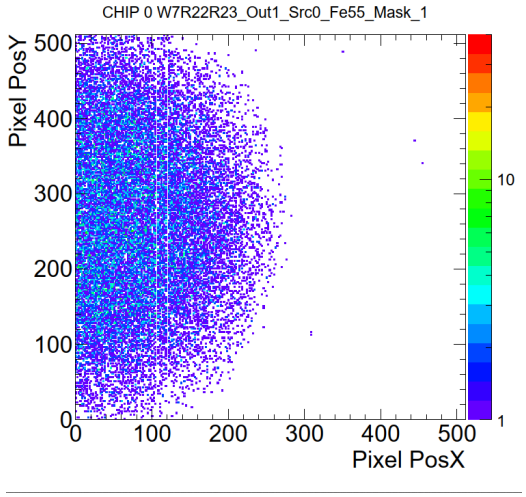
Chip0→Chip1→Out





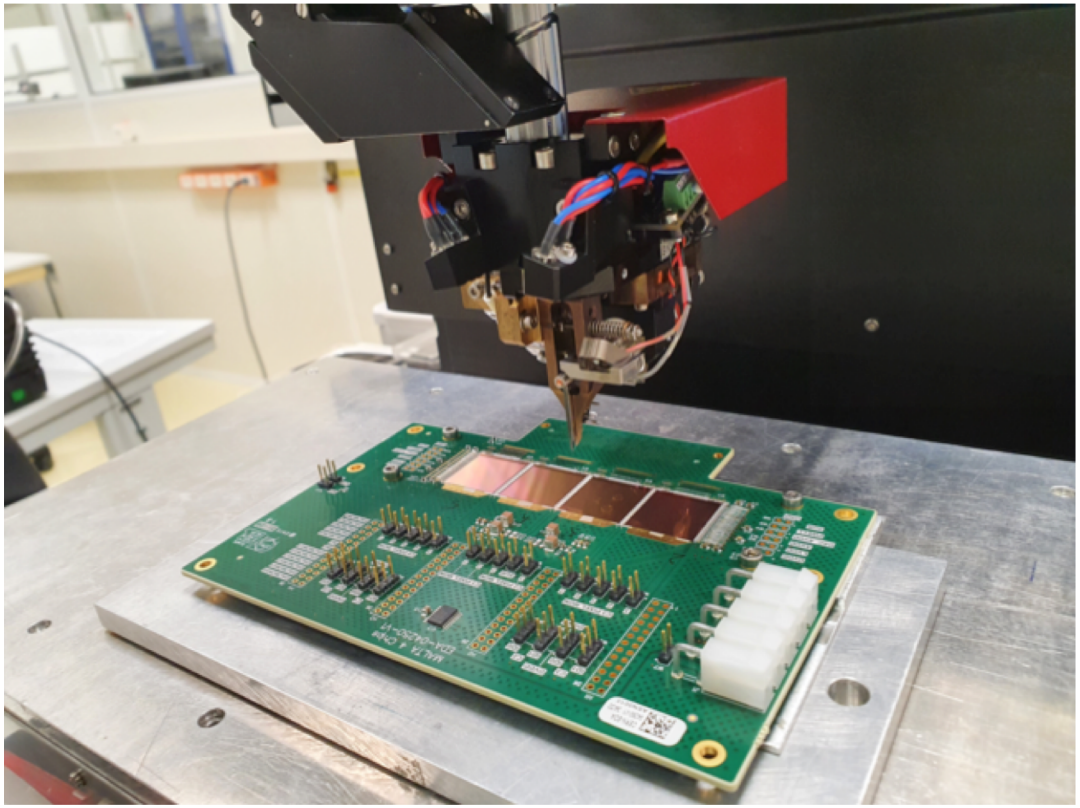
Chip1→Chip0→Out





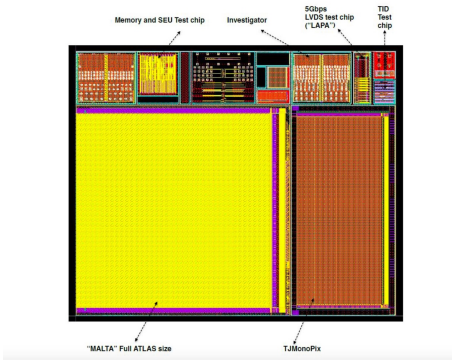
Multi-chip MALTA module

- Test of four MALTA chips mounted together on a test-card have started.
- Data and power connections between neighboring chips have been realized using Al wedge wire bonding.

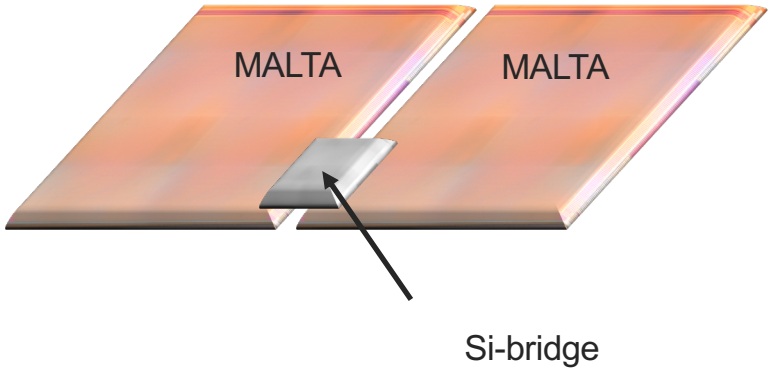


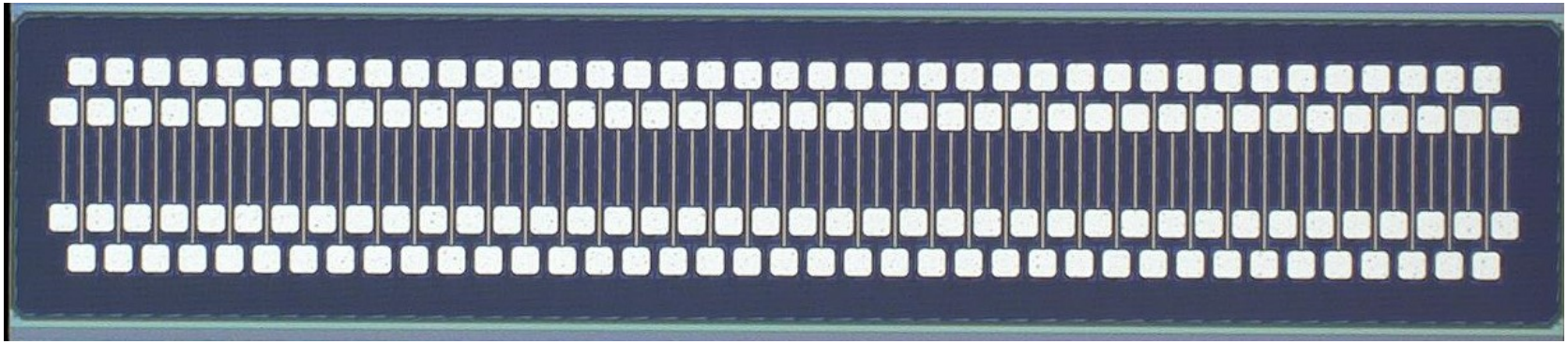
Chip-to-chip connections

- A **flip-chip interconnection structure (Si-bridge, ~ 1mm x 5 mm)** was designed and included in the STREAM reticle to **connect the CMOS transceivers and the power pads** at the edges of two MALTA sensors.



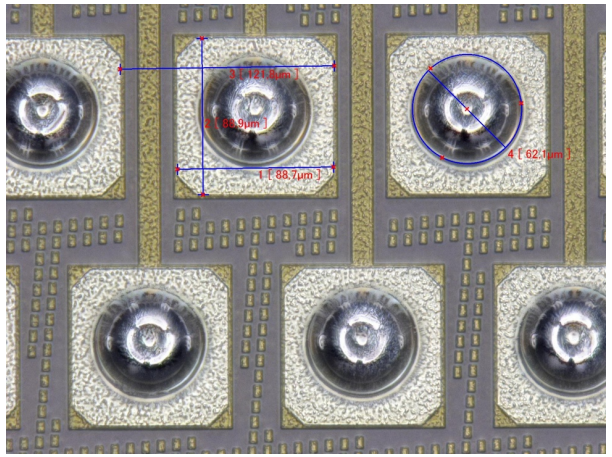
- The 40 connection pads are arranged in a staggered configuration to match the corresponding MALTA layout.

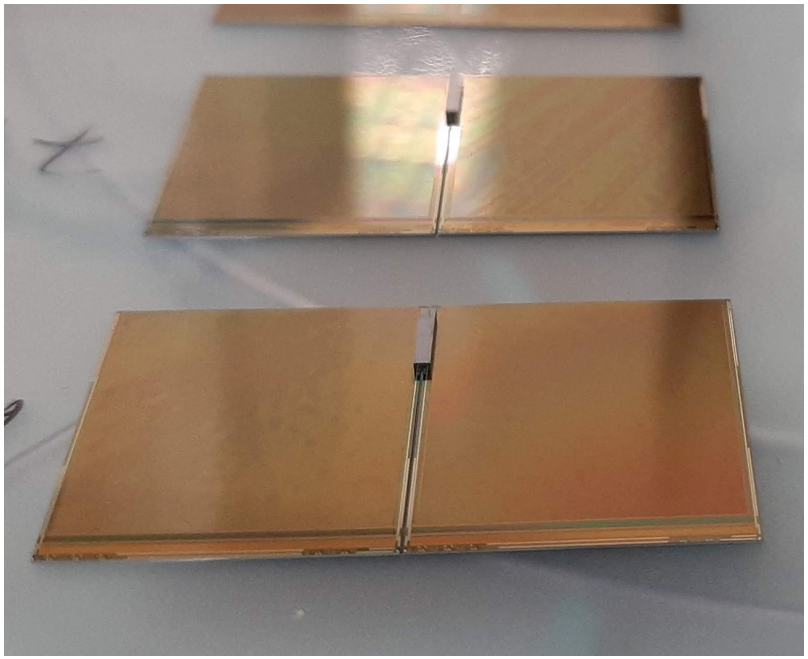


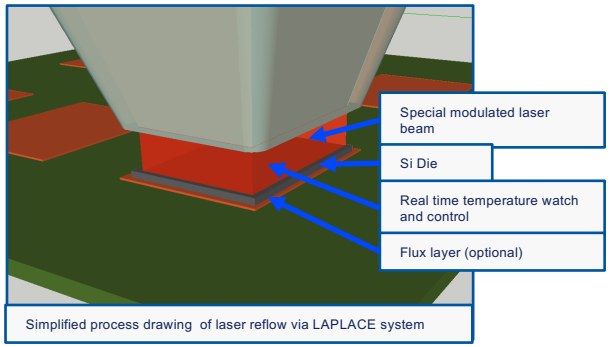


Chip-to-chip connections

- Cu-pillars with Sn/Ag solder caps (PacTech) on the Si-bridge pads (processing on 200 mm wafer): 60 µm diameter, 120 µm pitch
- E-less Ni/Au plating of the MALTA connection pads
- Connection between MALTA chips and Si-bridge carried out using the PacTech LaPlace flip-chip process (modulated laser beam, no flux)





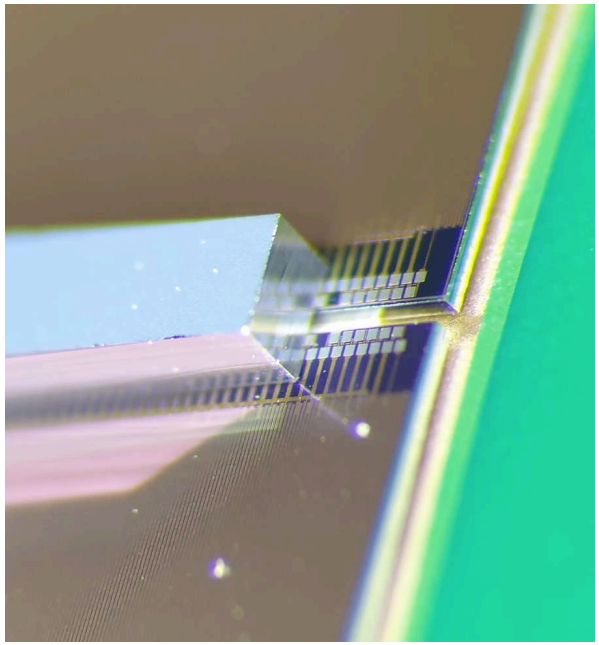


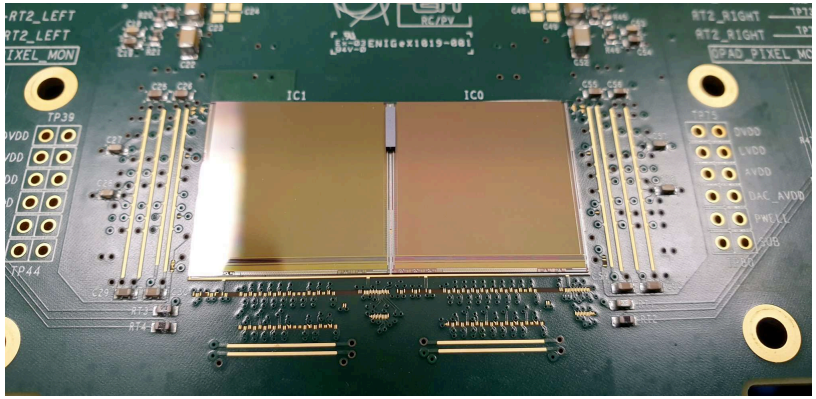
Simplified process drawing of laser reflow via LAPLACE system

Chip-to-chip connections

- First (non-functional) MALTA chips with Si-bridges have been mounted on test-PCBs and wire bonding tests were completed successfully.
- Assembly of functional MALTA sensors with Si-bridges is currently underway.
- In parallel studies using ACF (Anisotropic Conductive Film) to connect the Si-bridge with the MALTA sensors are in preparation.

see presentation by M. Vicente Barreto Pinto at this workshop





Summary and outlook

- MALTA is a monolithic pixel chip designed in a 180nm process by TowerJazz that provides the possibility for high speed data (and power) transmission from chip to chip.

- Functional tests using ultrasonic wire-bonding between two MALTA chips have been completed and further tests are now planned for chips connected with a Si-bridge structure.

- These studies are first stepping stones to building a large area and low-mass MALTA module. RDLs (redistribution layers) will be added in a next step to distribute the CLK and control signals that are still individual for each MALTA chip, while data and power are transferred from chip to chip.