3D INTEGRATION IN NANOELECTRONICS: BASIC TECHNOLOGIES AND APPLICATIONS TO IMAGE SENSORS

16th "Trento" workshop on Advanced Silicon Radiation Detectors, Dr. Christophe Wyon, February 17, 2021

OUTLINE

- The main technology drivers to move towards 3D Integration
- Basic 3D integration technologies
- 3D integration: applications to « image » sensors
- Takeaways

CEA-LETI AT A GLANCE

“3rd Innovative Public Research Organization Worldwide” 2012 -2020

Since **1967**

2,000 people

Patents:

- > 3,000 in portfolio
- 40**%** under license agreement

Startups:

- 69 created for 20 years (75% in activity)
- 3500 jobs created

Cleanrooms:

- 500 state-of-the-art equipment in 200 & 300 m²
- 10 000 square meters cleanroom

Budget:

- 315 M€
- 85% from R&D contracts

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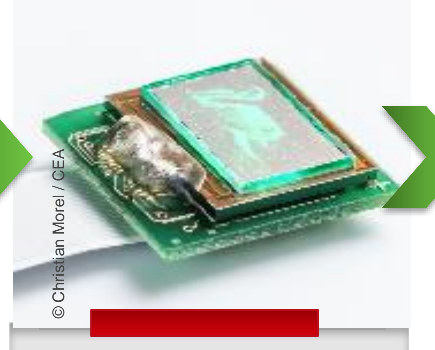
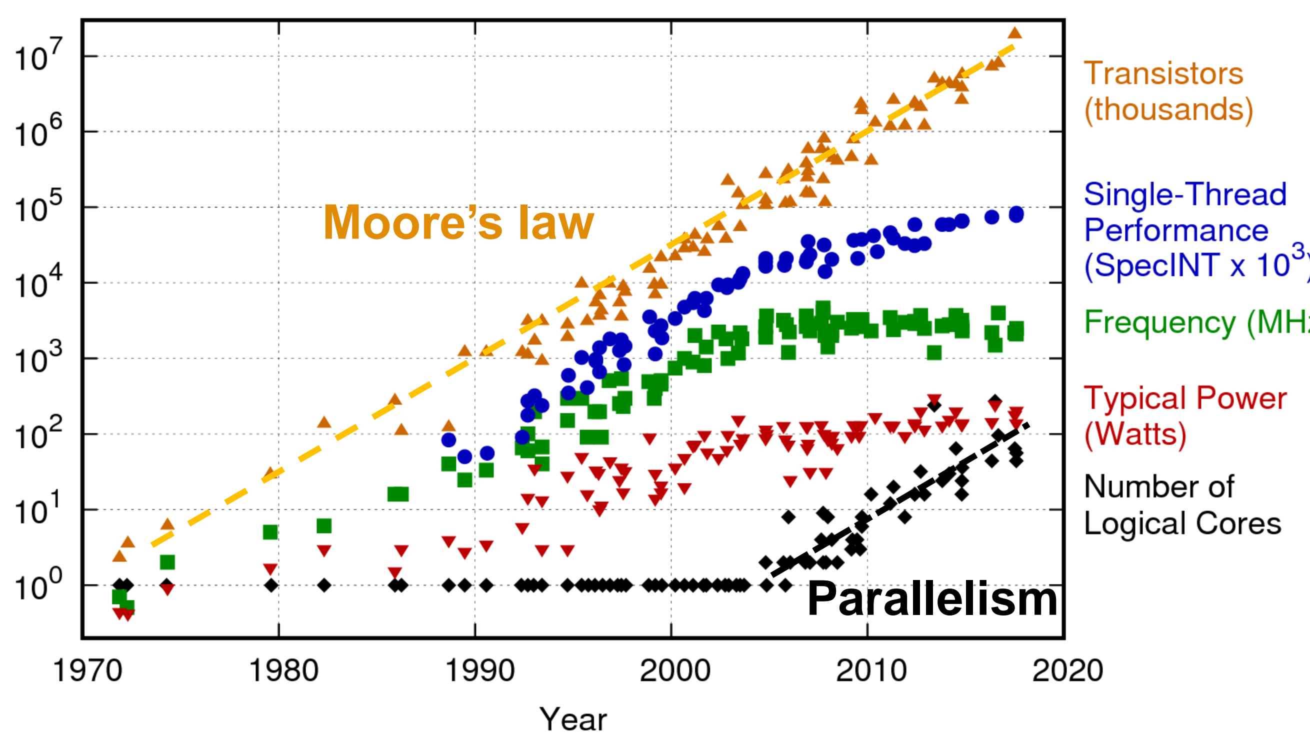
TECHNOLOGIES FUELING APPLICATIONS

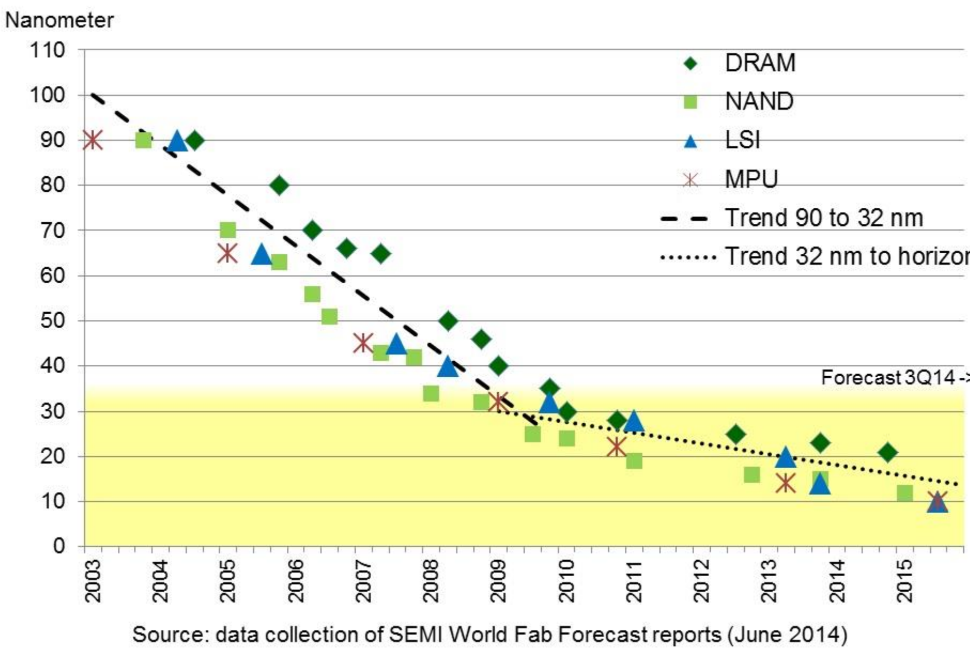
MATERIALS	FOUNDRY PROCESS	COMPONENTS DEVICES	FUNCTIONS ARCHITECTURES	ALGORITHM SOFTWARE	SERVICES PRODUCTS
					
SOI, SiC GaN, III-V, 2D materials …	Si Photonic, FDSOI CMOS, MEMS, NEMS, 3D sequential …	LED, T-MOS, RF Switch, NVM-RAM, TSV, PMUT…	RF Front-end, Sensors & actuators, Neural Network, Display, Cybersecurity …	Data fusion, tracking & classification algoritms, cybersecurity …	Localization, Lidar Autonomous Driving, Structural Health Monitoring

Mastering the entire value chain.
Gathering a complete ecosystem.

THE MAIN TECHNOLOGY DRIVERS TO MOVE TOWARDS 3D INTEGRATION

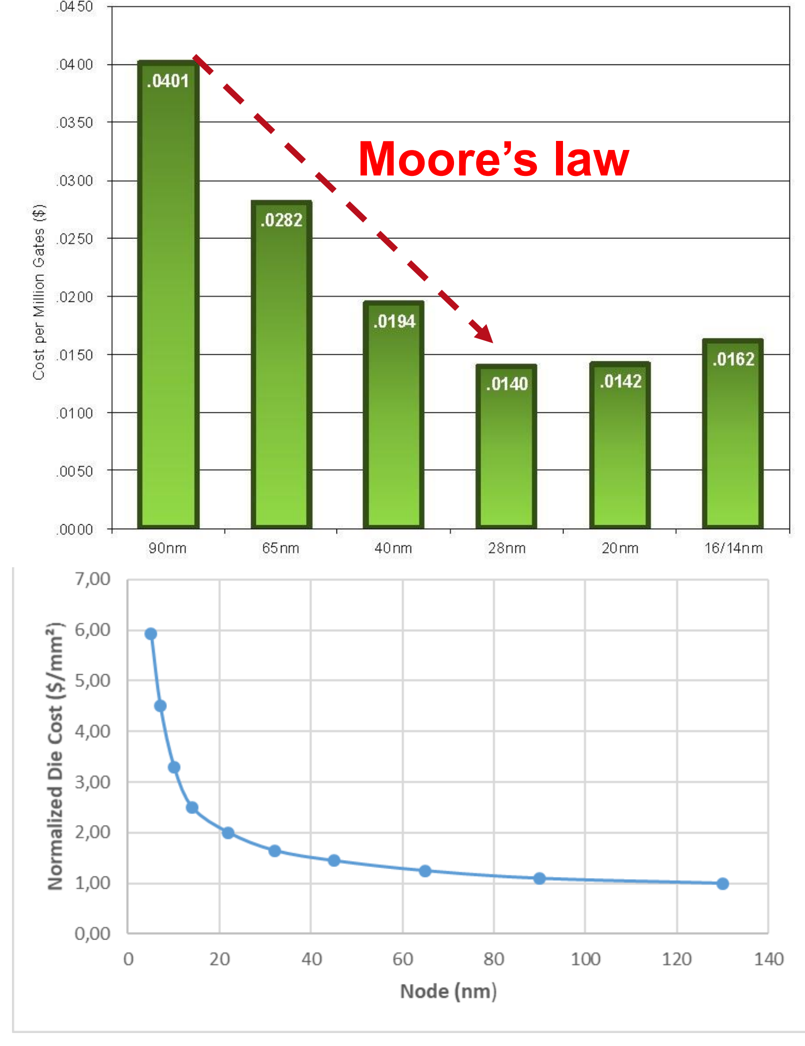
- ## Moore's law is slowing down

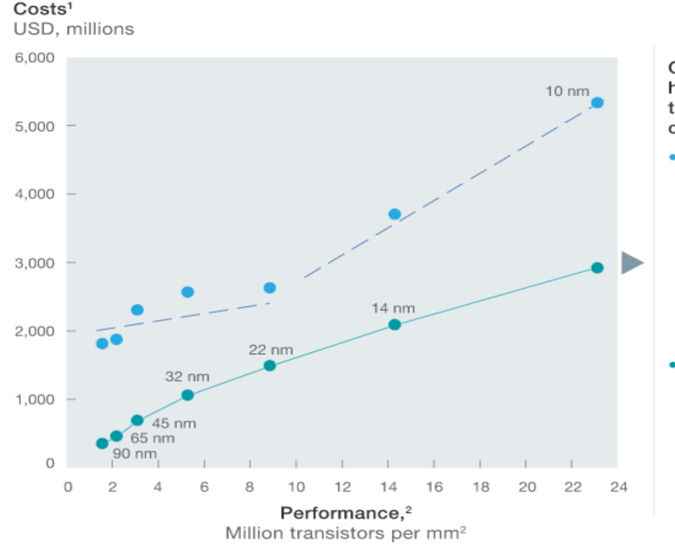


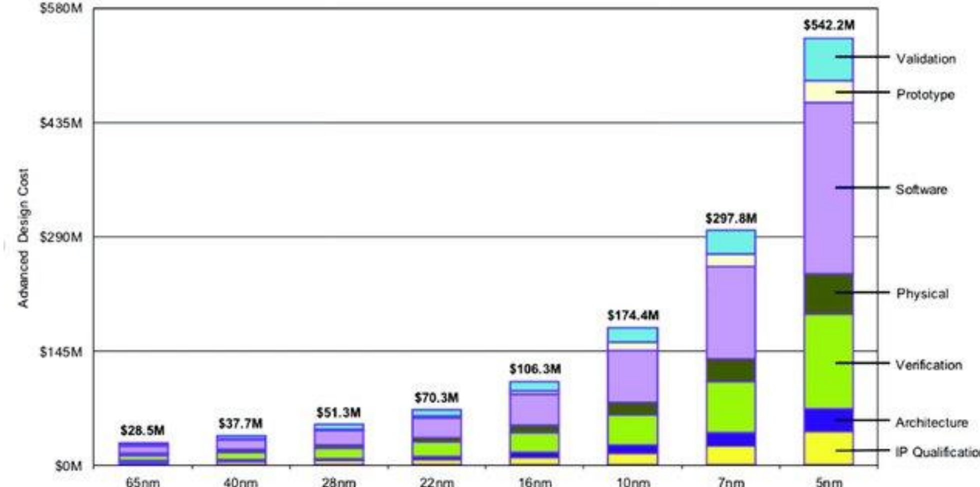


THE MAIN TECHNOLOGY DRIVERS TO MOVE TOWARDS 3D INTEGRATION

Moore's law is slowing down



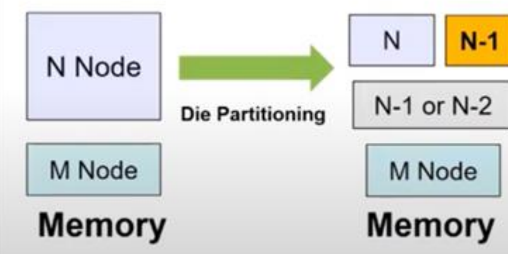


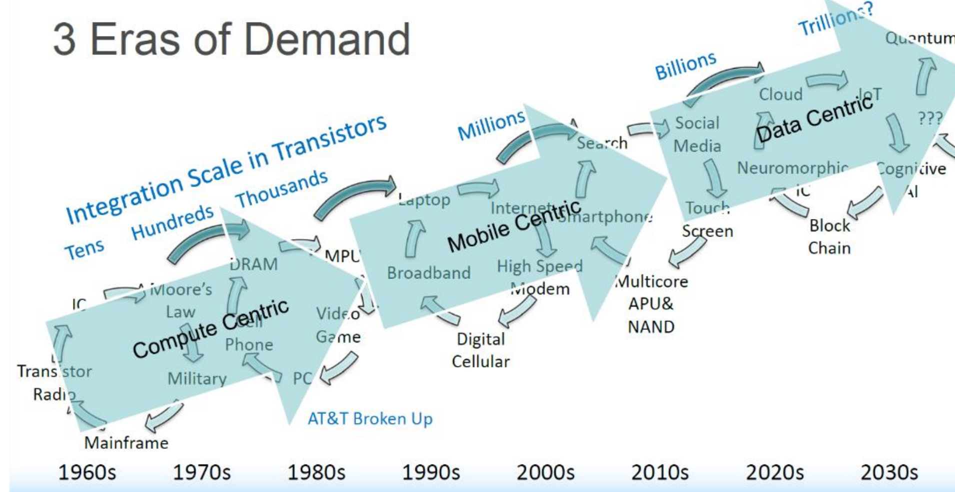


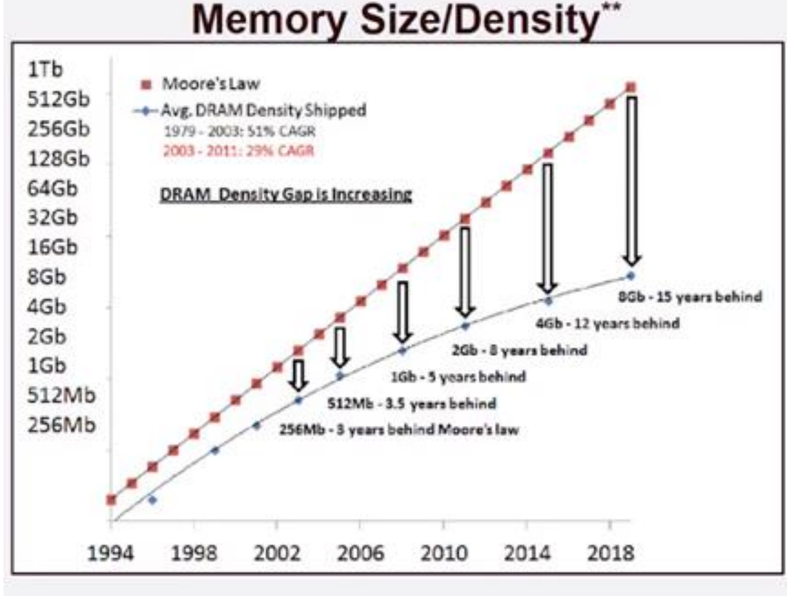
THE MAIN TECHNOLOGY DRIVERS TO MOVE TOWARDS 3D INTEGRATION

2 paradigm shifts

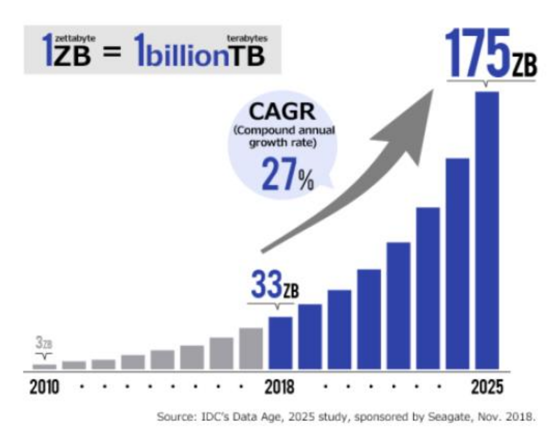
- **Move to a System Approach**
  - Silicon industry was technologically driven
  - Focus on function and usage => develop the suitable technologies accordingly
  - **SoC: System on Chip**
  - **SiP: System in Package**
  - Parameters:
    - Performance, footprint, form factor
    - Energy consumption
    - Cost







- **Move to a data centric paradigm**
  - Data is the fuel of our digital society
    - Deluge of data
  - Data storage is an issue
    - Risk of Si wafer shortage
  - Only 2% of stored data is used => AI



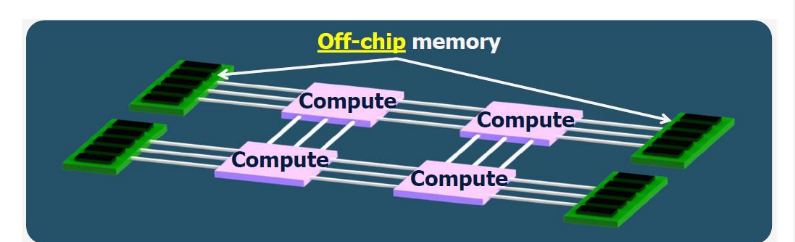
Ishimaru, 2019

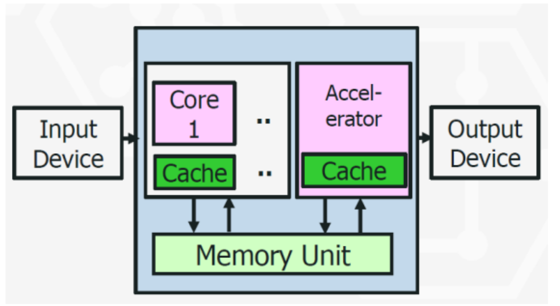
Clapp, 2015

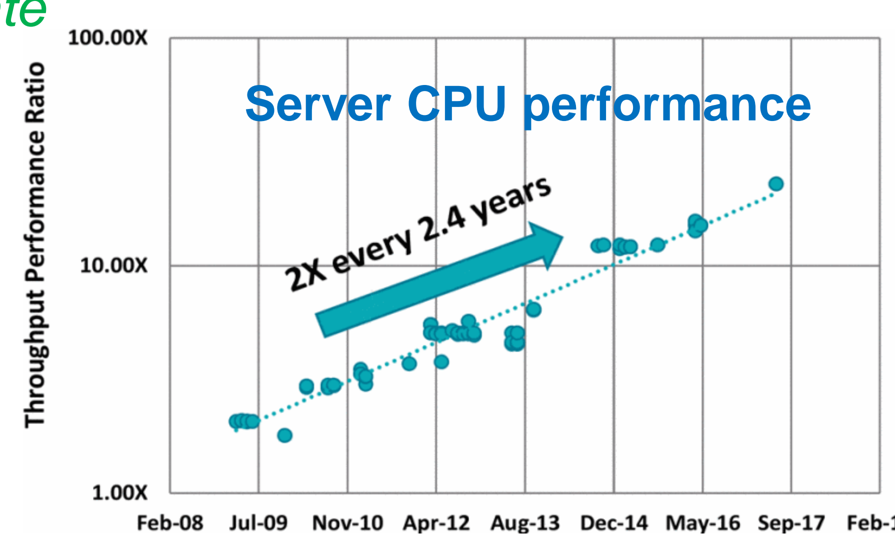
THE MAIN TECHNOLOGY DRIVERS TO MOVE TOWARDS 3D INTEGRATION

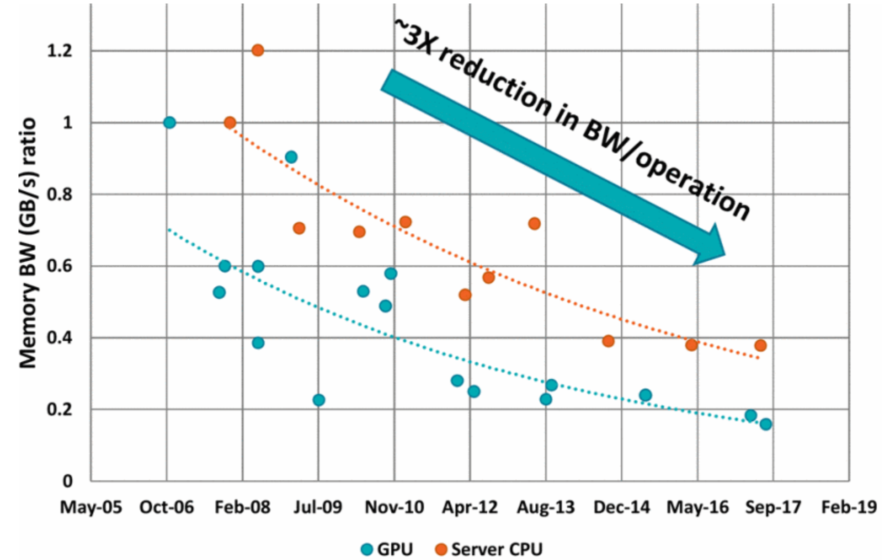
Performance and latency

- Logic devices: **Von Neumann architecture**
- Performance of CPU or GPU increases with generation nodes (Moore's law)
- *Perf= #cores*f_{core}*#operations/cycle*
- But not the memory bandwidth (BW) => **memory bottleneck**
- *BW= w_{bus}*f_{bus}*data rate*









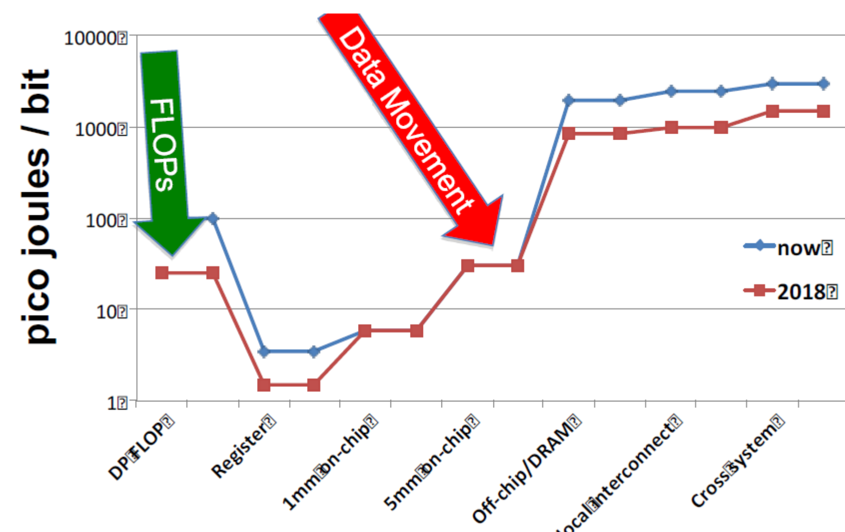
Memory bandwidth per operation in server CPU and GPUs

Source: Lisa Su – IEDM 2017

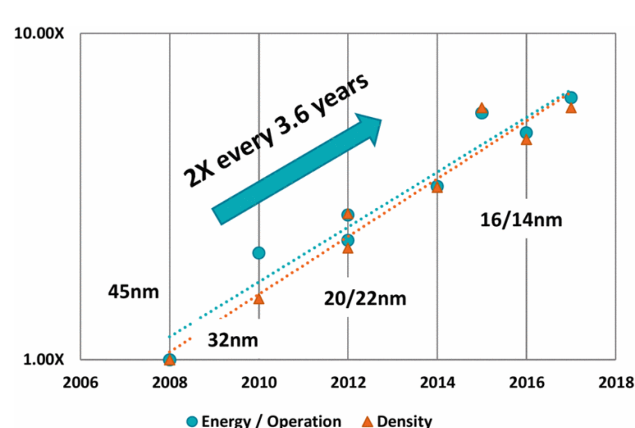
THE MAIN TECHNOLOGY DRIVERS TO MOVE TOWARDS 3D INTEGRATION

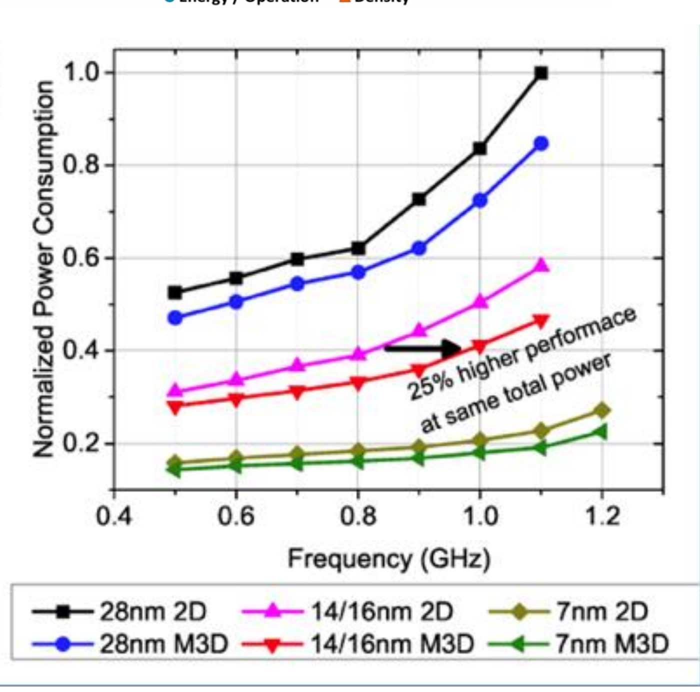
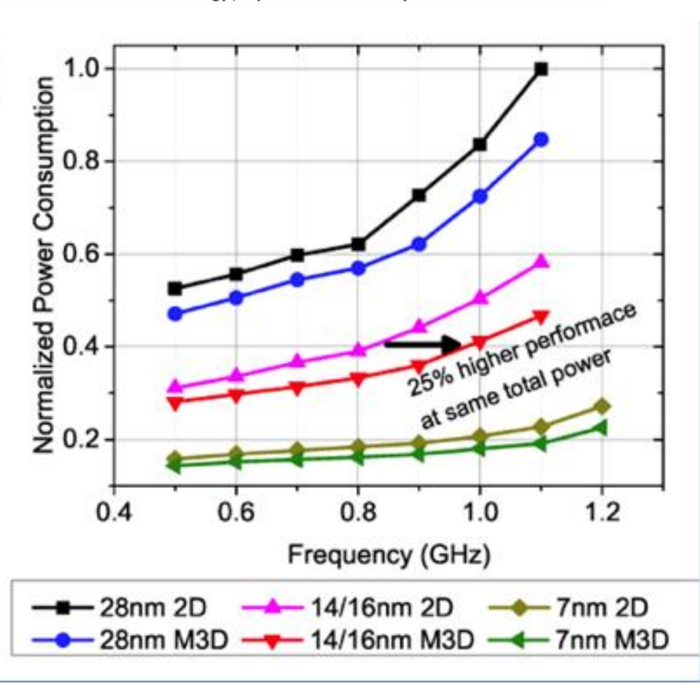
Power/Energy consumption

- Energy operation decreases with generations (Moore's law)
- **Data movement consumes a lot**
- Power for moving a bit in a conductor:
- *P= data rate*L/cross section(w)*
- **Shorten L and/or increase w**



Source: S. Horst, Optical Interconnect Conference, 2013



Sinha, 2020

Source: Lisa Su – IEDM 2017

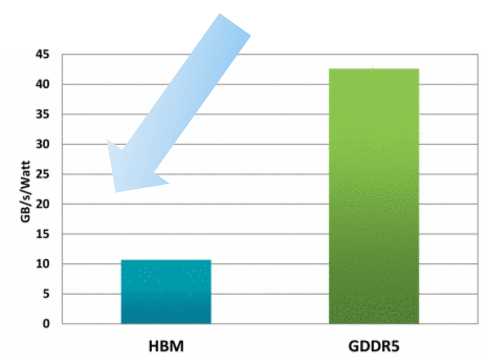
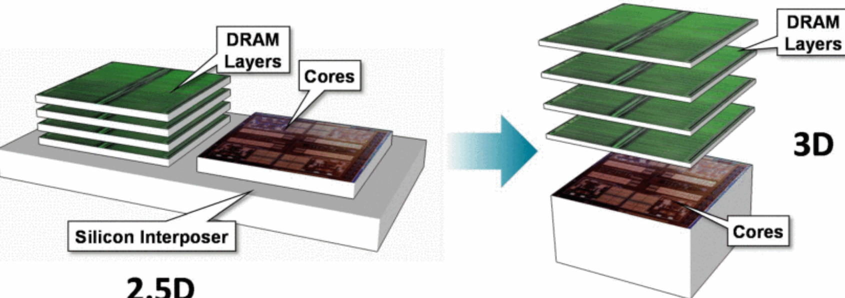


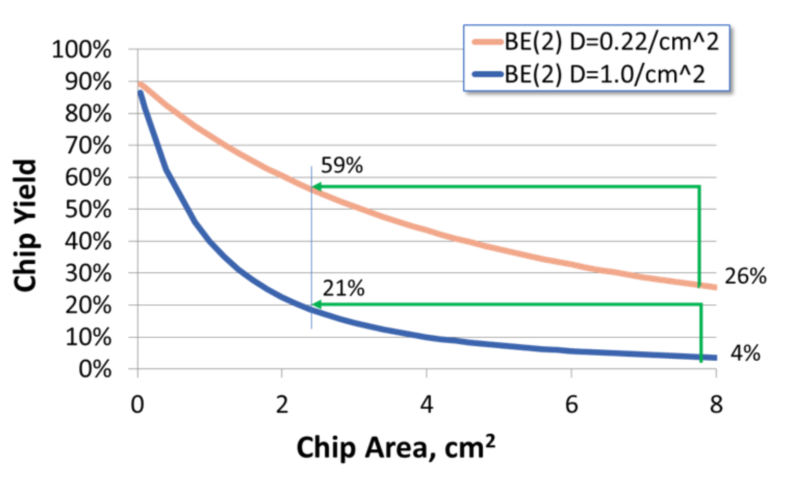
Fig 13. HBM 2.5D provides both higher bandwidth and lower power.

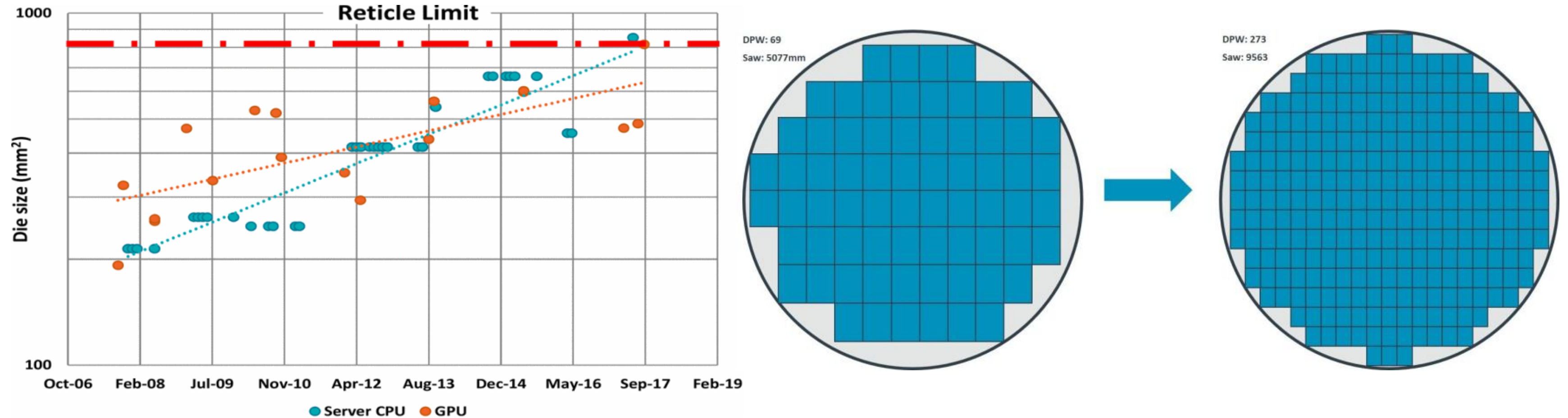


THE MAIN TECHNOLOGY DRIVERS TO MOVE TOWARDS 3D INTEGRATION

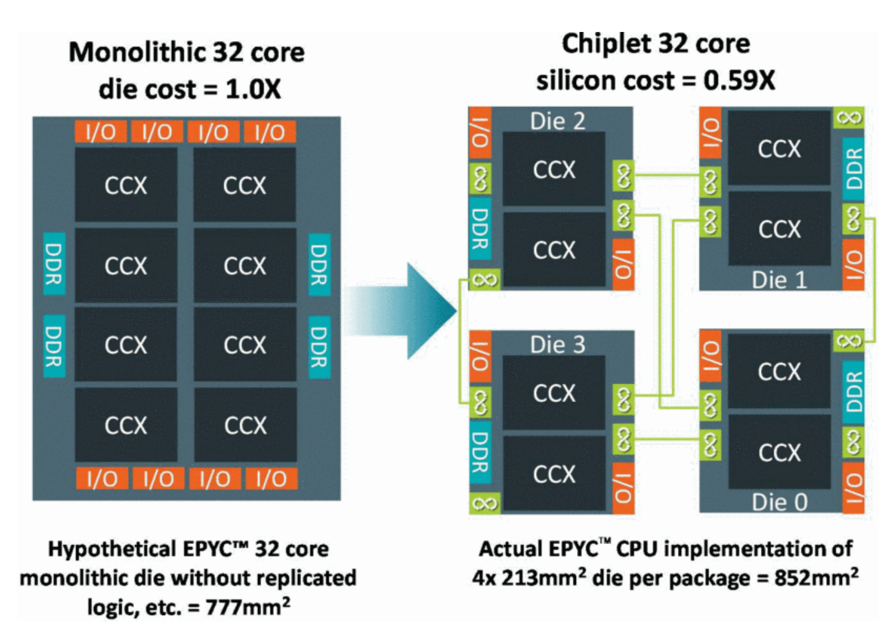
Cost savings

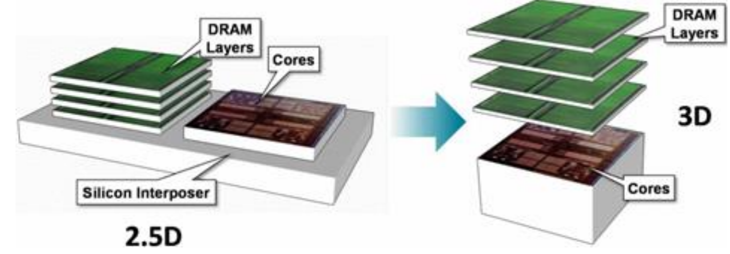
- **Wafer cost is key**
- **Chip cost increases with:**
  - The manufacturing node
  - The Si area
  - SoC requires huge Si area
- **But the chip yield decreases with the Si area**





Source: Lisa Su – IEDM 2017



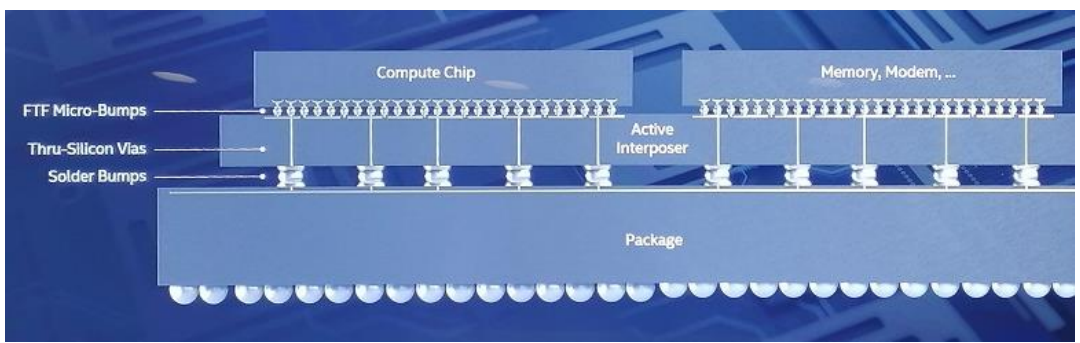


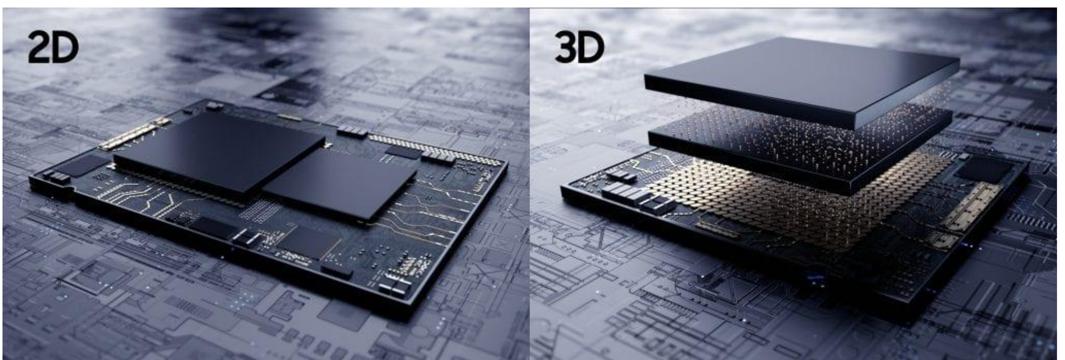
ARM: 5nm, 500mm² => 32%
GF: 625mm² => 63%

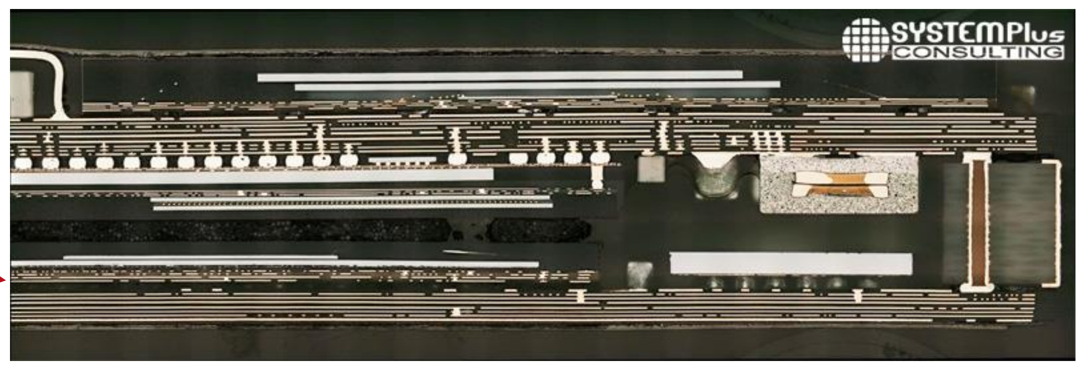
THE MAIN TECHNOLOGY DRIVERS TO MOVE TOWARDS 3D INTEGRATION

New market strategy

- SoC was the Si industry behemoth
- Chip assembly, packaging and test usually outsourced (OSAT)
  - Human resources => Asia
- **Introduction of wafer-level packaging**
  - IP and EDA became available
  - ADK developed by foundries
  - Automated assembly tools were (are) developed
- Adding functionality to FEOL process
  - At the wafer level
- **Intel, Samsung and TSMC entered in the 3D game**
  - W2W, D2W, Chiplet…







OUTLINE

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- **Basic 3D integration technologies**
- 3D integration: applications to « image » sensors
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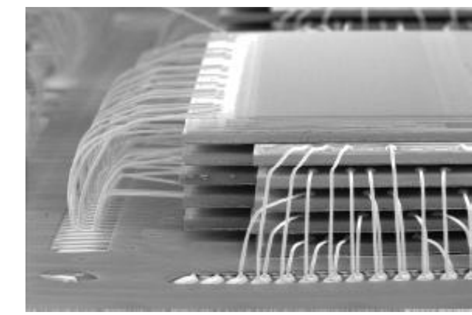
BASIC 3D INTEGRATION TECHNOLOGIES



ST

- **2.5 and 3D interposer based integration**
  - Dies are placed/stacked side by side on top a passive Si interposer based on TSV
  - Through Si via (TSV)
    - Organic, glass…
- **3D Wafer level packaging**
  - Wafer to wafer
  - Die/chip to wafer
- **3D stacked ICs**
  - Hybrid bonding
- **Chiplets**
  - With an active interposer
- **Monolithic 3D-IC**

2.5D: Side-by-side die stacked on a passive interposer that includes TSVs

2.5 or 3D: Interposer with top and bottom connection

3D + Interposer: Mix of side-by-side and stacked implementations on an interposer

3D Memory on Logic: One or more DRAM die stacked directly on logic die

Connections / mm^2 (1, 10^2, 10^4, 10^6, 10^8) vs Connection Pitch (µm) (1000, 100, 10, 1, 0.1); Design Complexity (a.u.)

3D microarchitectures
3D partitioned IP
Chiplets
Advanced Packaging
Wafer/Die Stacking
Monolithic 3D
Wafer-to-wafer bond
Die-to-wafer bond
uPillar
C4
Solder ball

System in Package (SiP) — 1998
RF Module — 2004
2.5D-IC (Silicon Interposer) — 2010
Ultra-High-Density RDL/FOWLP — 2016
Bump-Less 3D-IC — 2018
Heterogeneous Integration (Disaggregated SoC) Photonics — Now
Monolithic 3D-IC — Future

BASIC 3D INTEGRATION TECHNOLOGIES

3D/2.5D PACKAGING MARKET DRIVERS

TIMELINE — ≤2019 — 2020* — 2021 — 2022 — 2023 — 2024 — 2025

I/O DENSITY

YOLE Développement

TYPES OF TECHNOLOGIES
- Hybrid bonding
- Embedded Si bridge
- TSV, micro-bumps
- 2.5D interposers
- UHD FO

YMTC Periphery + Array
X-Stacking

Intel HBM+GPU
Kaby Lake-G

Intel FPGA
Stratix 10

Intel FPGA + Chiplets
Agilex

HPC (x)PU in Servers
TSMC & Intel – 3D SoC

NVidia GPU Interposer HBM2E
A100

Samsung HBM
Flarebolt

Stacked DRAM
3DS

Google (x)PU
TPU V3

Samsung HBM2E
Flashbolt

Intel CPU + Active Interposer
Intel Lakefield Foveros Core i5-L16G7

Intel Exascale GPU - HPC
Ponte Vecchio: Co-EMIB

Xilinx FPGA
Virtex Ultrascale

AMD GPU
Vega Frontier

NVidia GPU
Pascal 100

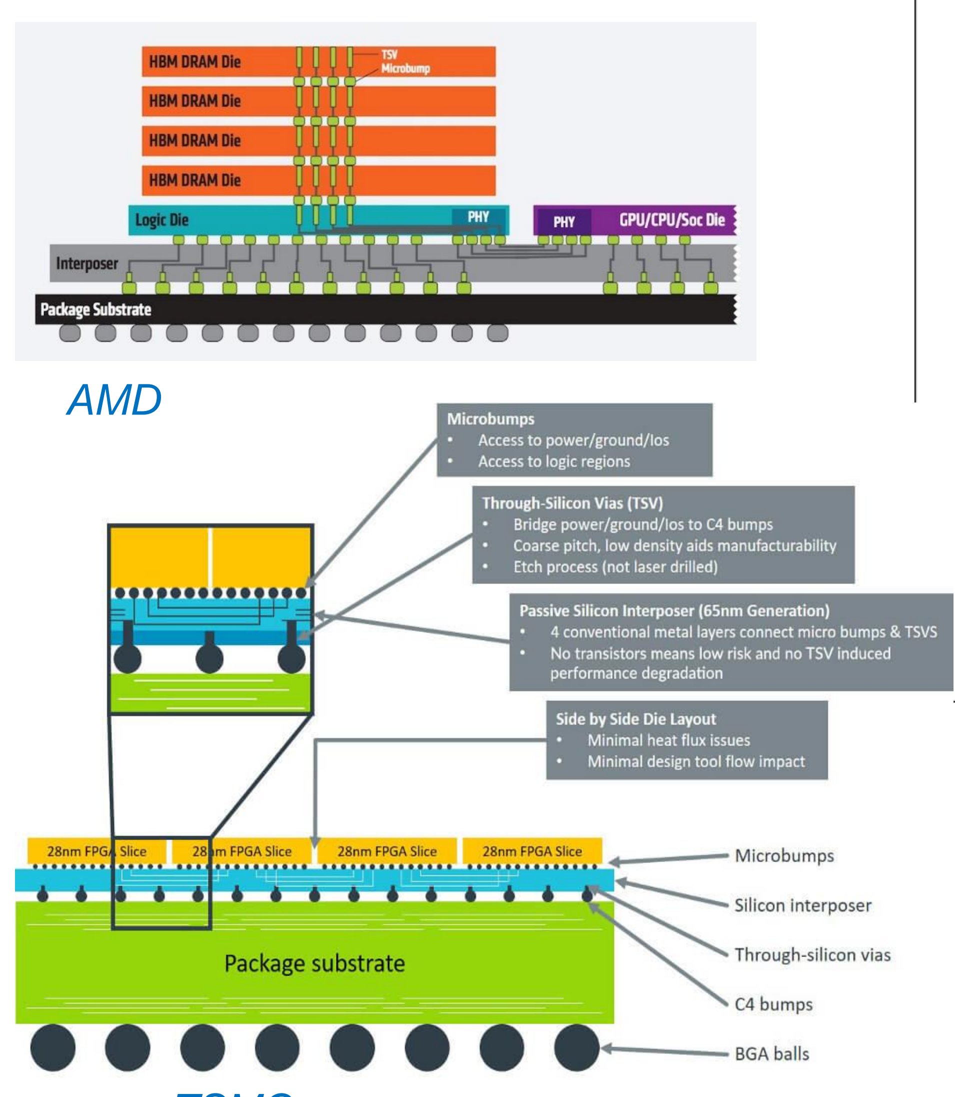
Broadcom (x)PU + HBM
Jericho2

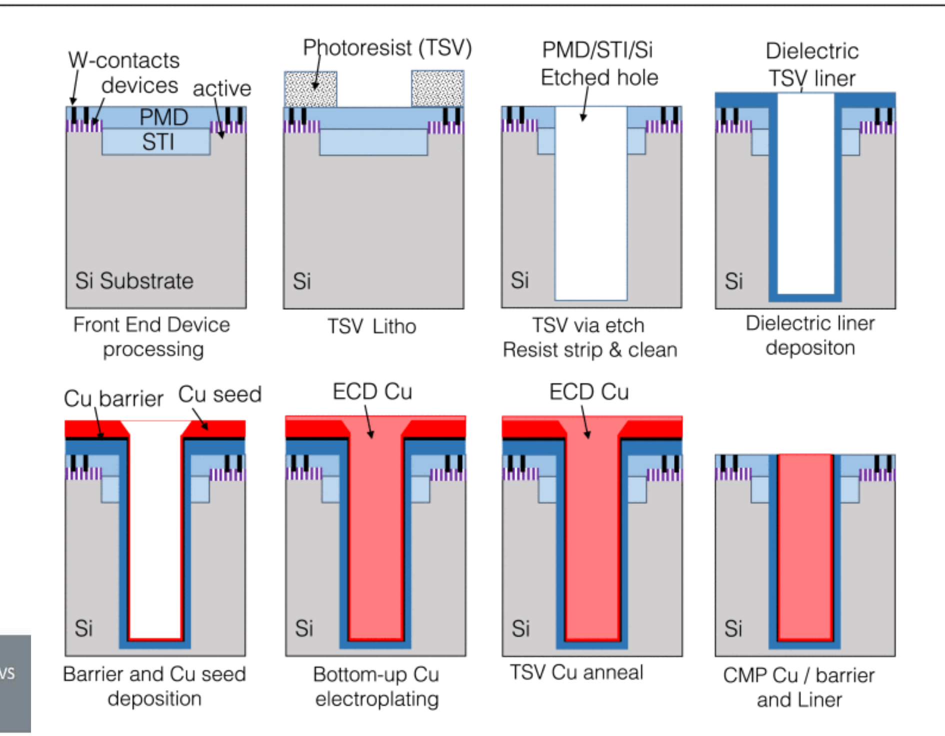
Intel (x)PU Ethernet Switch
Tofino2

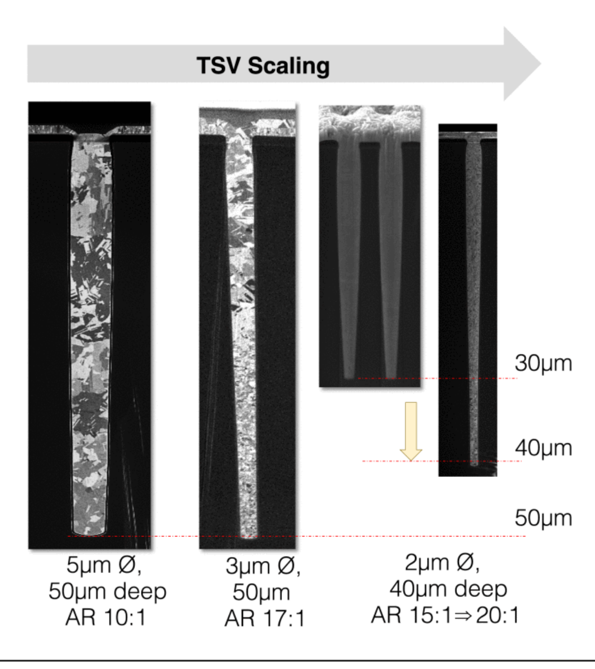
HPCs potentially for Tesla and Cerebras
TSMC inFO_SoW

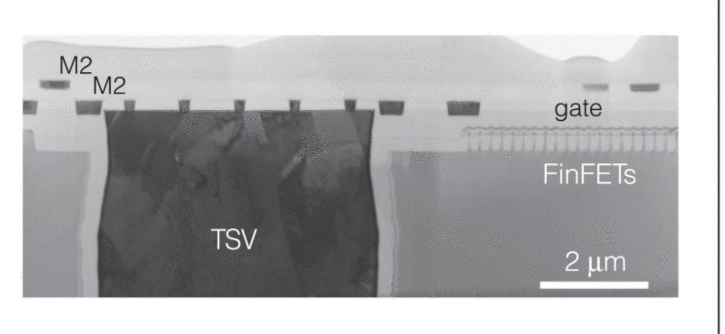
HiSilicon CPU (Storage)
Hi1610 (Now known as Kunpeng)

BASIC 3D INTEGRATION TECHNOLOGIES: PASSIVE INTERPOSER AND TSV









E. Beyne, IEEE Design, 2016

BASIC 3D INTEGRATION TECHNOLOGIES: 3D SIC OR SOIC

Micron

Barrier layer
Si
Cu
Dielectric layer

Stack of 16 DRAM

Ratio	μbump	SoIC
BW	1	1.2 (20%)
Energy/bit	1	0.85 (15%)

Heat spreader
Thermal paste
Silicon
tier n
Microchannels
TSVs
underfill & microbumps
microchannel cover
ILD & metal layers
underfill & C4 bumps
tier 2
tier 1
Package substrate
BGA balls
PCB

Zajac, 2019

C4 Solder 150 µm 50 I/O
Cu Pillar 150 µm 100 I/O
Cu µPillar 50 µm 400 I/O
Cu µPillar 30 µm 1,000 I/O
Cu µPillar 20 µm 2,500 I/O
Cu µPillar 10 µm 10,000 I/O

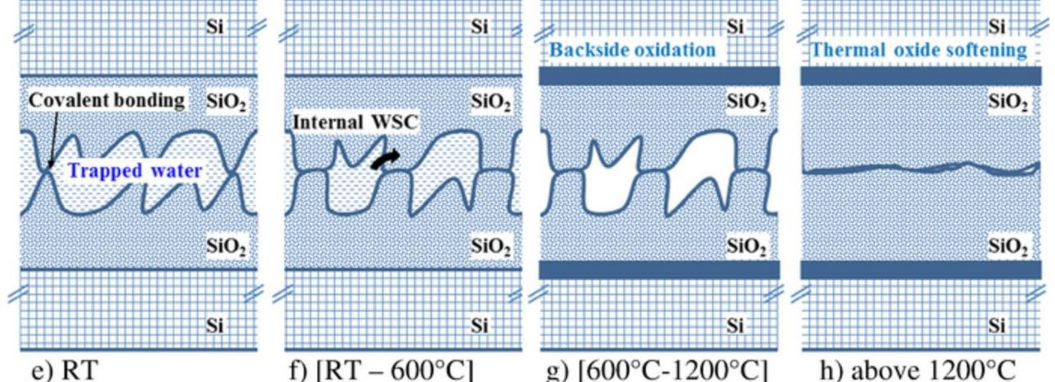
C4 (Flip-Chip) ~120/mm²
→ µ-bump (3DIC) ~ 800/mm²
→ Bump-less (SoIC) 12,000 → 1,200,000/mm²

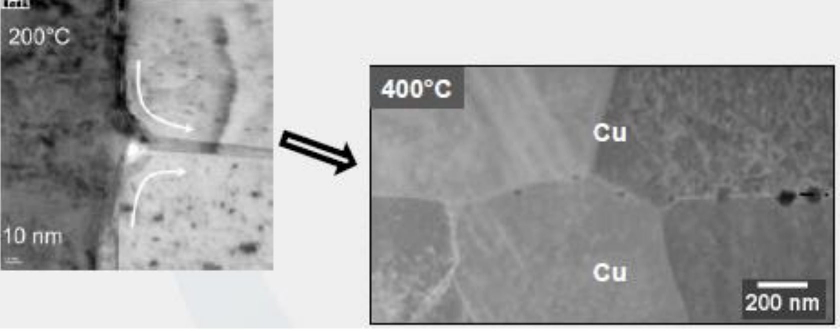
TSMC

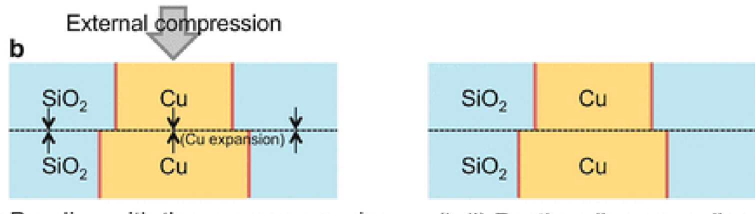
BASIC 3D INTEGRATION TECHNOLOGIES: (HYBRID) BONDING

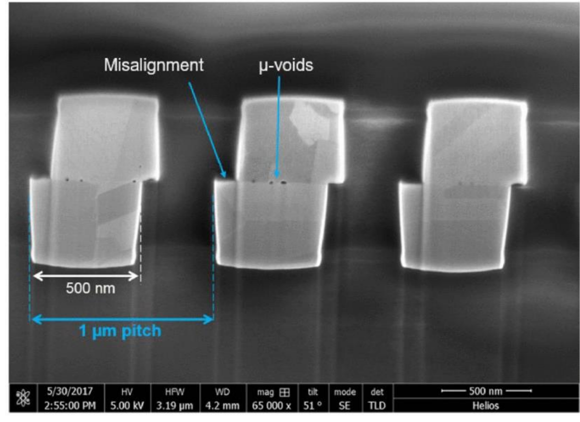
- **SiO_2-SiO_2 bonding: the most efficient**
  - Si-Si bonding not useful for 3D integration
- **Metal-Metal bonding**
  - Cu-Cu is widely used
- **Hybrid Cu-SiO_2 bonding**
  - Used for W2W and D2W bonding

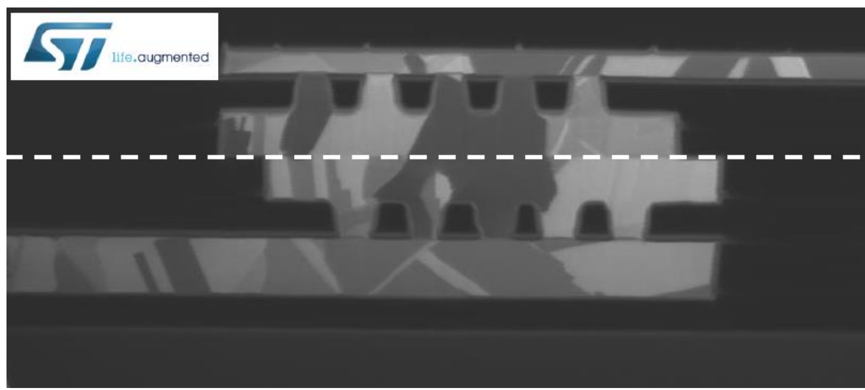
Fournel, 2015



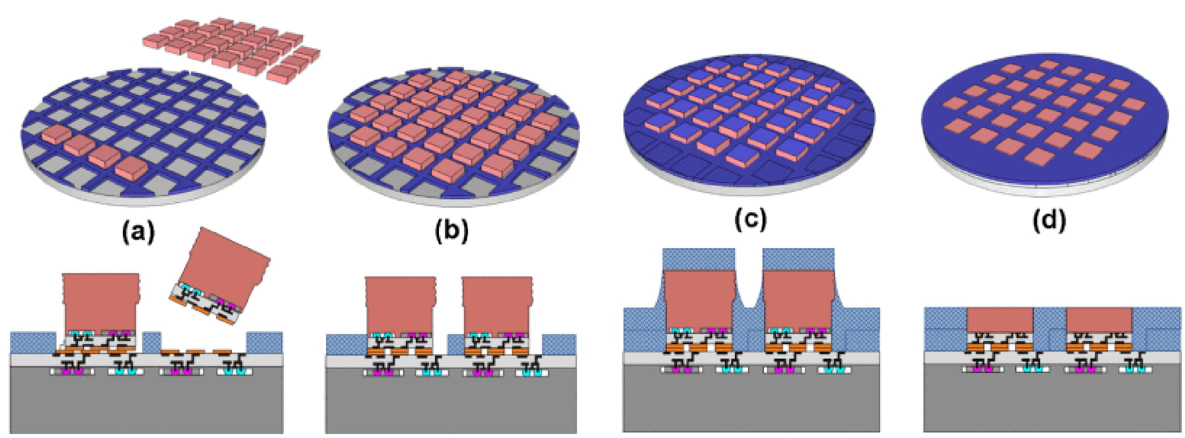


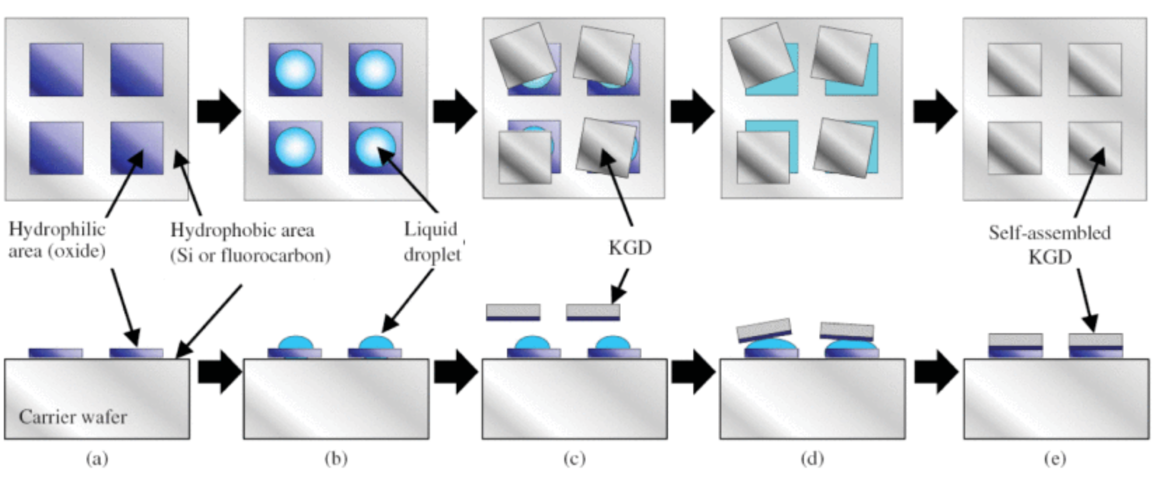


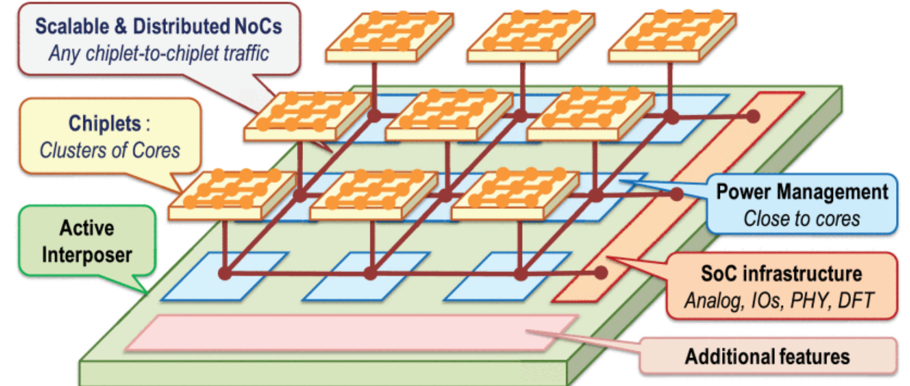


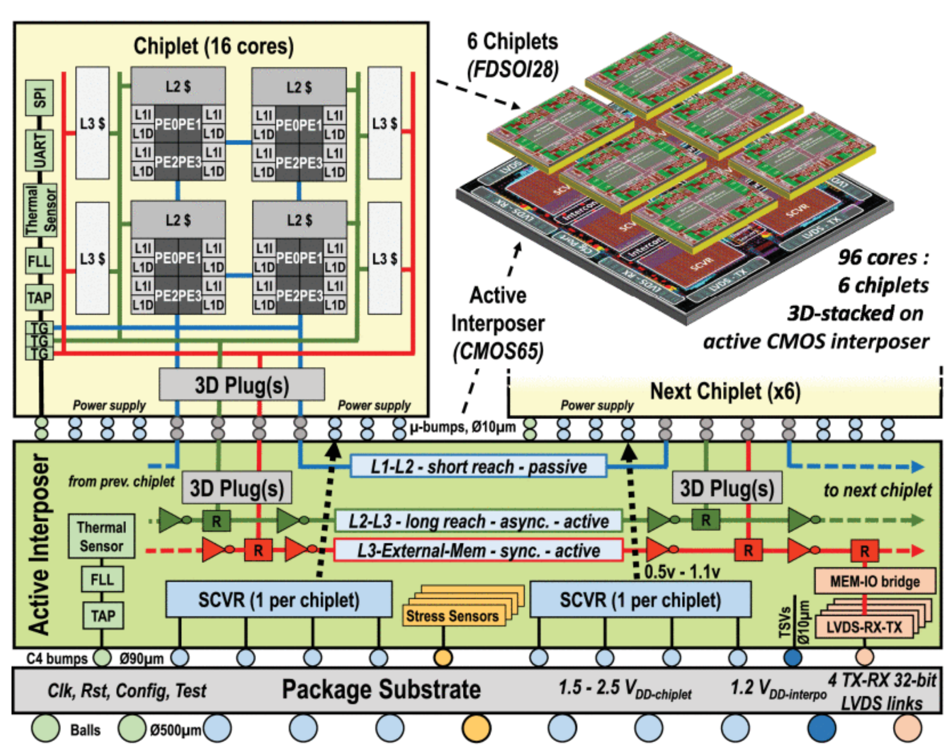


BASIC 3D INTEGRATION TECHNOLOGIES: D2W AND CHIPLET APPROACHES



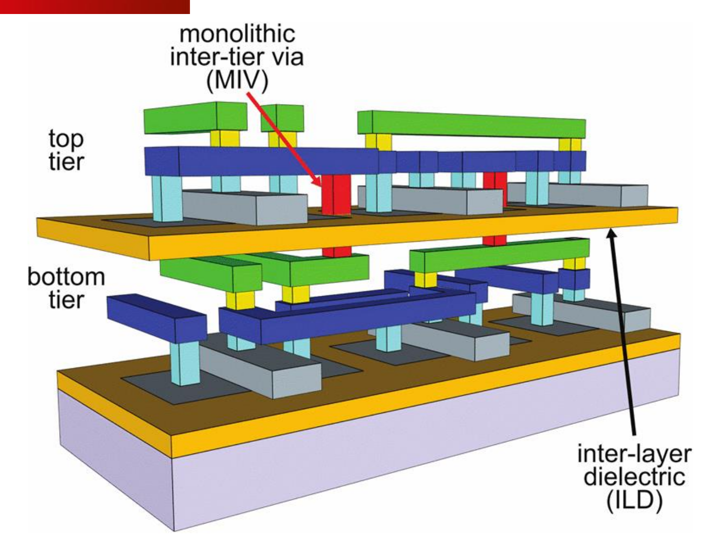


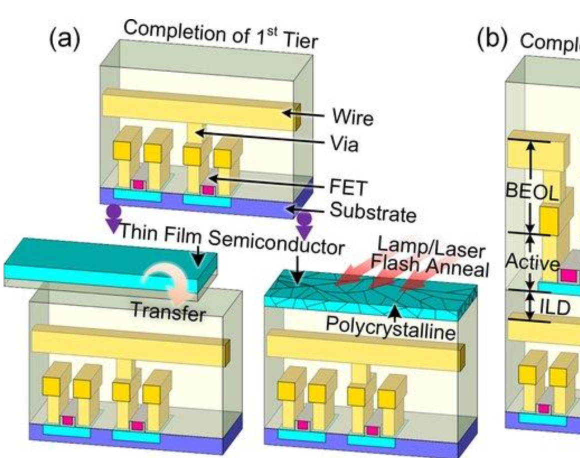


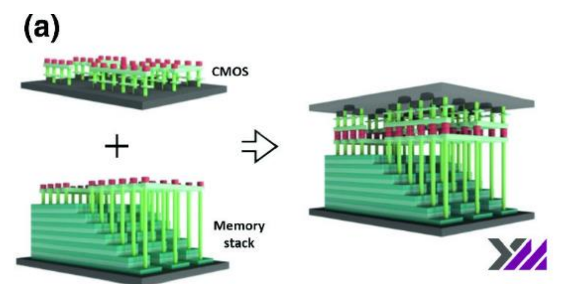


Vivet, 2021

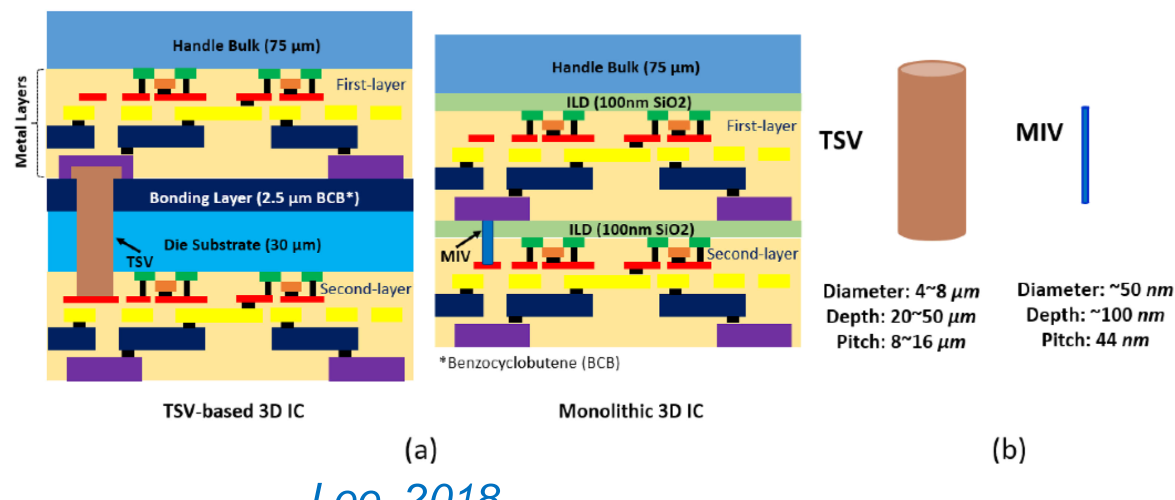
BASIC 3D INTEGRATION TECHNOLOGIES: MONOLITHIC INTEGRATION



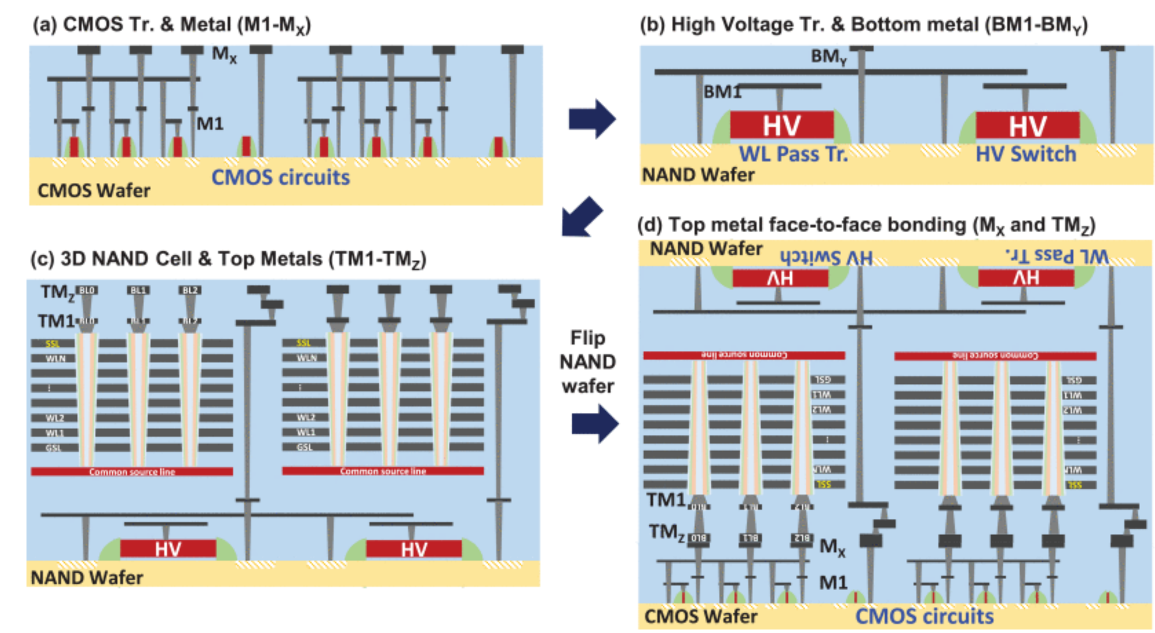




3D-NAND – 128/176 stacked layers



Lee, 2018



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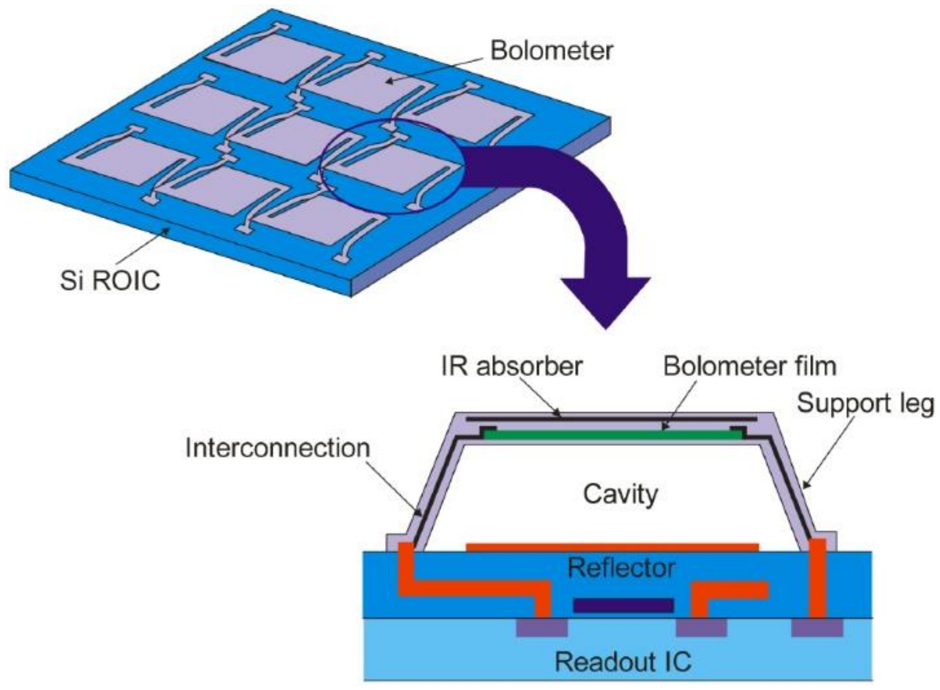
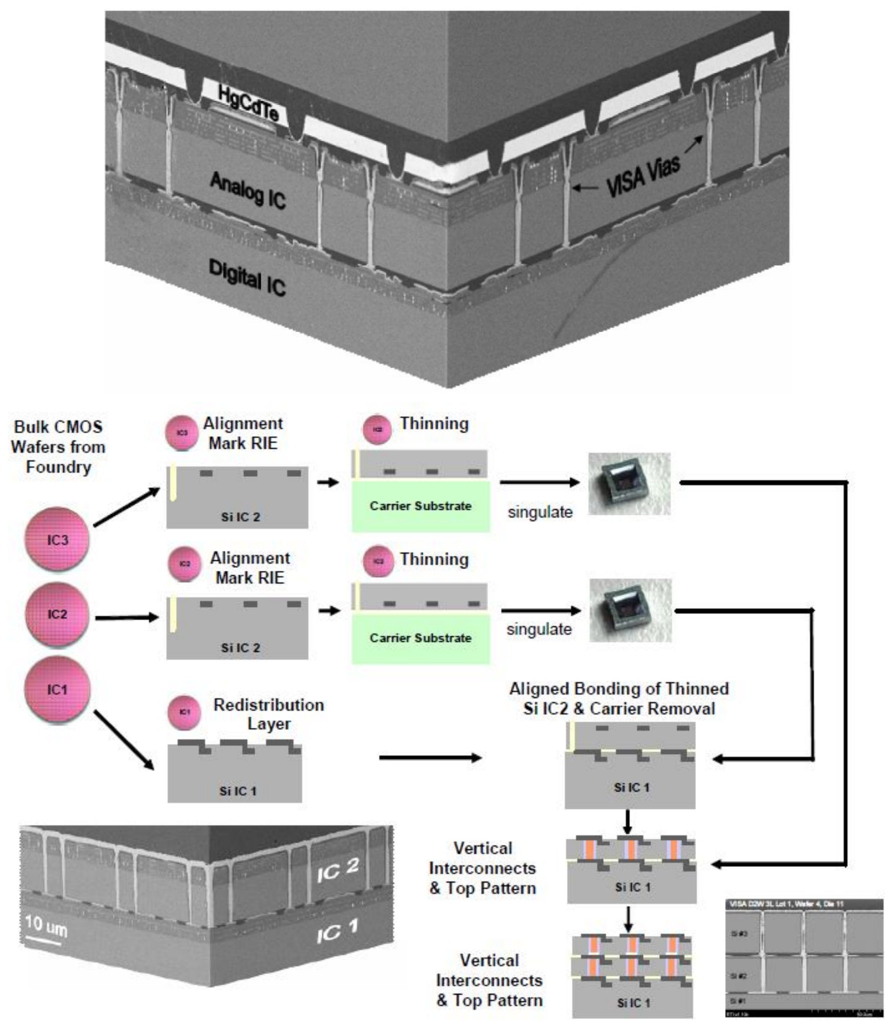
3D INTEGRATION: IR SENSORS

Uncooled IR sensor: micro-bolometer



Rogalski, 2016

Cooled IR FPA



Temple, 2006

3D INTEGRATION: CMOS IMAGE SENSORS – HYBRID BONDING

On chip color filter and micro lens
Si (CIS)
Insulator (CIS)
Insulator (Logic)
Si (Logic)

Top part
(BI-CIS process
technology)

Bottom part
(Logic process
Technology)

Sukegawa, 2013

Top part
(BI-CIS process
technology)

Middle part
(DRAM process
technology)

Bottom part
(Logic process
technology)

On chip color filter and micro lens
Photo Diode
Storage Node
5um

Haruta, 2017

Pixel
Peripheral

Pixel
DRAM
Logic
Interface between
Pixel and DRAM
Interface between
DRAM and Logic
Si
BEOL
TSV wiring
Si
Memory Cell
BEOL
BEOL
Si
TSV
(Pixel-DRAM)
TSV
(DRAM-Logic)
10μm

Kagawa, 2019

3D INTEGRATION: CMOS IMAGE SENSORS

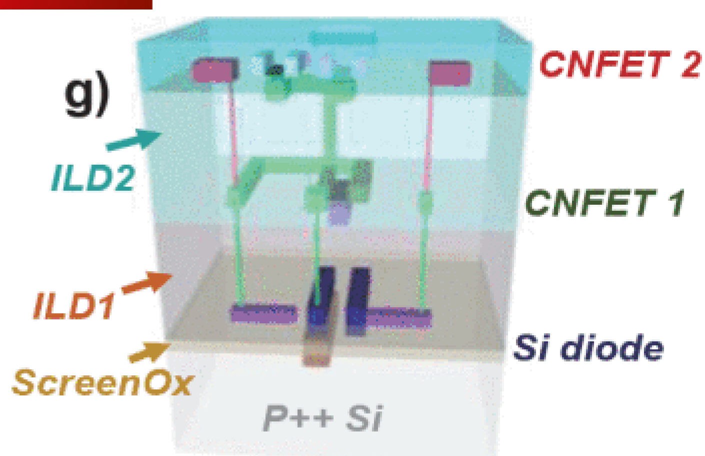
Flagship Smartphone, Primary Cameras

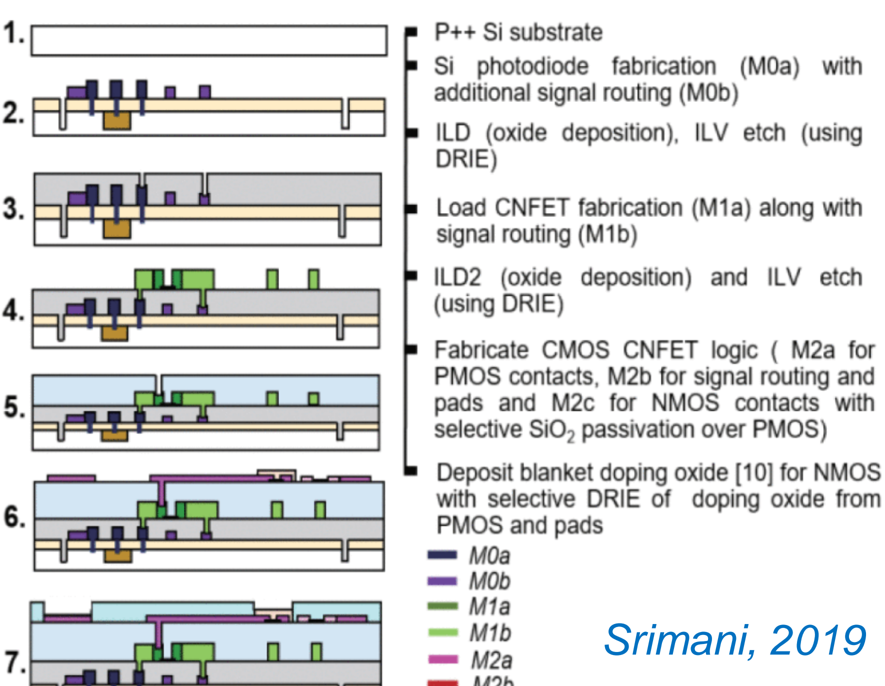
	iPhone XS	HUAWEI P30	SAMSUNG Galaxy S10
CIS	5.79 mm x 7.01 mm (40.6 mm²)	6.23 mm x 8.47 mm (52.3 mm²)	5.88 mm x 7.68 mm (45.2 mm²)
Interconnect	SONY – Hybrid Bonding Interconnect (6.0 µm pitch)	Hybrid Bonding Interconnect (6.0 µm pitch)	SAMSUNG – TSV Interconnect (5.0 µm pitch)
ISP	40 nm gen.	40 nm gen.	28 nm gen.
DRAM			Flip-chip + TSV Interconnect; 3.17 mm x 5.33 mm (16.9 mm²), 20 nm gen.

- Hybrid bonding array = TSV array replacement

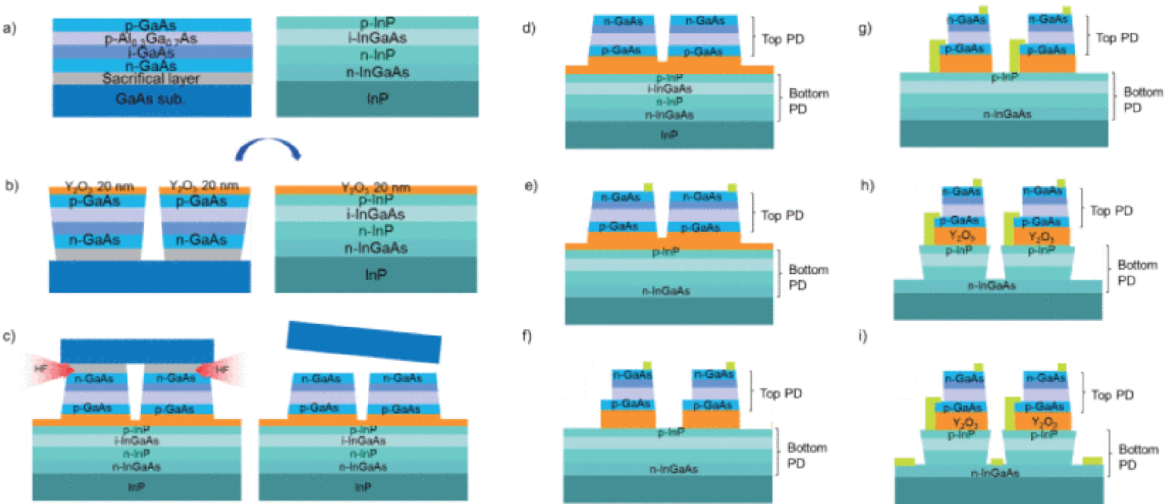
TechInsights

3D INTEGRATION: CMOS IMAGE SENSORS – MONOLITHIC INTEGRATION



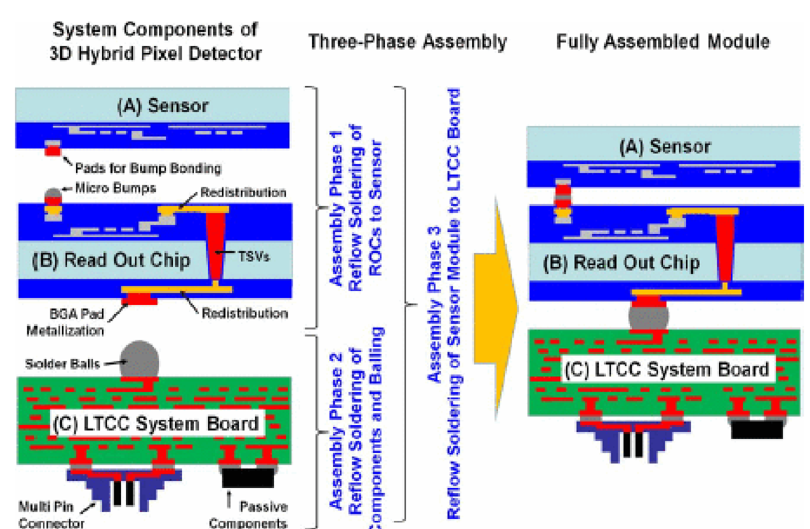


Srimani, 2019

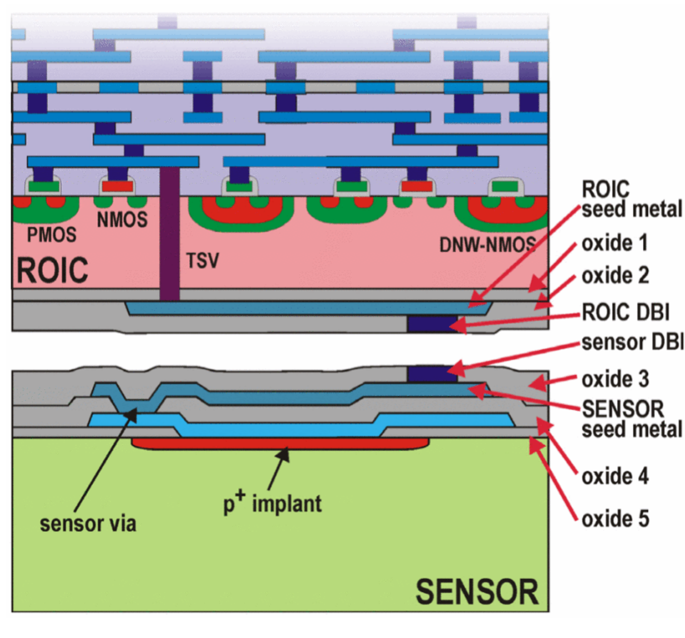


Multi-color detection
Geum, 2019

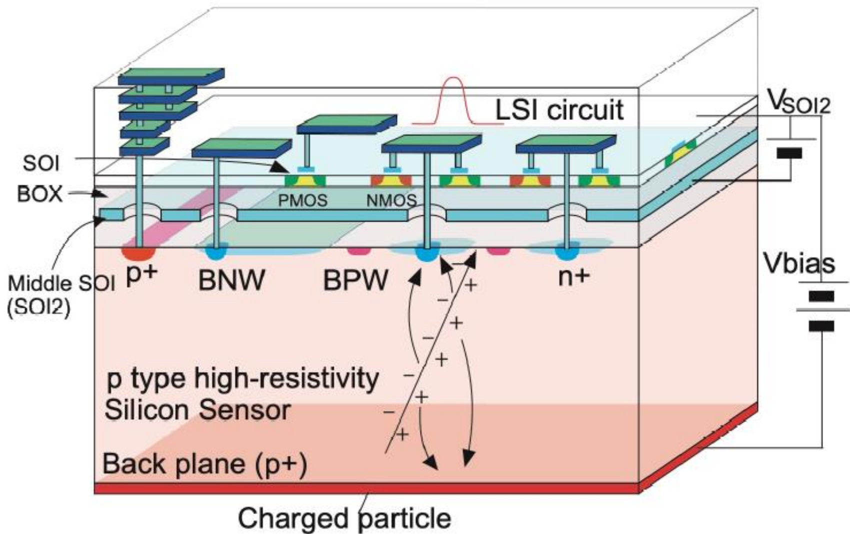
3D INTEGRATION: X-RAY DETECTORS

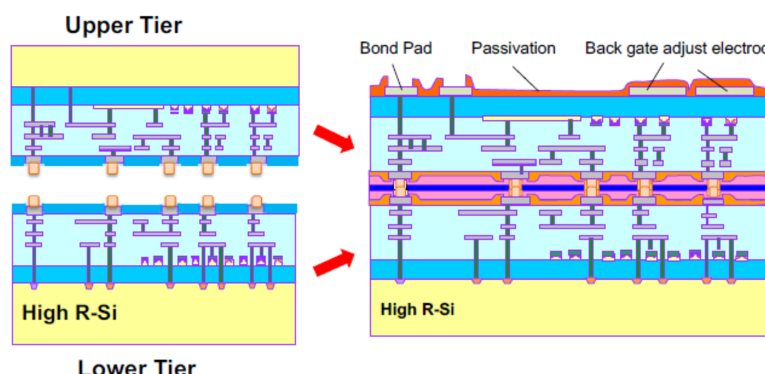


Zoschke, 2017



Deptuch, 2016



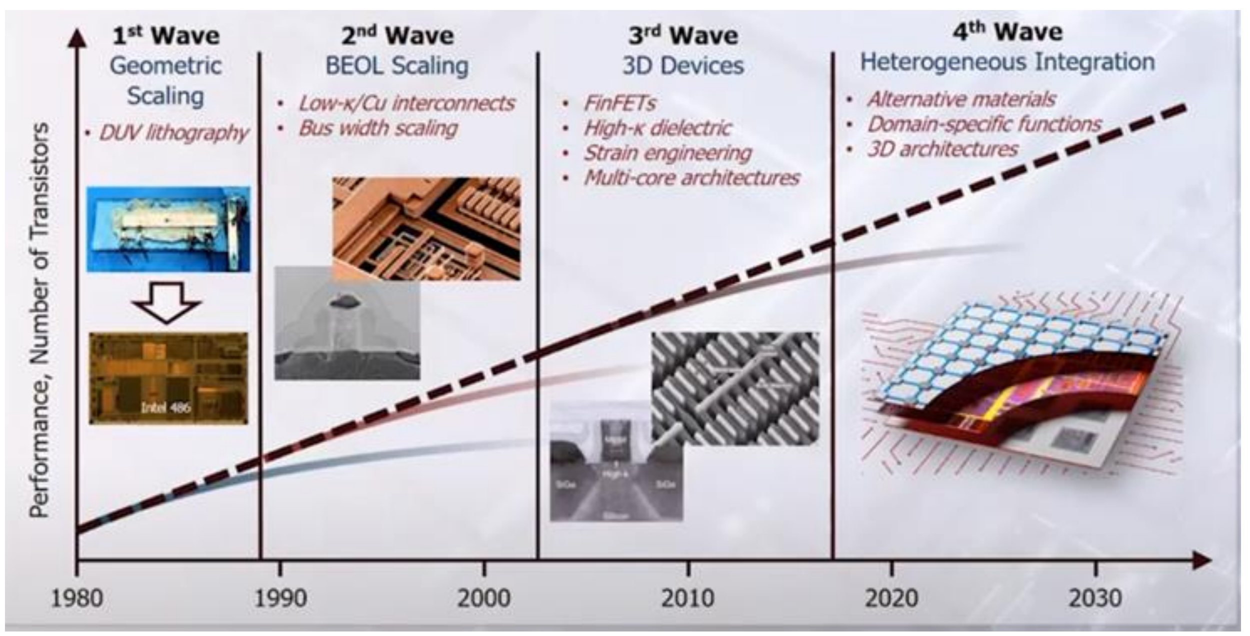


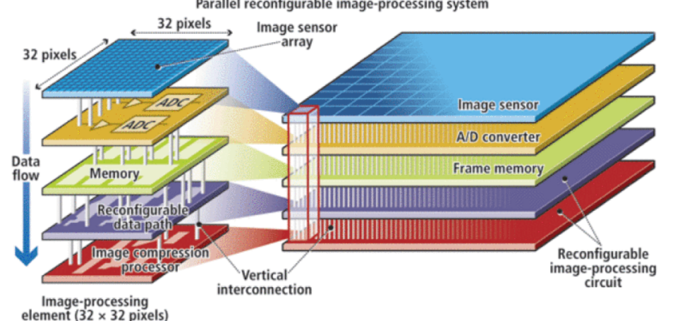
Yamada, 2019

TAKEAWAYS

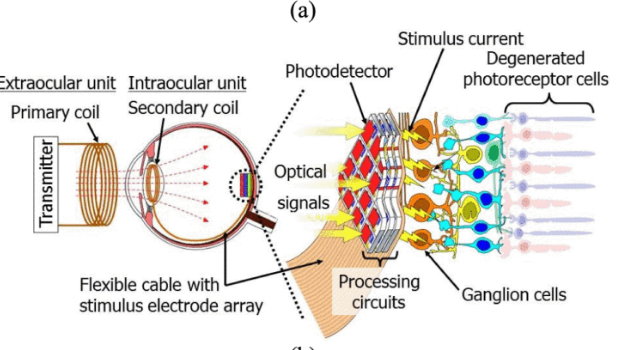
- **Several technologies are now available for achieving reliable and robust 3D integration**
  - One can almost stack anything on anything
  - Next phase of Moore's law
- **Main technology drivers for 3D integration:**
  - Cost, performance, power consumption
- **However 3D integration exhibits some issues:**
  - Thermal, stresses (TSV), electro-migration
  - **Cost**

- **"Image" sensors were the 1st 3D-integrated devices and will continue to pull the 3D integration technologies**



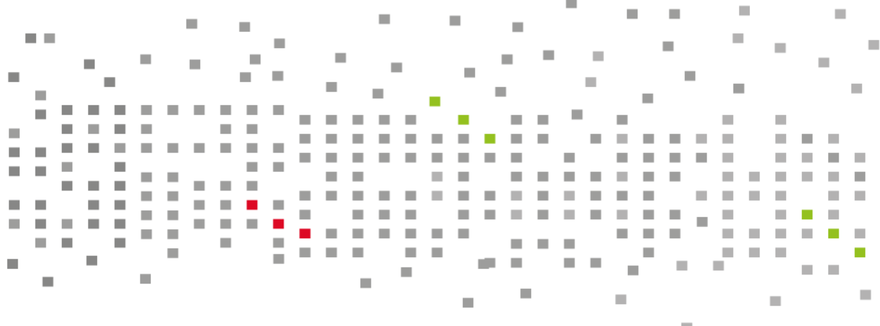


(a)



(b)

Retinal Prothesis
Koyanagi, 2013



Thank for your attention

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