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3D integration in nanoelectronics: Basic technologies and applications to image sensors

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The Moore's law, which governs the development of microelectronics for 50 years, is nearly ending due do its physical limits at the 2nm or 1nm technology nodes. In order to improve the device performance and for reducing the signal latency and the power consumption, the semiconductor industry has focused its efforts for stacking wafer on wafer, die on wafer, and die on die. This paper will review the basic technologies for achieving 3D chip integration, such as TSV, hybrid bonding, monolithic integration, and the chiplet approach. Applications of some of these technologies to visible and IR sensors will be presented.

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