Advanced Electronic Packaging Technologies for Hybrid Detectors

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Outline

- Flip Chip and Bonding Technologies
  - Status Bump Bonding
  - Flip Chip Technologies for 3D Assembly

- 3D Integration Technology for Hybrid Detector Modules
  - TSV Process – Introduction
  - TSV Last - Via Backside Process: ATLAS FE-I4
  - TSV Last - Via Front Side Process: AGH UFXC32k
  - Interposer
Introduction: Assembly of Hybrid Pixel Detectors

- Step 1: UBM deposition on sensor wafer
- Step 2: solder bump deposition on readout chip wafer
- Step 3: Flip Chip Assembly of readout chip to sensor chip

Advantages:
- Separate development and optimization of sensor and readout chip
- Variable use of different semiconductor sensor materials
Flip Chip Assembly Key Parameter: Interconnection Pitch

Fine pitch bumping:
Pitch 100...50μm
Bump size: 50...25μm
Material: Solder bumps, pillar bumps with solder cap

μ-bumping:
Pitch 50...20μm
Bump size: 25...12μm
Material: Solder bumps, pillar bumps

Sub-10μ-pitch:
Pitch 10...2μm
Bump size: 6...1μm
Material: pillar bumps, metal pins

Reduction of pixel pitch – more challenging assembly process
Bonding Technologies for 3D Chip Stacking

**Solder Bump Bonding**
- ECD solder bumps (SnAg, In, InSn, AuSn, Cu-pillar/Sn cap)
- Reflow temperature
- without or low pressure

**Transient Liquid Phase Bonding (TLPB/SLID)**
- ECD Cu and Cu-Sn pads
- High melting Cu$_3$Sn IMC
- Temperature, pressure

**Metal-Metal Direct Bonding**
- ECD pads (Cu, Au, Ni)
- Planarized surfaces, preconditioning
- Temperature, pressure

**Metal – Oxide Hybrid Bonding**
- ECD Cu pads (or Ni)
- Surface planarization (CMP)
- Surface activation (plasma)
- Room temperature bond
- Annealing step

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Solder Bumping on 300mm Wafer: RD53A/RD53B

- 300mm wafer, TSMC 65nm technology
- ~ 90/132 RD53A/ITKPix readout chips per wafer
- SnAg solder bumping, reflow temperature ~250°C
- Bump size and height ~25..30µm, pitch 50x50 µm²
- RD53A: 400x192 bumps (76.800 chip / 6.835.200 wafer)
- RD53B: 400x384 bumps (153.600 chip / 20.275.200 wafer)
- Volume production ready - complete 300mm wafer industry standard process line available

- Wafer thinned thickness:
  - 500µm for setup batch
  - 150µm for qualification batch
Hybrid Module Assembly – ATLAS/CMS ITK Pixel Detector Upgrade

- Assembly of single chip, double chip and quad chip hybrid modules:
  - 6” planar sensors 100µm, 150µm thickness
  - 6” 3D sensor wafer
  - 8” CMOS sensor wafer, 150µm thickness

- Readout chip size:
  - RD53A regular size ~2x1cm²
  - RD53A_BIG/ RD53B (ITKPix) size ~2x2cm²
Bonding without Solder: Metal-Metal Diffusion Bonding

- ECD Cu pads (Au, Ni)
- Planarized surfaces, pre-conditioning
- Bonding parameters:
  - 250°C...400°C,
  - 50...150MPa
  - t= min...h
  - Vacuum, inert atmosphere
- Available for wafer to wafer bonding
- R&D for Chip to Chip assembly

Cu, (Au, Ni)  
Cu, (Au, Ni)

(a)  
(b)  
(c)  
(d)

Cu-Cu bond  
Cu-Cu bond SEM image  
Au-Au bond
Bonding without Solder: Gold µ-pillar Thermo-Compression Bonding

- evaluation of thermo-compression (TC) bonding process
- Daisy Chain Test Design with MEDIPIX3 chip size, 256x256 bump matrix (65536 bumps per chip)

Reduction of Bonding Force:
- Regular pad: 30µm, 150MPa → ~7kN bonding force per chip
- Pillar pad: 10µm, 150Mpa → 770N bonding force per chip

- Chip to chip bonding
- Bonding temperature range: 250°C ... 300°C
- Bonding pressure: 100 ... 150 Mpa
- Applicable for Au-Au or Au-NiAu bonding
Metal – Oxide Hybrid Bonding

**Cu/SiO<sub>2</sub>**

**Process:**
- SiO<sub>2</sub> passivation + Cu pads
- Surface planarization (CMP)
- Surface activation (plasma, chemicals)
- Room temperature bond
- Annealing 150 – 300°C
- 3D chip stacking: memory chips, image sensors

**Motivation for DBI®:**
- W2W, D2W
- Highest interconnect density: I/O pitch down to 1 µm
- High alignment accuracy
- No bumps, no intermetallics
- No gap – no underfilling
- High reliability

**Fraunhofer IZM-ASSID:** 300mm W2W Bonding with <5µm alignment accuracy

**Fraunhofer test chip with 4 µm pad /18µm pitch, Metal density: 4.5%**

**Source:** J. Wolf „3D System Integration Requirements and Potential Solutions“, European 3D Summit, 22-24.1.2018, Dresden, Germany.

**Surface preparation in nanometer range → Atomic force microscopy**
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TSV Integration Schemes

**Via first or middle**
- TSV integration before FEOL or after FEOL / before BEOL
- Processes established at IDMs

**Front Side - Via last**
- TSV integration after complete wafer processing
- TSV through thick BEOL oxide
- Requires keep out zones in FEOL and BEOL for TSV integration
- Support wafer bonding
- Wafer backside thinning
- TSV reveal
- Backside RDL and bump formation
- Support wafer de-bonding

**Back Side - Via last**
- TSV integration after complete wafer processing
- Requires TSV adapted landing pad design in BEOL for TSV connection
- Support wafer bonding
- Wafer backside thinning
- TSV formation with access to landing pads
- Metall liner and backside RDL formation
- Support wafer de-bonding (if required)
Basic Process Steps of TSV Formation – TSV Backside – Via Last

1. Frontside process / carrier wafer bonding
2. Si-wafer thinning
3. TSV silicon etching
   DRIE BOSCH Process
4. TSV and wafer surface oxide passivation
   TEOS, PE-CVD, SA-CVD
5. Oxide Etch at via bottom
6. Barrier-/Seed-Layer
   Ti (TiW, TiN, Ta(N)) / Cu HI-PVD
7. TSV Cu filling + RDL Cu by ECD
8. Backside Passivation and Bond Pad UBM

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TSV Process with ATLAS FE-I4 readout chip wafer

**Backside TSV via last process:**

- Frontside UBM pixel pads (1)
- Frontside carrier wafer bond
- Backside thinning (100µm/80µm)
- Backside TSV Si etch and oxide passivation (2)
- Oxide etch on BEOL-M1-Layer
- TSV/RDL-Cu metallization (3)
- Backside passivation layer
- Backside UBM contact pads (4)

ATLAS FE-I4 after TSV process:
Cross section of backside TSV
Wafer thickness 100µm and 80µm
ATLAS FE-I4 TSV Hybrid Module Assembly

1st Level Assembly Flip Chip Bonding to Sensor:
- Assembly onto MPG HLL planar sensor
- Sensor with solder bumps

Hybrid modules with ATLAS FE-I4 chips on top:
2 layer RDL connecting all WB pads for the power nets: VDDD, DGND, VDDA, AGND. Ni/Au layer pad metallization

Cross sections of hybrid module:
80μm thick ATLAS FE-I4 TSV ROC top, MPG-HLL sensor bottom

2nd Level Assembly at Bonn University:
- Module Attach to PCB
- Sensor on top and HV wire bonded to frontside of the PCB
- FE chip connected via TSVs from the PCB’s backside through a hole of the PCB

Images 2nd Level Assembly by Fabian Huegging © Bonn University

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ATLAS FE-I4 TSV Bare Chip and Hybrid Module Test

Bare chips with both RDL types are working well:

- Performance in terms of threshold, noise, data transmission is similar to standard FE-I4B chips
- Noise of ~120e- at thresholds of 2000e-
- Data transmission at 160 MBit/s showed no issues with the additional capacitance load of the TSVs

Hybrid Module Test (2 modules tested):

- Both modules are working well
- Very good bump connectivity, one module shows a few disconnected pixel at one edge (maybe handling issues during BB)
- Noise is about 180e- at 1650e- threshold with a dispersion below 40e-

Source scan: Sr90, 60s, 60V

F. Hügging et. al., Advanced Through Silicon Vias for Hybrid Pixel Detector Modules, DOI: 10.1016/j.nima.2018.08.067
TSV Back Side - Via Last 3D Integration

3D Wafer Level CSPs for Fabrication of 4×4 Optical Sensor Arrays

- Wafer level packaging of sensor chips with through silicon vias (TSVs)
- Each sensor chip is protected by a thin glass layer which is transparent for light
- Redistribution of electrical connections to back side of chips enables four side stitching with minimal gaps
- 4x4 array assembly of sensor chips onto PCB by pick & place and reflow soldering
Basic Process Steps of TSV Formation – TSV Frontside – Via Last

1. TSV blind hole etch and isolation
2. TSV filling
3. Front side RDL
4. Front Side Passivation / IO Formation
5. Temporary bonding
6. Si-wafer thinning
7. TSV Reveal
8. Back Side Passivation
9. Back Side RDL
10. Back Side RDL + passivation
11. BGA Bump Pad Formation
TSV Frontside – Via Last Process: Ultra Fast Xray Pixel Matrix Chip

UFXC32k Readout Chip developed by AGH Krakow, Poland

Process at IZM:
- TSV-frontside process
- Completely-filled Cu-TSV
- Frontside and backside RDL
- Frontside Solder Bumps/Pillars
- Backside solderable Pad Metallization
- 1st level assembly: hybridization of two ROICs to silicon sensor
- 2nd level assembly: Bonding to LTCC substrate

Cross section of Bare Module, with Cu filled TSVs in ROC

Silicon Bare Module, with sensor and two UFXC32k TSV-ROCs

X-ray Detector Module: Sensor + TSV-ROC + LTCC Board; x-ray image of chip package

Silicon Interposer - Front Side Via First / Back Side Via Last

2.5D Interposer Assembly for GPU Device

2.5D Interposer as liquid Cooling Device

- Interposer on 200mm wafer
- Cu-TSV density > 10000/cm²
- 42,459 TSVs per Device

2 half-shells forming a microchannel cooler

Cu/Sn TLPB W2W bond or AuSn TLPB W2W bond

Fluid port micro-channel micro-seal (TSV connection)
Glass Interposer with Through Glass Vias (TGV)

TGV – metallization process setup wafer

- 200 mm glass wafer
- Wafer thickness 300 μm
- Through glass vias diameter 60 μm
- Cu filling on side wall
- Double sided RDL coating
- Glass interposer for RF application

TGV cross section and TGV-daisy chain structure for reliability investigation

RF-Transceivers using Glass Interposers
Transceiver 4x28GBit/s

![Image of RF-Transceivers using Glass Interposers](image-url)
Outlook

- 300mm readout chip wafer becomes the standard in HEP
- 300mm process equipment: automated handling is industry standard
- 300mm wafer tools require more space / more cost
- Bumping and other metal deposititon technologies are available on industry standard level
- Semi-automated tools → R&D with low wafer number possible
- 3D integration process is more complex due to several vacuum processes
- Individual process steps on 300mm wafer require extensive process setup
- Availability of large 300mm wafer batches for R&D setup not given so far
  → option: provision of large wafer number R&D batches
  → option: down sizing of 300mm to 200mm and use of semi-automated 200mm TSV process equipment
thank you for your attention

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