RD53 pixel chip developments for the ATLAS and CMS High Luminosity LHC

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on behalf of the RD53 Collaboration

and ITkPixV1 Testing Team

RD53 Collaboration

RD53 Collaboration is a joint effort between ATLAS and CMS to develop readout chips for the HL-LHC pixel detectors

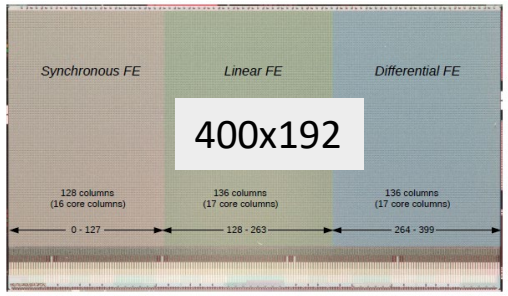
1. Characterization of chosen **65nm CMOS** technology in radiation environment
2. Design of a **rad-hard IP library** (Analog front-ends, DACs, ADCs, CDR/PLL, high-speed serializers, RX/TX, ShuntLDO, …)
3. Design and characterization of **half-size pixel chip demonstrator (RD53A)** with design variations

4. Design of pre-production (**RD53B**) and production (**RD53C**) pixel readout chips

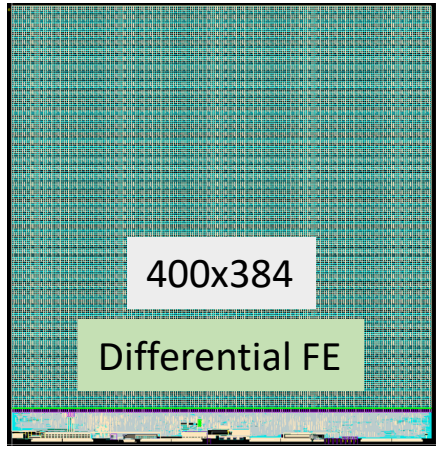
   ATLAS and CMS chips are two instances of the same common design, having different size and Analog Front-End, according to specific requirements of the experiments

	ATLAS/CMS
Chip size	20x21mm^2/21.6x18.6mm^2
Pixel size	50x50 µm^2
Hit rate	3 GHz/cm^2
Trigger rate	1 MHz/750kHz
Trigger latency	12.5 us
Min. threshold	600 e-
Radiation tolerance	500 Mrad @-15C
Power	< 1W/cm^2

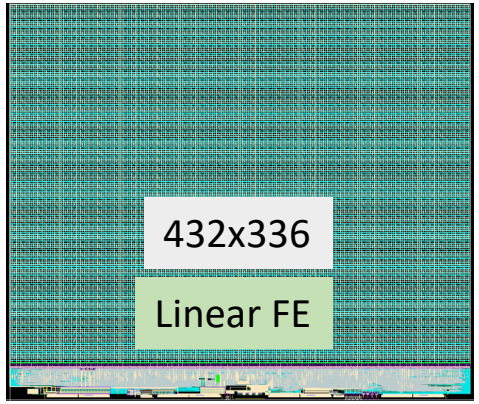
https://cds.cern.ch/record/2663161



RD53A
- submitted in August 2017
- Size: 20 x 11.5 mm2



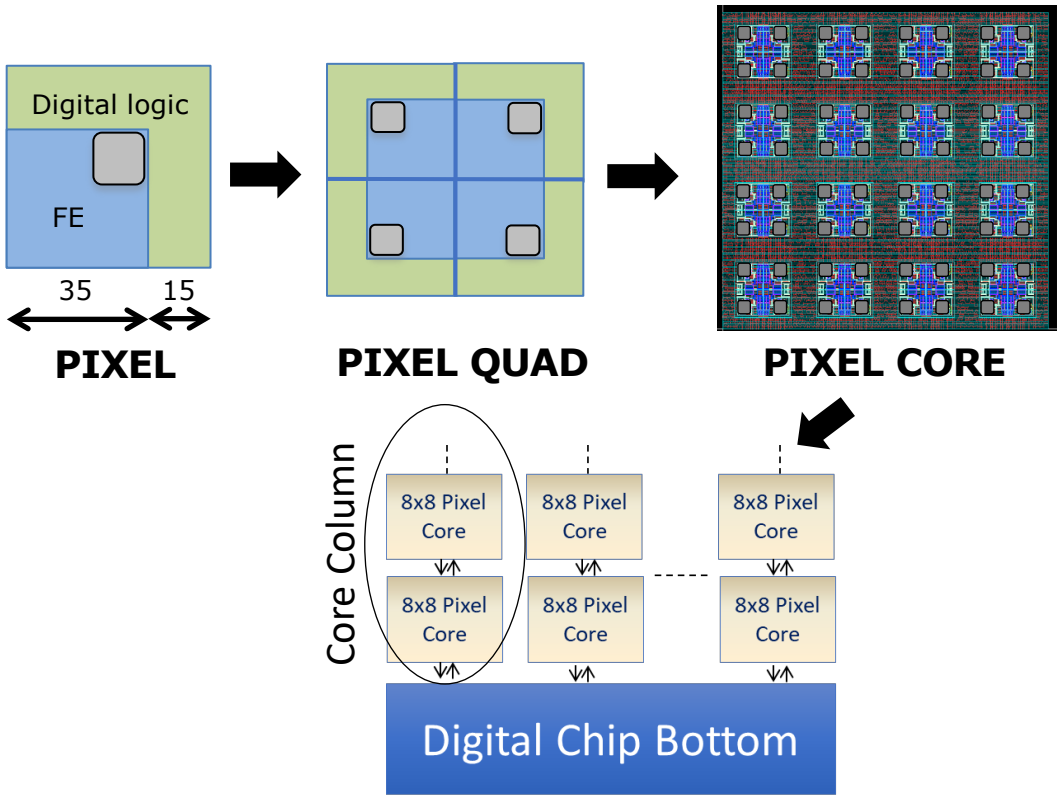
RD53B-ATLAS (ItkPix_V1)
- submitted in March 2020
- size: 20 mm x 21 mm

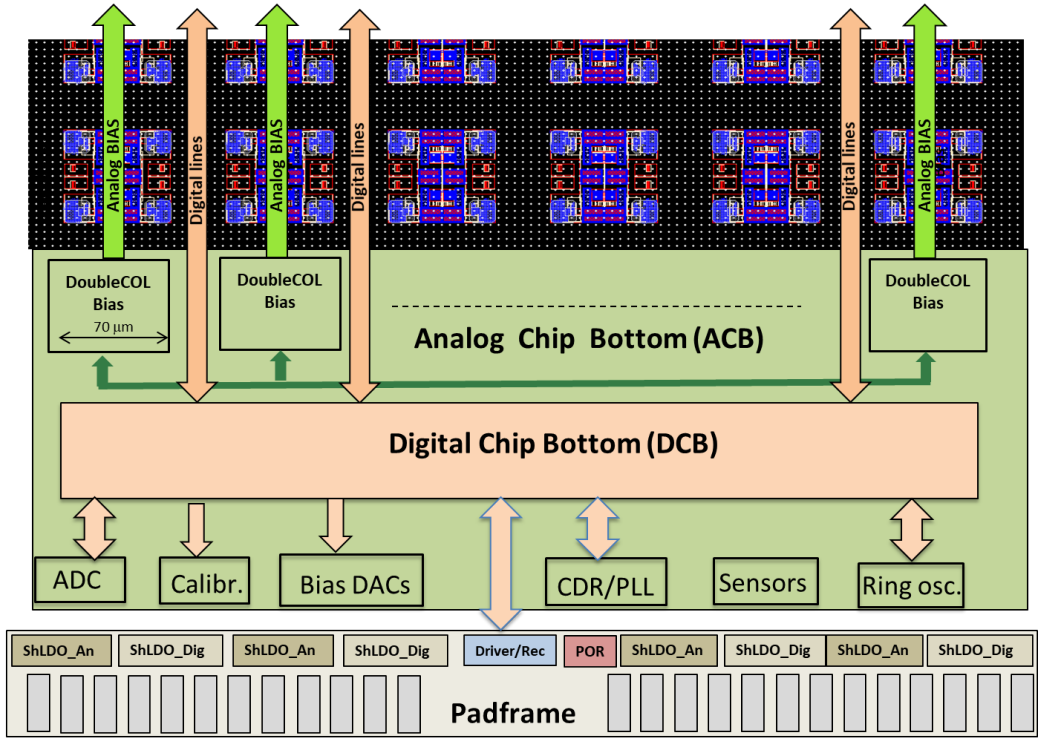


RD53B-CMS (CROC_V1)
- to be submitted in March 2021
- size: 21.6 mm x 18.6 mm

RD53C-ATLAS: Q4 2021
RD53C-CMS: Q1-Q2 2022

Floorplan





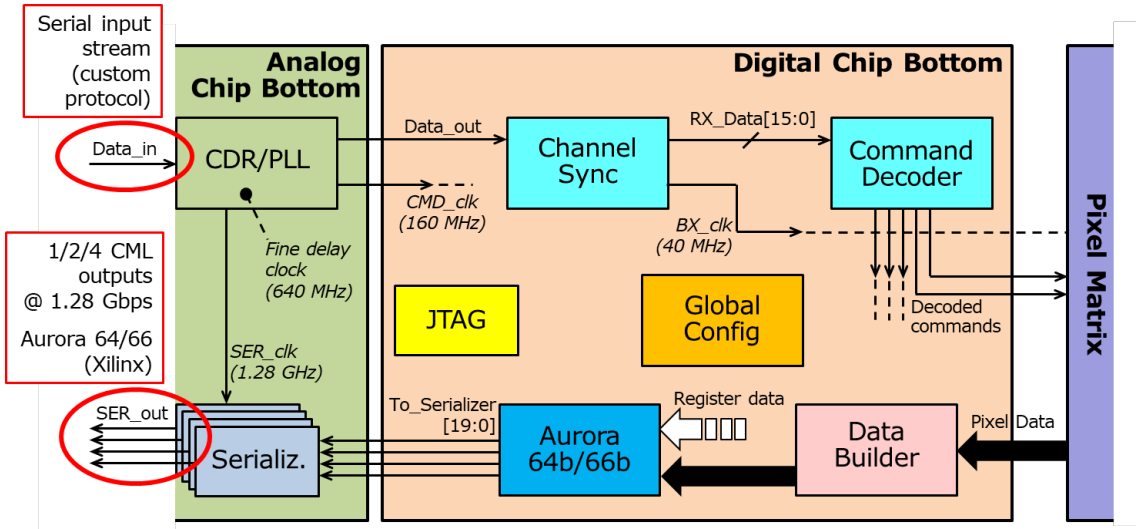
Pixel array

- Built up of **8 x 8 Pixel Cores** → **16 quads**
- All Cores are identical → efficient hierarchical verifications
- Cores are abutted: each Core receives all input signals from the previous one (closer to the DCB) and regenerates them for the next Core → no external routing for connections

Chip periphery

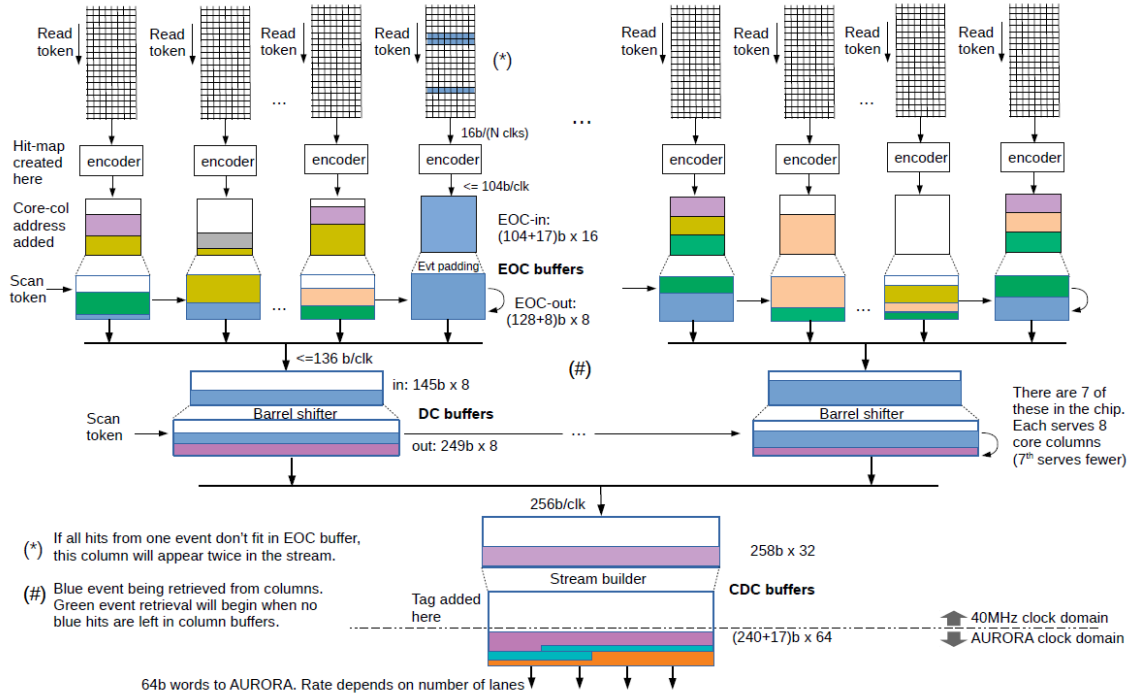
- Analog Chip Bottom (ACB): analog and mixed/signals building block for Calibration, Bias, Monitoring and Clock/Data recovery
- Digital Chip Bottom (DCB): synthesized digital logic
- Padframe: I/O blocks with ESD protections, ShuntLDO for serial powering

Data flow architecture

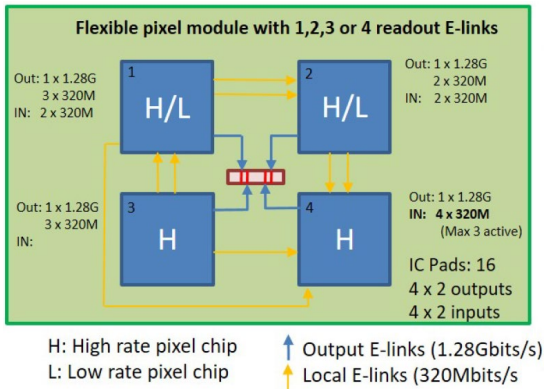


- Hits are stored as Time-over-Threshold, associated to a time stamp
- 6-bit ToT counter, but only 4 bits are stored and read-out
- Each pixel has 8x4-bit ToT memories
  - Support of 6-to-4 ToT mapping (dual slope)
  - Selectable counting clock: 40 MHz or 80 MHz
- The time stamp memory is shared among 4 pixels of the same 4x1 **Pixel Region**

- Token-based readout of hits, organized in Core Columns
- Multiple levels of data processing, event building, buffering and formatting before final readout via serial links

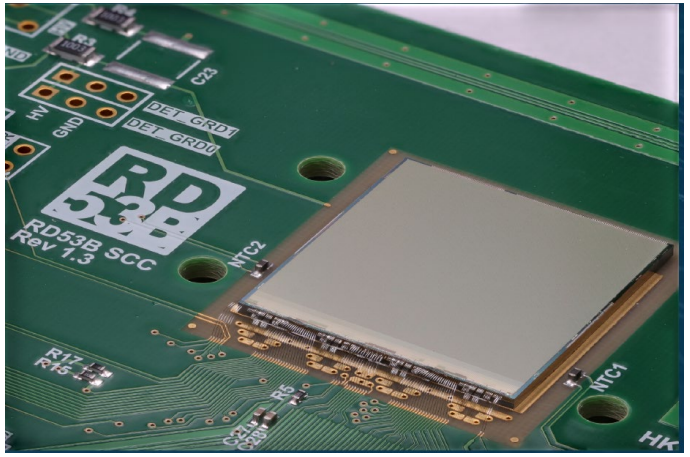


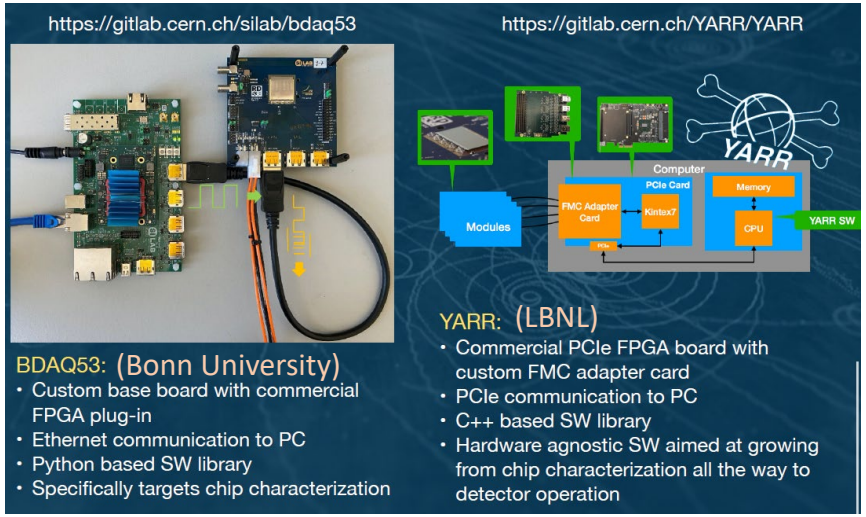
- **Command, control and timing** is provided by a **single 160 Mbit/s** differential control link, driving up to 15 chips (4 bit addressing)
  - CDR/PLL recovers Data and Clock
- **Readout via serial links** (1-4 x 1.28 Gbit/s) using Aurora 64/66 encoding
- **Multi-Chip Data Merging** available for low-rate outer pixel layers: one chip of the module can be configured as "primary" to aggregate serial data from one or more other "secondary" chips and merge them with its own output



RD53B-ATLAS testing

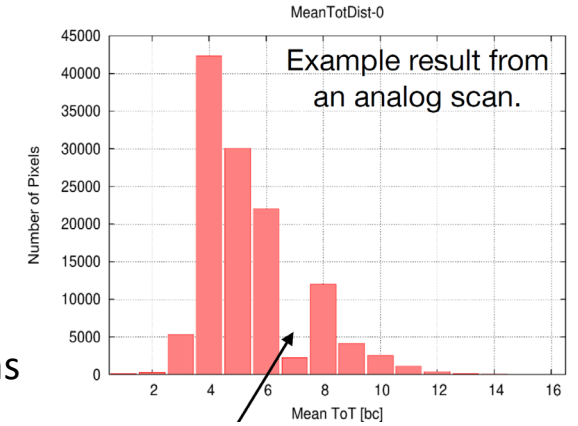
RD53B-ATLAS (ITkPixV1) received in June 2020





Upon first power-on, we observed an **abnormally large digital current (2-3A instead of 200mA)**

- Bug in the design of the custom 4-bit latch used to implement the ToT memory to save ~ 50% memory area, otherwise all the required functionalities could not fit in the constrained pixel area
- high current consumption when inputs differ from stored values in latched state. Since at power-up the latch state is random, this results in large current consumption upon power-up
- also causing corruption of stored ToT values when multiple bits are "1"



Missing hits for ToT=7

Despite this problem, **most blocks and all digital functionalities can be tested in this version:**

- setting all ToT memories to '0000', the chip is set in normal current state
- Analog front-end can be characterized using the precision ToT feature
- Radiation and SEU test could be performed
- Only limitation: high power-up current makes it impossible to use this chip for system testing of power chains
- High current issue solved by a patch in metal layers applied to 4 wafers being held at foundry without metallization → ATLAS ITk Pixel pre-production will rely on this patched chip **ITkPixV1.1**

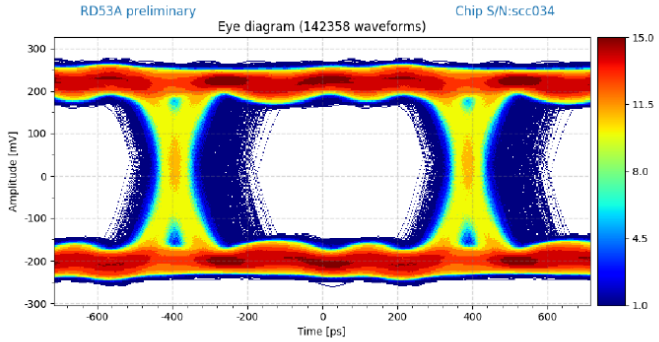
CDR/PLL

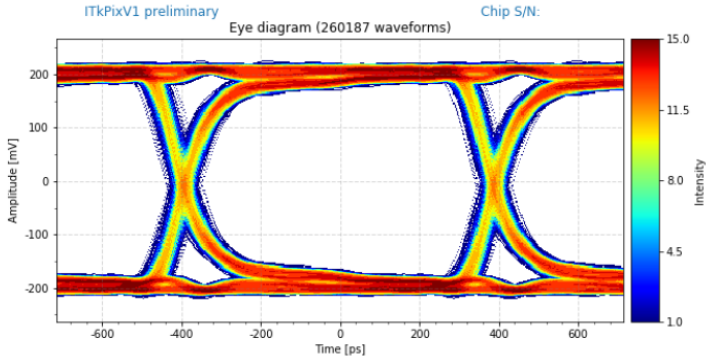
- **CDR/PLL greatly improved compared to RD53A in terms of jitter and start-up reliability**
- **Aurora output link stable with good quality**

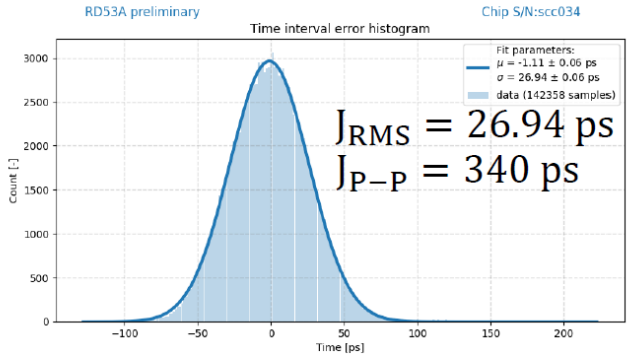
Input jitter = 5ps rms

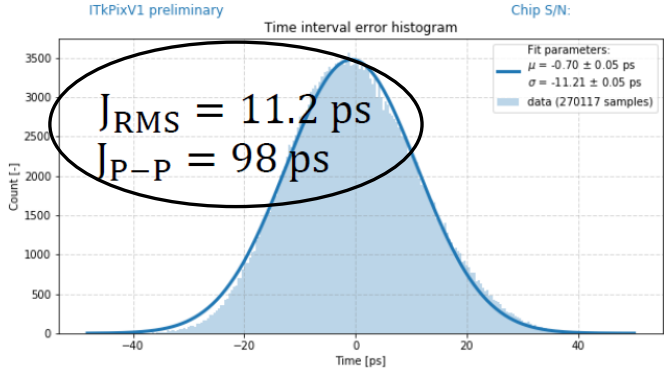
- **RD53A**
- Input: Threshold scan
- Output: Aurora (1.28 Gbps)

- **ITkPixV1**
- Input: PRBS5
- Output: Aurora (1.28 Gbps)





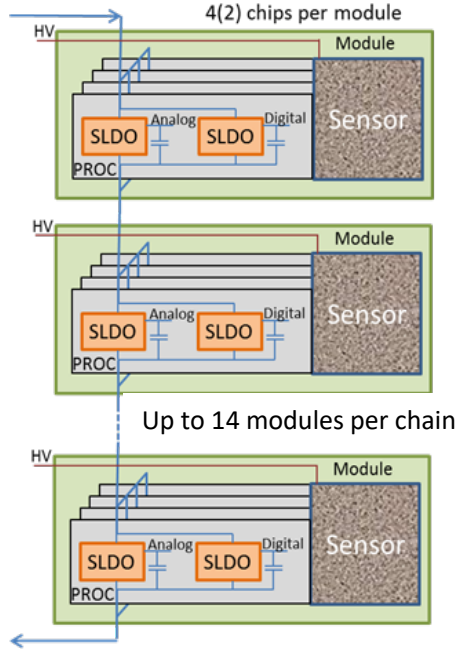


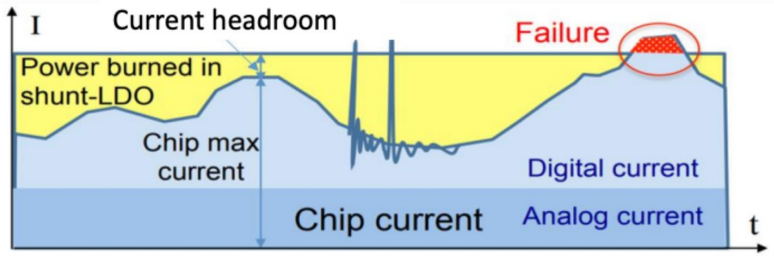


ShuntLDO for Serial powering

ATLAS and CMS will adopt for the upgrade pixel detectors a **serial powering scheme:**

- **ShuntLDO** regulators in the readout chips (1 for Analog, 1 for Digital domain)
- **Constant input current Iin** is shared among chips (2÷4) on the same module (less cables)
- Modules are in serial chains: "recycle" current from one module to another
- I_{in} dimensioned to satisfy the highest load, with ~20% headroom for stable operation, absorbed by the Shunt device
- In case of chip failure, its current can be absorbed by the other chips of the module
- Not sensitive to voltage drops (low mass cables)
- On-chip regulated supply voltages, low noise
- Radiation hardness (> 500 Mrad) silicon proven in RD53A and next prototypes

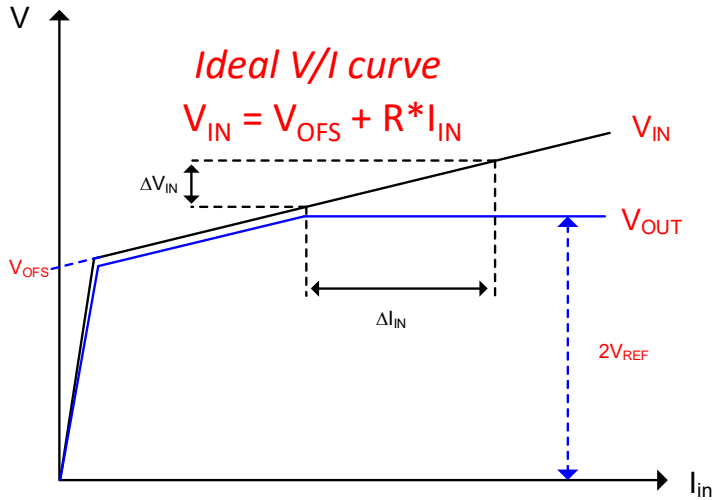




Example current consumption of one readout chip

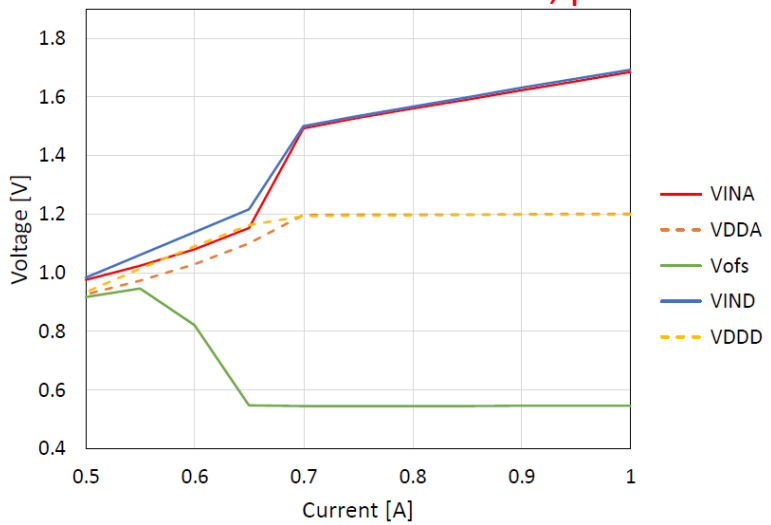
Protections:

- *Over-voltage protection*: V_{IN} clamped to 2 V
- *Under-shunt protection*: V_{OUT} decreased in case shunt current goes below a certain threshold (due to excess load current)

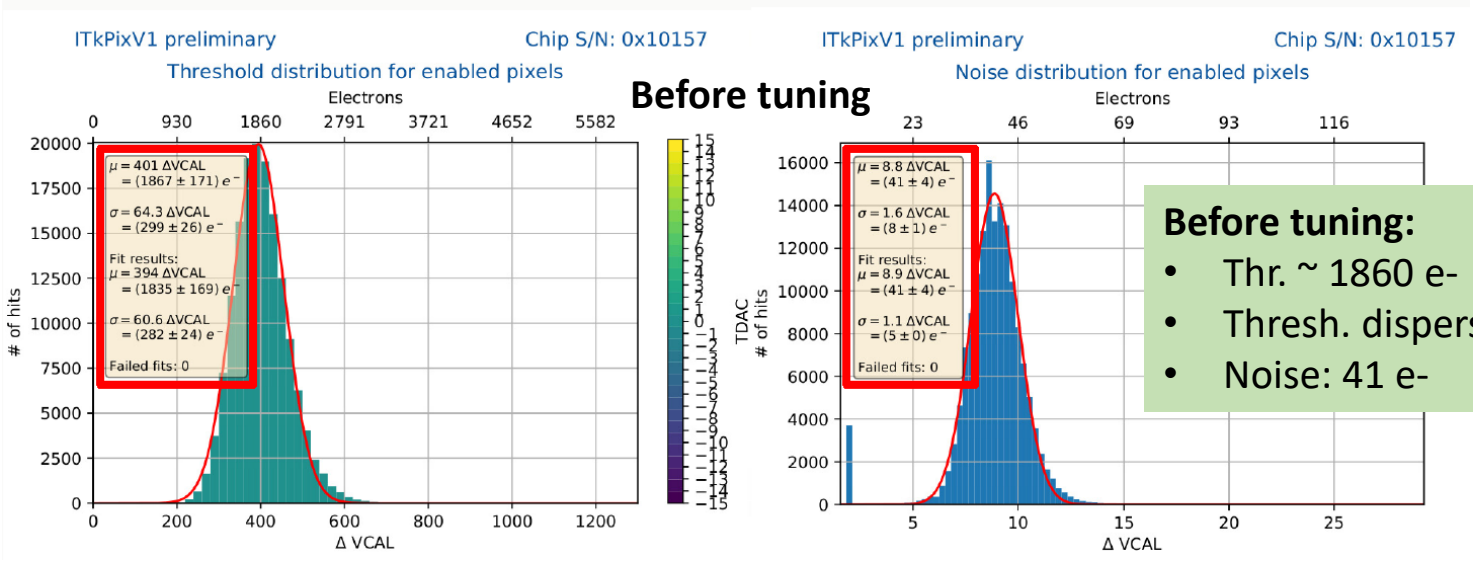


- V/I curve parameters (Voffset, slope) defined by external resistors
- V_{OUT} tunable by chip configuration

ITkPixV1.1 measurement at room T, pre-rad



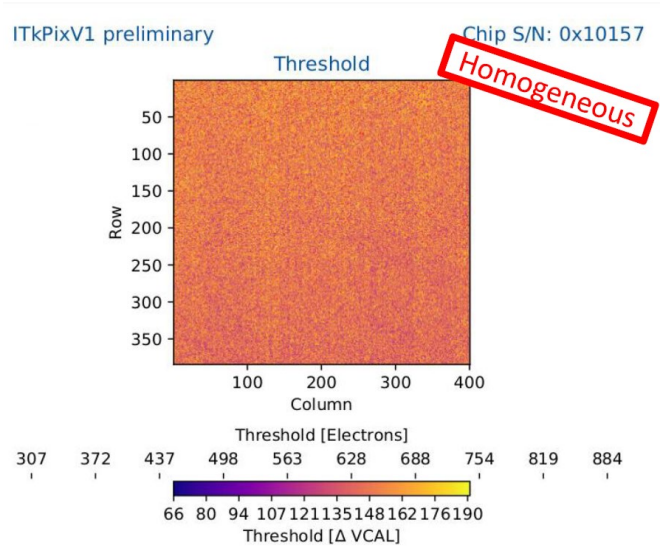
ITkPixV1 Front-End threshold tuning and noise

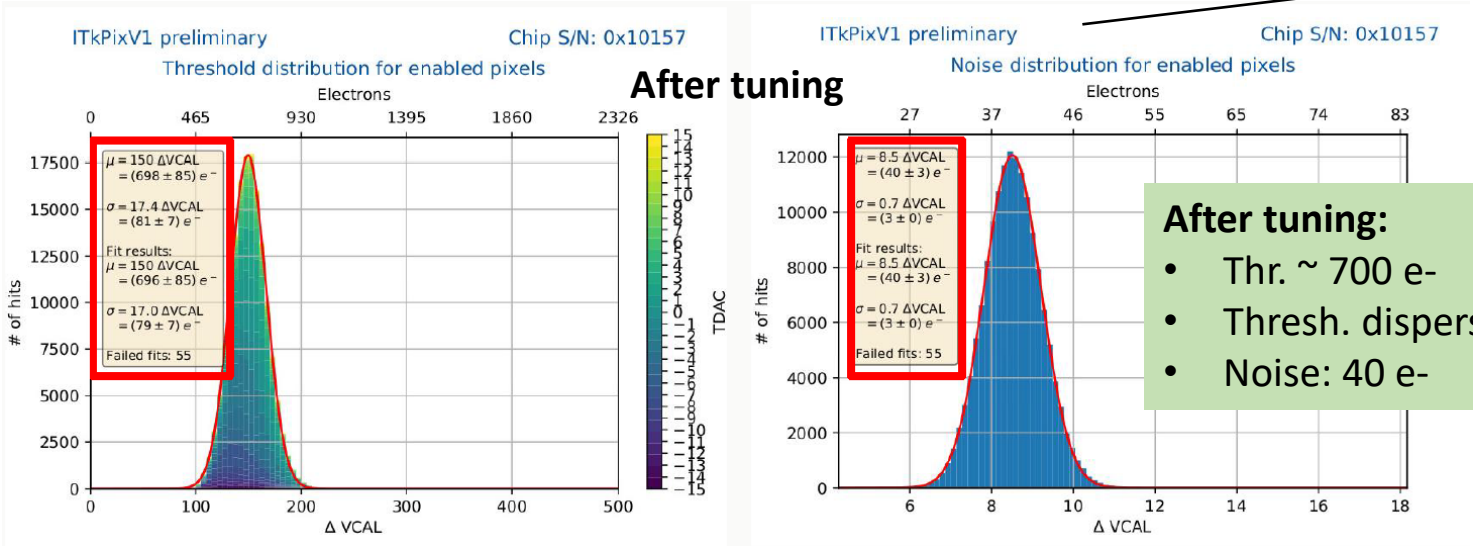


Before tuning

Before tuning:

- Thr. ~ 1860 e-
- Thresh. dispersion: ~ 300 e-
- Noise: 41 e-

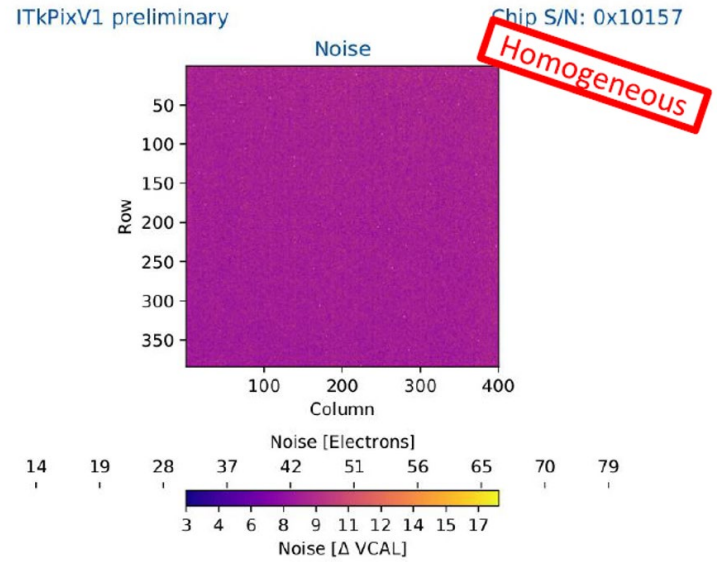




After tuning

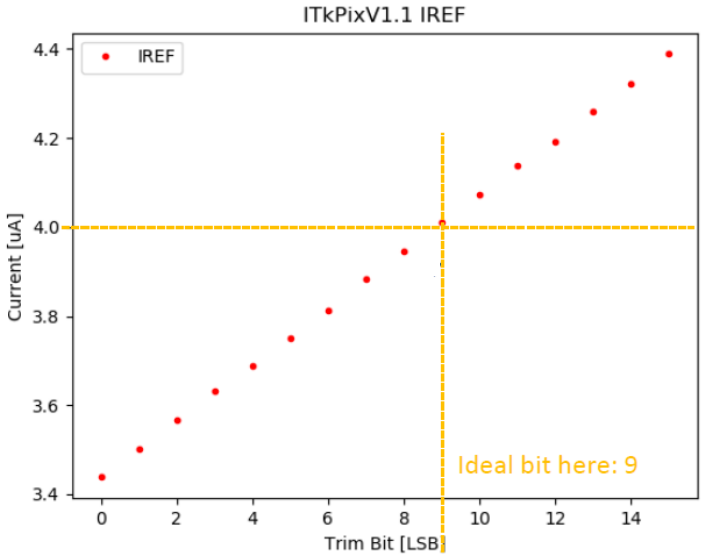
After tuning:

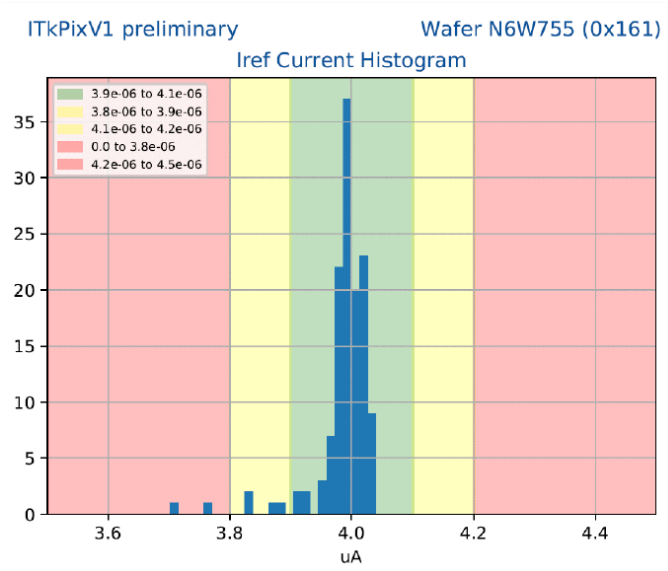
- Thr. ~ 700 e-
- Thresh. dispersion: ~ 80 e-
- Noise: 40 e-

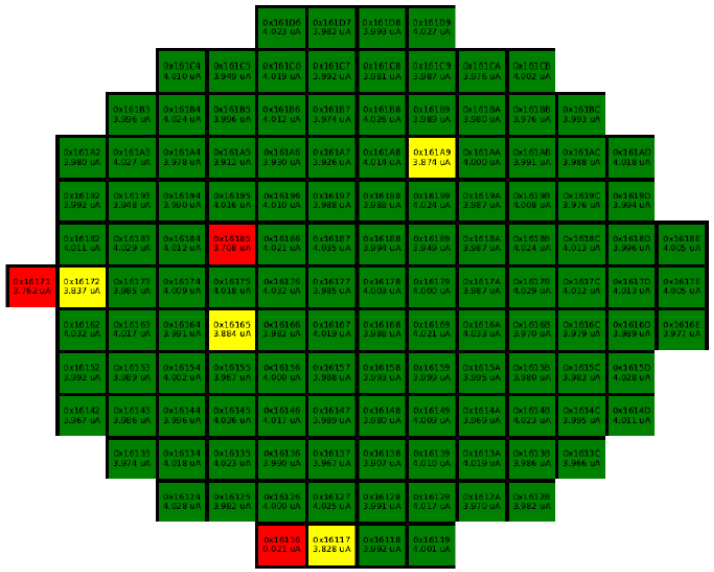


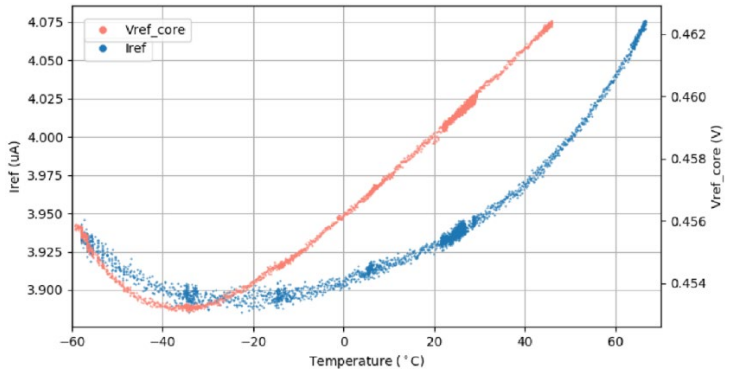
Bias circuit

- BIAS network is based on Bandgap reference circuits, to provide a reference voltage/current with low sensitivity to temperature variations
- Tuning by means of 4 wire-bond trimming pads (no risk of SEU bit flips), whose optimal value is found during **wafer probing**
- The tuned current I_{ref} is replicated and used as reference to 23 Digital-to-Analog converters to bias the analog Front-end, the CDR and other IPs

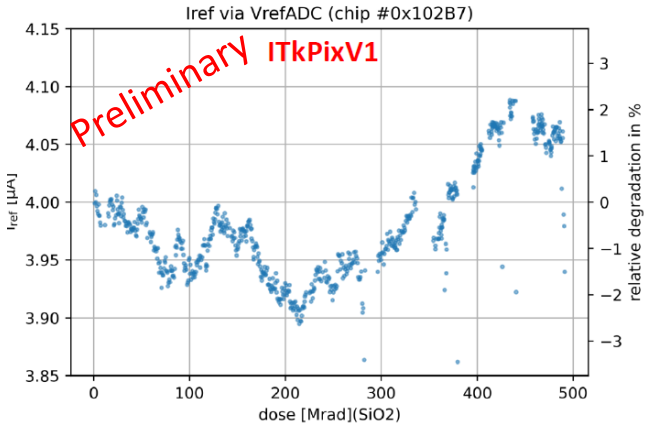




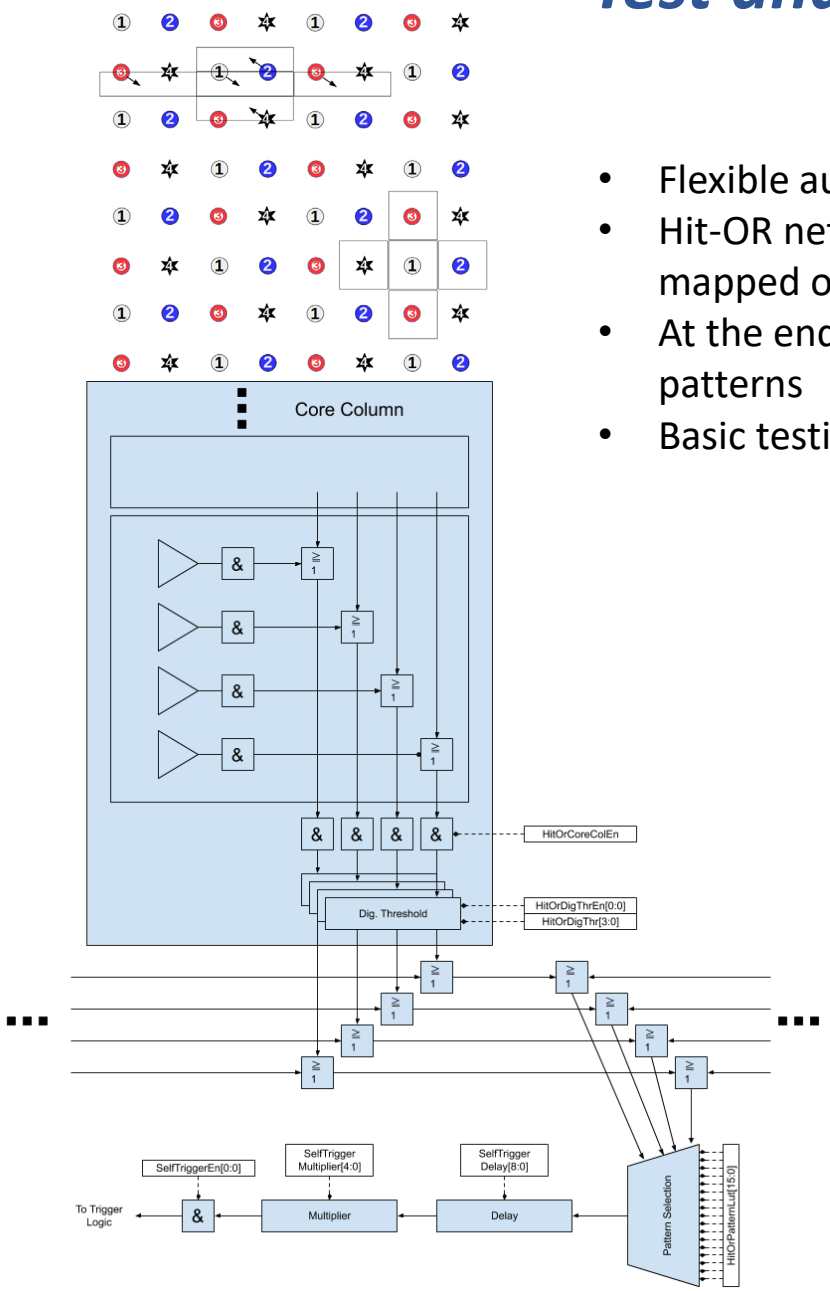




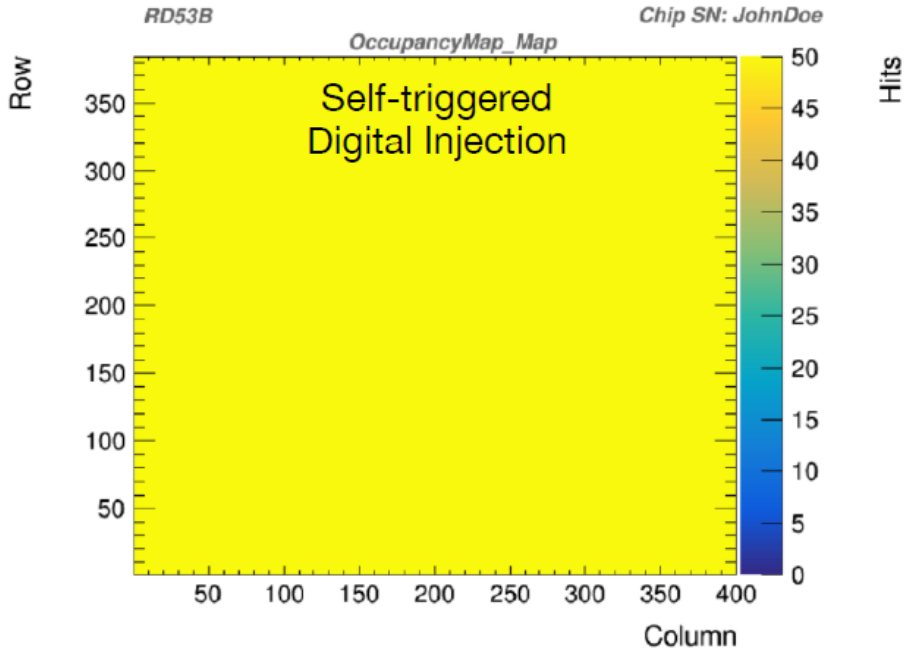
4% difference over
120°C temp. range



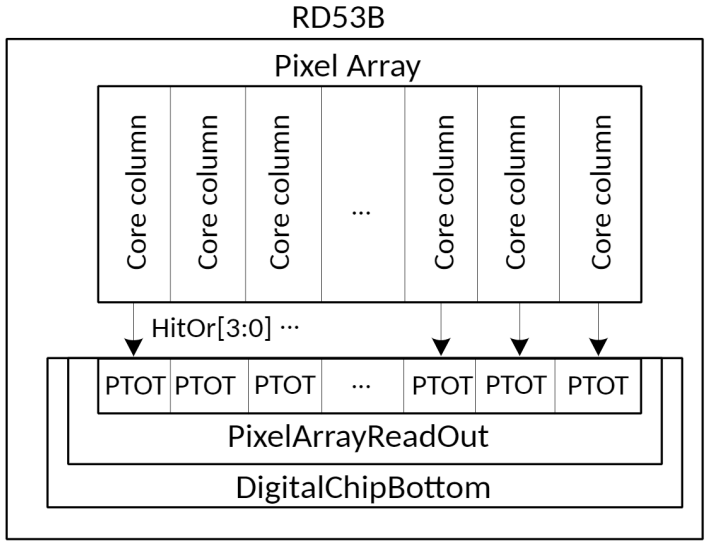
Test and debugging features: Self Trigger



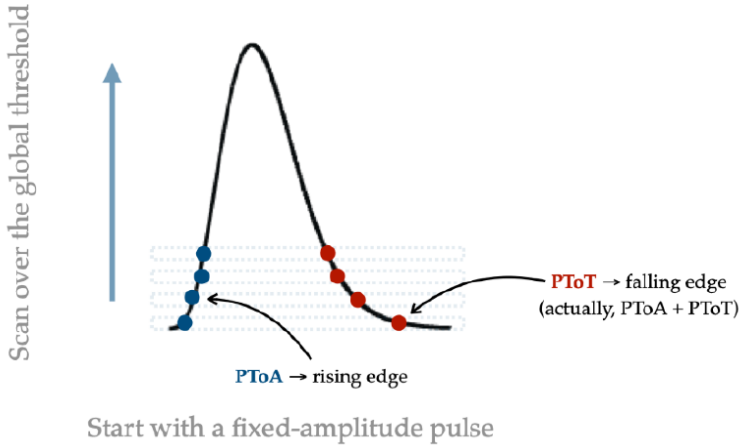
- Flexible auto trigger function, based on a Hit-OR network from the pixel array
- Hit-OR network consists of 4 OR lanes per Core Column, with a mapping such that neighbor pixels are mapped on different lines
- At the end of Core Column, the 4 lanes are combined to build the global Hit-OR with programmable patterns
- Basic testing with digital injection show that is **working as expected**



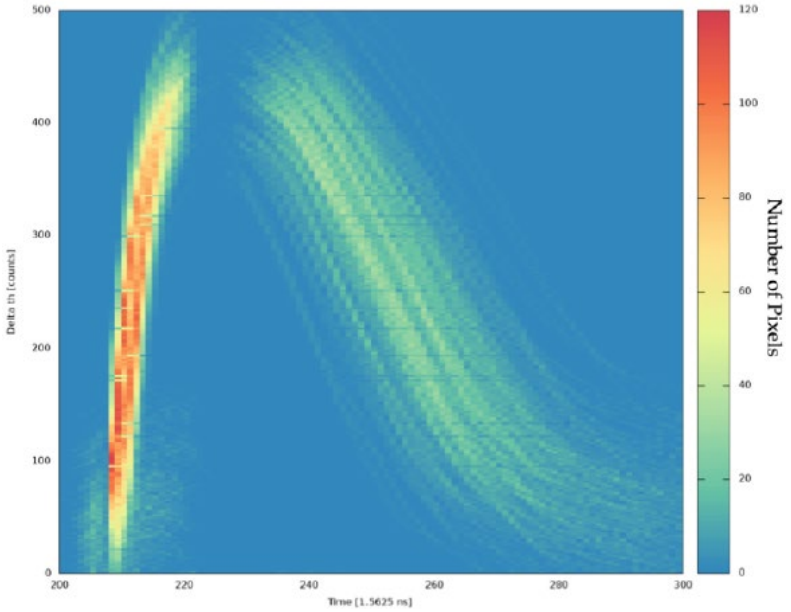
Precision ToT and ToA

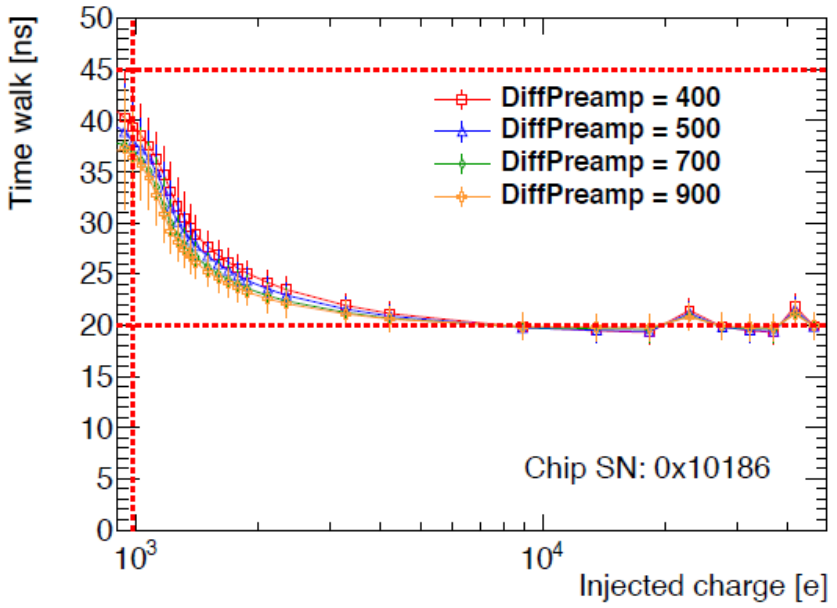


- PTOT module can be used for high resolution **Time over Threshold** and **Time of Arrival** measurement of the HitOR lines, using 640 MHz counting clock (1.5625ns resolution)
  - 11-bit PToT counters
  - 5-bit PToA counters, measuring the phase difference from HitOr leading edges and next BX clock rising edge
- Each Core Column is equipped with a PTOT module. Can be triggered for readout via the normal path, just like a Pixel Core
- Can be used to make precision measurements of analog front-end, like time walk, and also as a workaround for the bug in the pixel ToT memory
- Allows to reconstruct the amplifier output waveform (sort of oscilloscope)



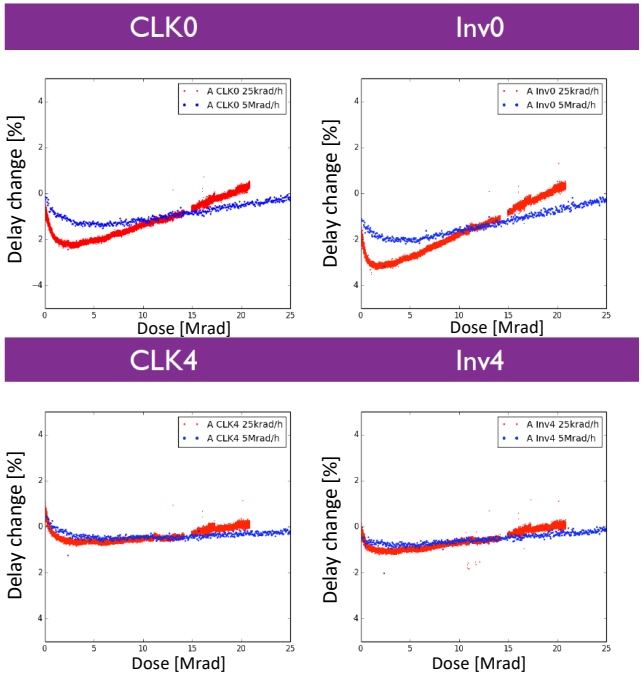
- Inject fixed calibration pulse
- Scan the threshold
- Sample PToA and PToT at each step





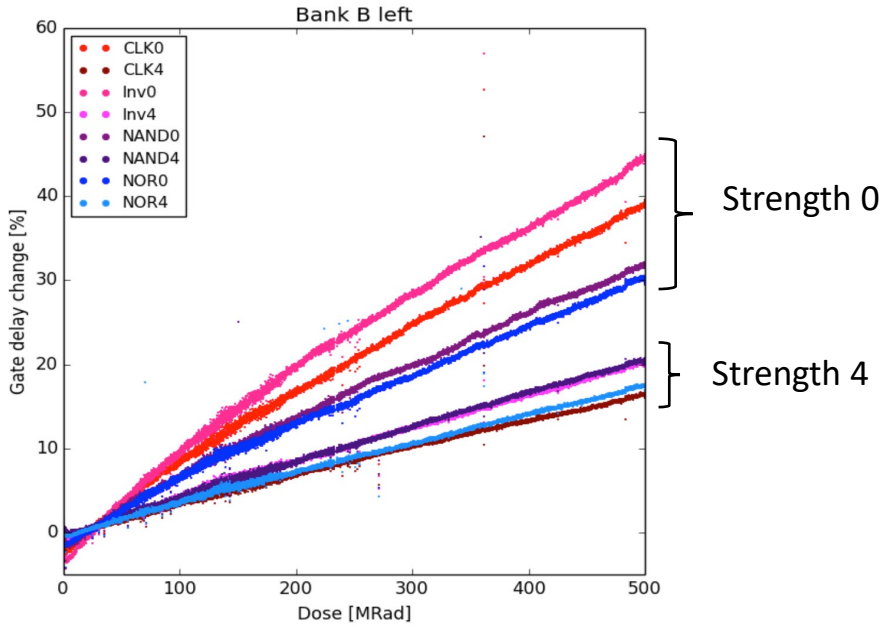
Radiation hardness

- Extensive TID X-ray tests done in the past years on RD53A and small prototypes to qualify IPs, analog FEs and digital standard cells
- The TID damage concerns essentially the digital design because of the small area devices
- Tests done at low temperature (-20°C) and high dose rate show that the RD53A chip is operating correctly up to 1 Grad
- From measurements on Ring Oscillators (RD53A and RD53B): **gate delay degradation roughly x2 larger for low dose-rate (LDR)**



Compare 5 Mrad/h and 25 krad/h

ROSC	Delay slope [%/MRad]		
	HDR	LDR	Ratio
CLK 0	0.051	0.121	**2.34**
CLK 4	0.012	0.026	**2.32**
Inv 0	0.076	0.176	**2.31**
Inv 4	0.029	0.055	**1.94**
NAND 0	0.034	0.085	**2.52**
NAND 4	0.008	0.016	**1.91**
NOR 0	0.051	0.097	**1.91**
NOR 4	0.031	0.051	**1.61**



Correction of HDR results using the ratio LDR/HDR

- Irradiation corner models and extreme corners from the foundry were used to predict the TID effect and design to guarantee good timing for the digital design. These corners resulted to be more pessimistic than the extrapolations of low dose-rate tests to 500 Mrad
- These tests, together with the policy to **avoid minimum size digital cells**, give confidence that RD53B chips will meet TID specifications if **operated at cold temperature**. Irradiated chips must be cooled while under power, **since room or high temperature annealing is detrimental**
- X-ray campaigns ongoing in different sites to fully characterize the analog FE and other IPs

SEU

Adopted strategy for SEU mitigation

- Pixel configuration registers with Triple Modular Redundancy (TMR) but without self-correction for lack of area in the pixel
- Global configuration and state machines in the chip periphery with TMR, self-correction and triplicated clock tree with skew
- Different structures and critical blocks (PLL) have been verified with analog SEU/SET injection simulations
- SEU in the digital logic, including pixel array have been verified with extensive SEU simulations

SEU tests on RD53B-ATLAS with heavy ions and protons

- evaluate the register cross-sections
- most of the tests performed in Bypass mode (external clock) to disentangle eventual effects on the CDR/PLL
- no major issues found in PLL mode in the proton beam, but a dedicated campaign is needed (GANIL, April 2021)
- No latch-up, no chip-stuck (limited statistics)

Site	Date	Beam type	Bypass/PLL mode
Louvain-la-Neuve	08.10.2020	Heavy ions	Bypass
Louvain-la-Neuve	17.11.2020	Heavy ions	Bypass
TRIUMF	20.12.2020	480 MeV protons	Bypass PLL

- Global configuration registers: $\sigma_{latch} / \sigma_{TMR\_with\_correction} \sim 400$
- Pixel configuration registers: $\sigma_{latch} / \sigma_{TMR\_no\_correction} \sim 100$ (assuming regular refresh)
- The triplication in the Global Configuration registers seems to be efficient
- Configuration registers must be continuously refreshed at recommended rate for Inner layers ~1Hz

	Pixel Config. cross-section (cm²) STD: single latch TMR: without correction	**Global Reg. cross-section (cm²)** TMR with correction and skewed clocks
Calculation for 200 MeV proton based on heavy ion testing (F. Faccio, CERN)	**STD: $8.63\ 10^{-15}$**	**$7.86\ 10^{-17}$**
Experimental from 480 MeV proton test	**STD: ~$1.2\ 10^{-14}$** **TMR: 1-5 10^{-16}**	**$3.57\ 10^{-17}$**

Summary

- The readout chips for the ATLAS and CMS HL-LHC pixel detectors are being developed by the RD53 Collaboration
- RD53B is a configurable design in CMOS 65nm technology implementing **the same chip** in **two versions** having different sizes and different analog Front-ends
- RD53B-ATLAS (ITkPixV1) was submitted in March 2020. A bug in the ToT memory did not prevent its characterization, apart from some system tests
- A patched chip (ITkPixV1.1) was submitted to solve the high current issue. It will be used for ATLAS ITk pre-production and majority of system testing with sensor assemblies
- All measurements up to now indicate that the chip is generally working fine, with few other minor bugs that have been fixed for next submissions. X-ray irradiations are ongoing.
- RD53B-CMS (CROCv1) will be submitted in March 2021. In addition to fixes for all known bugs, it also contains some additional features to improve calibration, monitoring and diagnostic. These will be present also in the ATLAS production chip

BACKUP

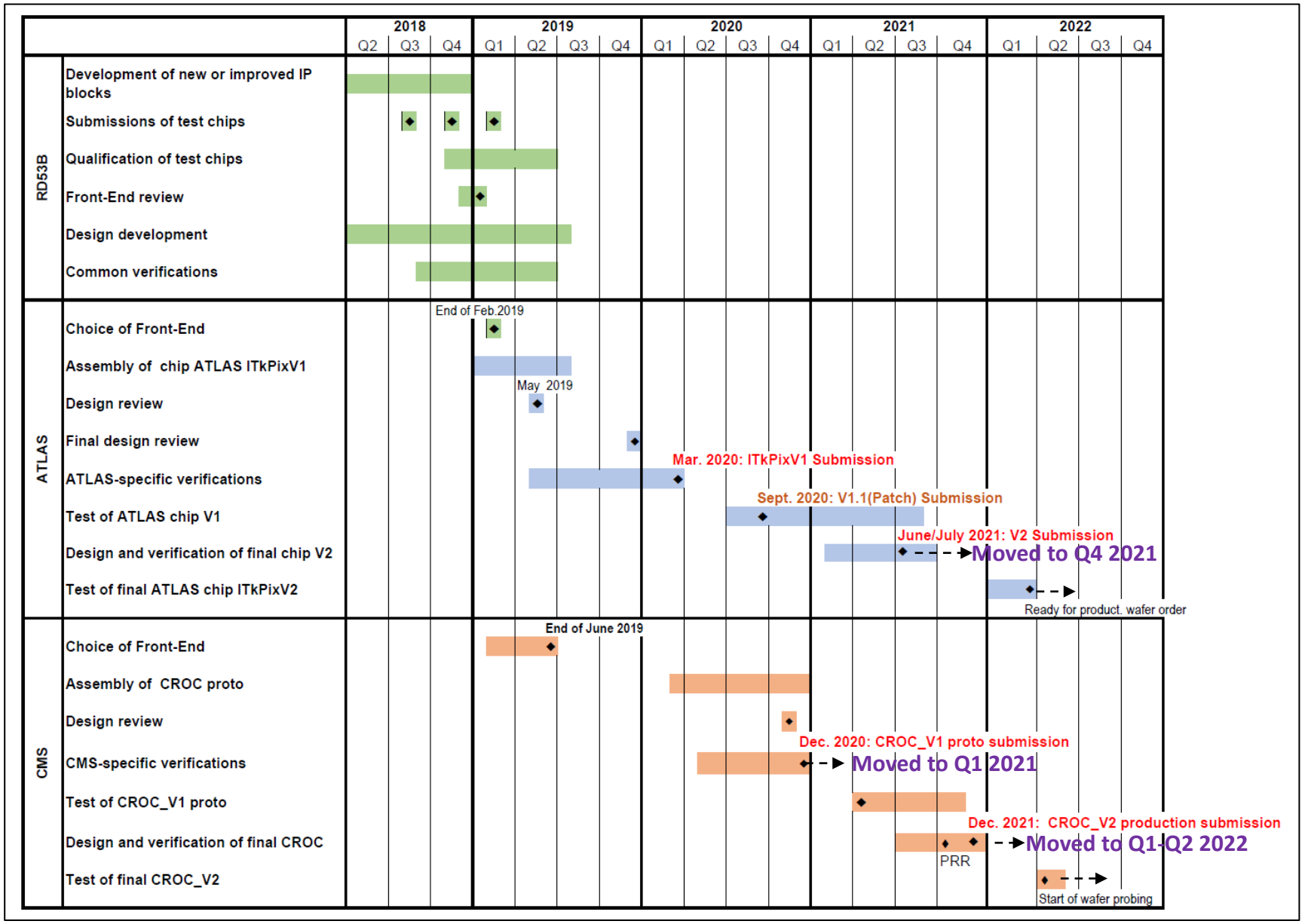
Requirement and documentation

https://cds.cern.ch/record/2663161

Technology	65nm CMOS
Pixel size	50 µm x 50 µm
ATLAS (CMS) pixel rows/columns	384 (336) / 400 (432)
Detector capacitance	< 100 fF (200fF for edge pixels)
Detector leakage	< 10 nA (20nA for edge pixels)
In-time threshold	< 1200 e-
Noise hits	$< 10^{-6}$
Hit rate	< 3 GHz/cm^2 (75 kHz avg. pixel hit rate)
Trigger rate	≤ 4 MHz (trigger only, without readout)
Trigger latency (L0)	≤ 12.5 µs (programmable)
Readout latency (L1)	≤ 25 µs
Manual readout rate	≤ 1 MHz
Hit loss (in-pixel pile-up + other sources)	≤ 2%
Charge resolution (Time over Threshold)	4 bits ToT (also 6-to-4 dual slope mapping)
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Radiation tolerance	≥ 500 Mrad, 1 10^{16} 1Mev n.eq/cm^2 (at -15°C)
SEU	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	< 1W/cm^2
Temperature range	-40°C ÷ 40°C

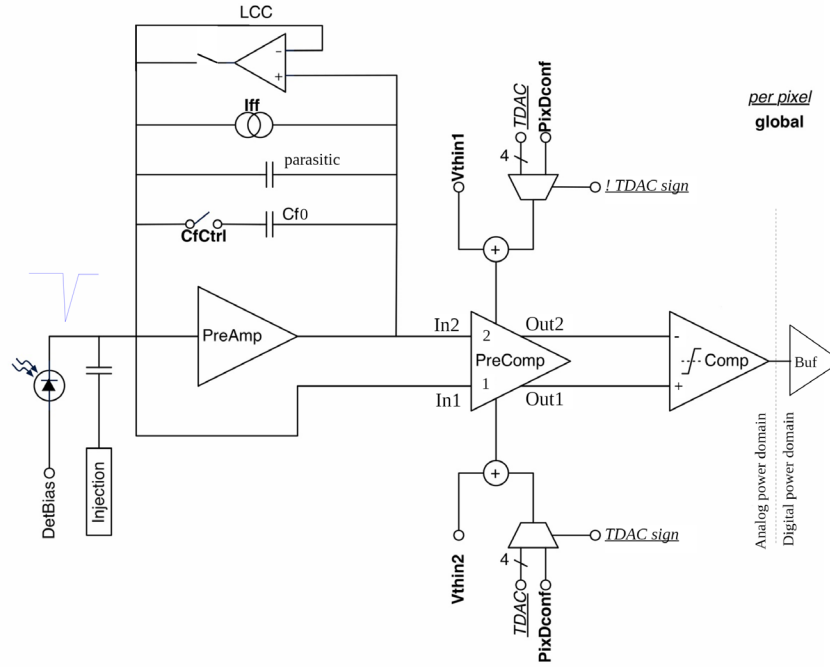
- RD53B Design manual and user guides: https://cds.cern.ch/record/2665301
- RD53B requirements: https://cds.cern.ch/record/2663161

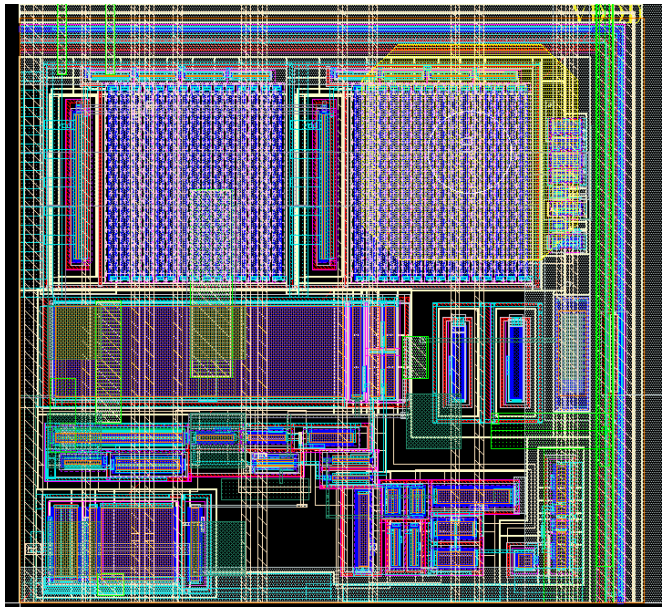
Schedule

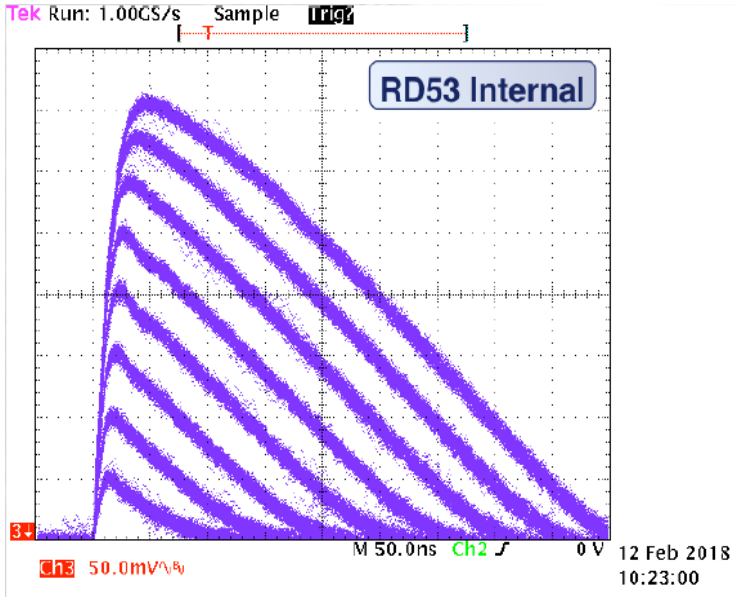


Warning: **shortage of TSMC production wafer capacity in 2021**. If this situation will persist in 2022, there is serious risk for further delay in our schedule

Differential Front-End (RD53B-ATLAS)

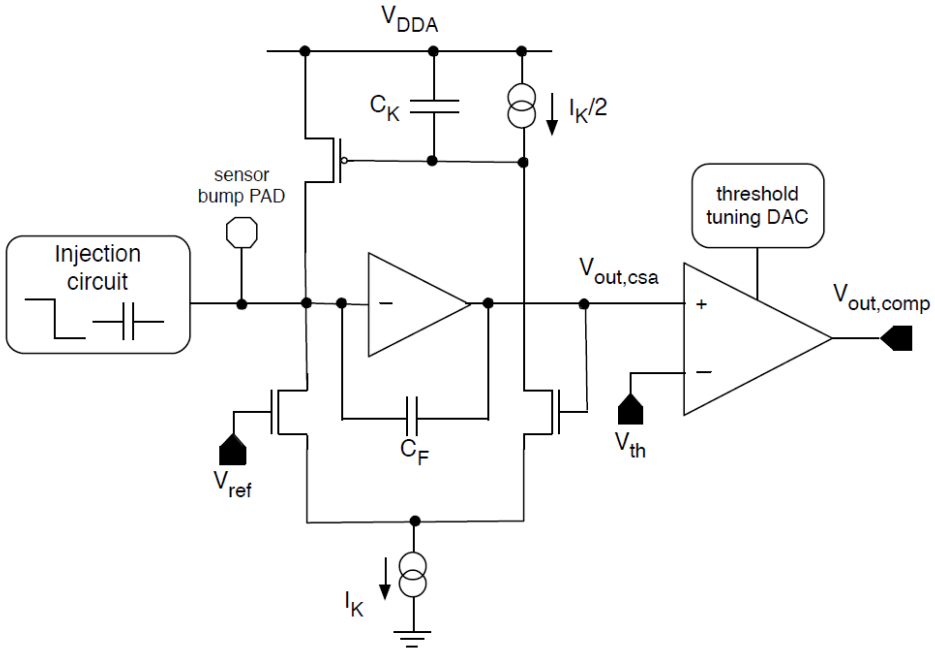


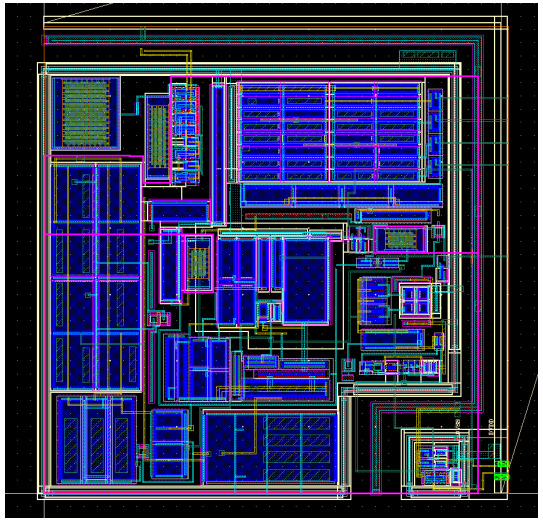


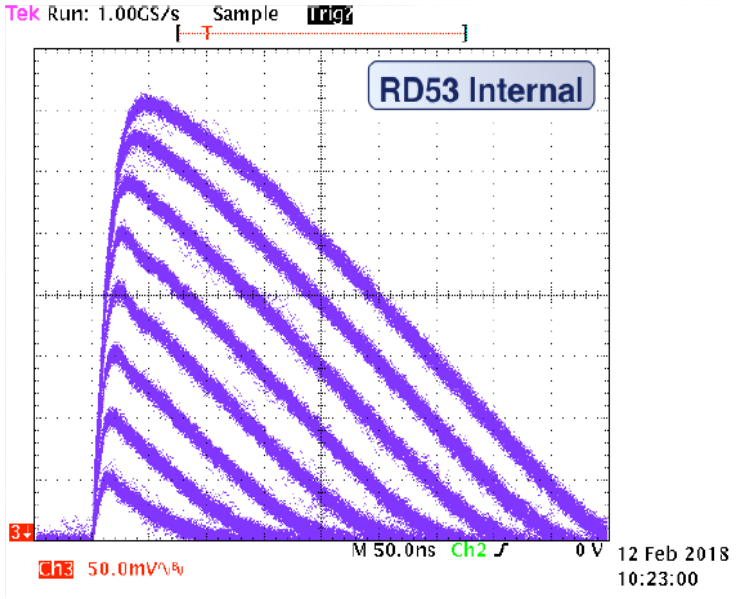


- **Charge sensitive amplifier**
- **Leakage current compensation circuit**
- **Continuous reset integrator, with tunable feedback current (global setting)**
- **DC-coupled pre-comparator stage**
  - ❖ **10-bit DAC for global threshold**
  - ❖ **4+1 bit local trimming DAC for threshold tuning**
- **Fully differential input comparator**

Linear Front-End (RD53B-CMS)







- **Charge sensitive amplifier**

•Krummenacher feedback for return to baseline and leakage current compensation

- **Comparator**
  - ❖ **10-bit DAC for global threshold**
  - ❖ **5-bit local trimming DAC for threshold tuning**

ITkPixV1 wafer probing

- Needle card
- Probe station
- Power supplies and Source meter
- Probe PC

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WAFER PROBING SETUP WN2 2021

RD53B

Power on chip in LDO Mode
Trim Iref
Trim LDO Registers
Power in shunt mode
Take regulator IV curves

Trim LDO Registers
Run Chip_ID Test
Run aurora lane test
Write Efuses
Run (pixel) register test

Measure all Ring Oscillatos
Injection cap. measurement
Measure injection DACs / ADC
Run Digital scan
Run Analog scan

Run Threshold Scan

Analog trimming and measuring
Digital testing
Injection measurements