Timespot1: A 28-nm CMOS ASIC for pixel read-out with time resolution below 20 ps.

S. Cadeddu

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Outline

• The TimeSPOT Project

• Timespot1 Architecture

• Analog Front-End (AFE)

• Time to Digital Converter (TDC)

• Readout Tree

• Board for Test and Demonstrator

• Conclusions
What is the TimeSPOT Project (TIME & SPace real-time Operating Tracker)

- Project for the development of a silicon and diamond 3D tracker with timing facilities
- financed by INFN
  - 10 Italian Institutes (INFN): Bologna, Cagliari, Genova, Ferrara, Firenze, Milano, Padova, Perugia, Torino, TIFPA
  - 60 heads, ~ 25 FTE.
  - People coming from different experiments: LHCb, ATLAS, CMS + others

- Final Target: Develop and realize a demonstrator consisting of a tracking system, with high timing resolution, integrating a thousand read-out pixels

- Some Specifications:
  - Space resolution: order 10 μm
  - Time resolution: ≤ 50 ps per pixel
  - Limited power per F/E channel (10’s of μW)

- Detector Results from Test beam with Minimum Ionizing Particles (MIP):
  - Discrete components analog Front-End readout used.
  - \( \sigma_t \) ranging from 35 ps (no TOT corrections) to ~ 20 ps (CFD)
  - Intrinsic time resolution (only sensor) estimated ~ 15 ps
Timespot1 Architecture

- 1024 channels, each equipped with Analog Front End and TDC

- A group of 256 channels is readout by a ROT (Read Out Tree) that addresses incoming data to 2 serializers that drive a LVDS driver each, sending data out @1.28 Gb/s

- There are 10 DACs giving Voltage references to the Front-End cells

- Different clock generator (PLL and DCOs) are implemented to give different clock sources for the circuit, with different jitter performances, to study the jitter influence on the time resolution

- All the chip is controlled/configured through I²C interfaces
Timespot1 Layout

- Size: 2.618 x 2.288 mm².
- Pin:
  - Total: 52
  - 8 LVDS out @1.28 Gbps
- Submitted on Oct. 2020
- Die Expected on Feb. 2021

Feb. 17, 2021
Analog Front-End

- CSA architecture consisting in an AC-coupled inverter-like core amplifier with a double feedback path.

- Small size (50 x 15 $\mu$m$^2$) to leave room for the TDC and controls
  - total pixel size: 50 x 55 $\mu$m$^2$.

- 15 ps rms jitter achievable within power constraints.

- Nominal Power Consumption < 20 $\mu$W/ch
  - ~17.5 $\mu$A CSA bias current, that becomes ~ 30 $\mu$A in High-Power regimes.
TDC

- Vernier Architecture
  - DCOs Frequency: ~ 1GHz
  - DCO's switched off after meas.
- Double measure:
  - Time of Arrival (TA) Res.: ~ 10 ps LSB
  - Time Over Thresholds (TOT) Res.: ~ 1 ns
- Max event rate: 3 MHz
- Size: 50 x 31.5 µm².
- Output: 24 bits (TA + TOT) Serial @ 160 MHz

### Power Consumption

<table>
<thead>
<tr>
<th>Mode</th>
<th>Tot Pwr (µW)</th>
</tr>
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<tbody>
<tr>
<td>IDLE</td>
<td>20.7</td>
</tr>
<tr>
<td>Calibration</td>
<td>552</td>
</tr>
<tr>
<td>DAQ 3MHz</td>
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<tbody>
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<tr>
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<td>TYP</td>
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<td>MAX</td>
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Analog Front-End Row

- 15 double rows (16x2 pixels) + 2 single rows (16 pixels): 512 pixels.
- Column content
  - 1 BandGap
  - 5 DAC sigma-delta (producing analog levels used by pixels)
  - Programmable bias cell (for power consumption)
  - bias replicas with source followers.
- Only power, controls and a reference current coming from outside.
Digital Row

- Digital row 16 x 2 TDC
- Center area used for:
  - Controls
  - Conf. registers
  - I²C Interface
- Size: 800 x 80 μm².
- TDC serial out on the left
- Right column for power and services
- Serial outs on the bottom where they are got from ROT.
ReadOut Tree (ROT)

- TDC data are deserialized and memorized inside a cache
  - two caches, data are written in the first free position
  - data are labeled with a 9-bit timestamp
  - an 8-bit address is paired with data at the ROT output

- ROT output is connected with two fifos
- the DDR block generate! a 640MHz DDR serial data that is connected with the LVDS link

- Max event rate: 200 kHz
A Board for Test and Demonstrator

- Size: 120 x 80 mm².
- Detector supply up to 200V
- PCB area below chip with less material
- Conceived for both ASIC tests and the demonstrator setup with the Detector on top
Conclusion

- We develop an ASIC in 28-nm technology for the TimeSPOT project.

- We integrate 1024 channels, each one equipped with an AFE and TDC.
- AFE jitter is below 15ps and TDC resolution is 10ps LSB (from post-layout simulation).
- Channel Power Consumption is around 40 $\mu$W.
- Each channel can sustain a max event rate up to 3 MHz.
- Data are output @ 1.28 Gbps.
- All the chip can sustain a max event rate up to 200 kHz (all channel fired), limited by data bandwidth.

- A Board was developed for both test and demonstrator.

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<td>Num. Pixels</td>
<td>Detector Resolution AFE Jitter TDC Resolution</td>
<td>AFE Consumption TDC Consumption</td>
<td>Channel Max Rate Chip Max Rate Link Data Rate Tot. Data Rate</td>
</tr>
<tr>
<td>1024</td>
<td>15 ps 15 ps 10 ps</td>
<td>&lt;20 $\mu$W &lt;25 $\mu$W</td>
<td>3 MHz 200 kHz 1.28 Gbps 10.24 Gbps</td>
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<tr>
<td>55x55$\mu$m$^2$</td>
<td>3,098 mm$^2$</td>
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