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Timespot1: A 28-nm CMOS ASIC for pixel read-out with time resolution below 20 ps.

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[1] INFN Cagliari — [2] INFN Milano — [3] INFN Torino — [4] Università di Milano, Dip. Di Fisica — [5] Politecnico di Torino
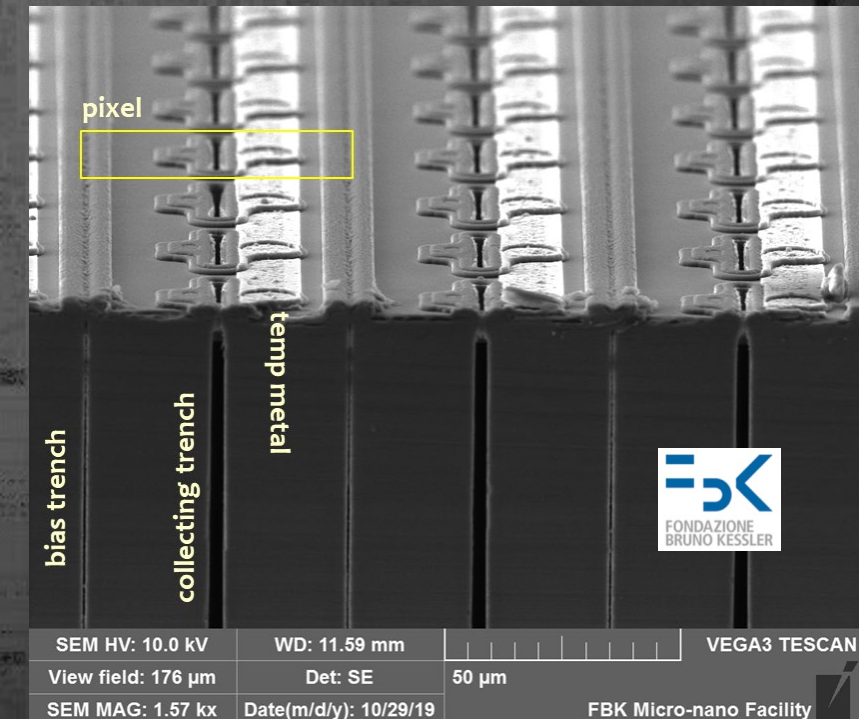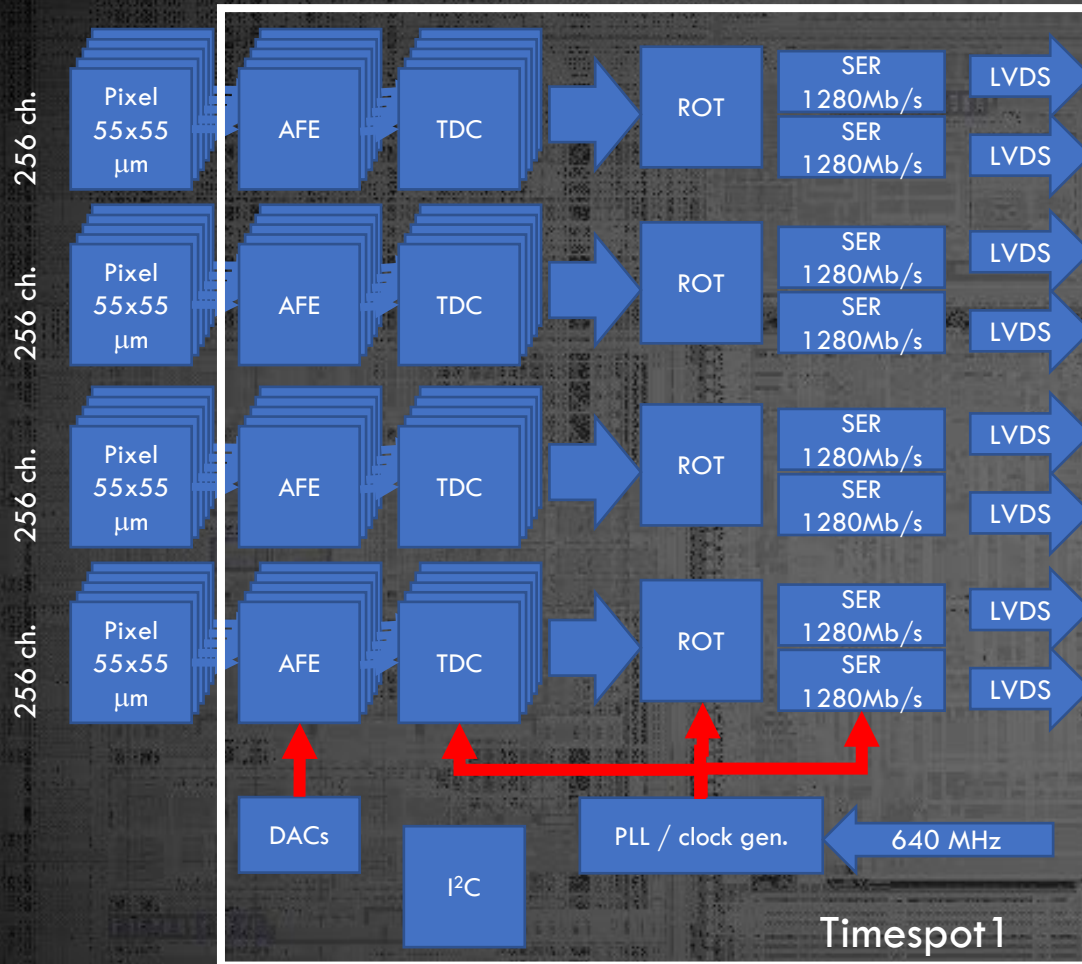
Outline

- The TimeSPOT Project

- Timespot1 Architecture

- Analog Front-End (AFE)

- Time to Digital Converter (TDC)

- Readout Tree

- Board for Test and Demonstrator

- Conclusions

What is the TimeSPOT Project (TIME & SPace real-time Operating Tracker)

- Project for the development of a silicon and diamond 3D tracker with timing facilities

- **financed by INFN**
  - 10 Italian Institutes (INFN) : Bologna, Cagliari, Genova, Ferrara, Firenze, Milano, Padova, Perugia, Torino, TIFPA
  - 60 heads, ~ 25 FTE.
  - People coming from different experiments: LHCb, ATLAS, CMS + others

- Final Target: Develop and realize a demonstrator consisting of a tracking system, with high timing resolution, integrating a thousand read-out pixels

- Some Specifications:
  - Space resolution: order 10 μm
  - Time resolution: ≤ 50 ps per pixel
  - Limited power per F/E channel (10's of μW)

- Detector Results from Test beam with Minimum Ionizing Particles (MIP):
  - Discrete components analog Front-End readout used.
  - σ_t ranging from 35 ps (no TOT corrections) to ~ 20 ps (CFD)
  - Intrinsic time resolution (only sensor) estimated ~ 15 ps

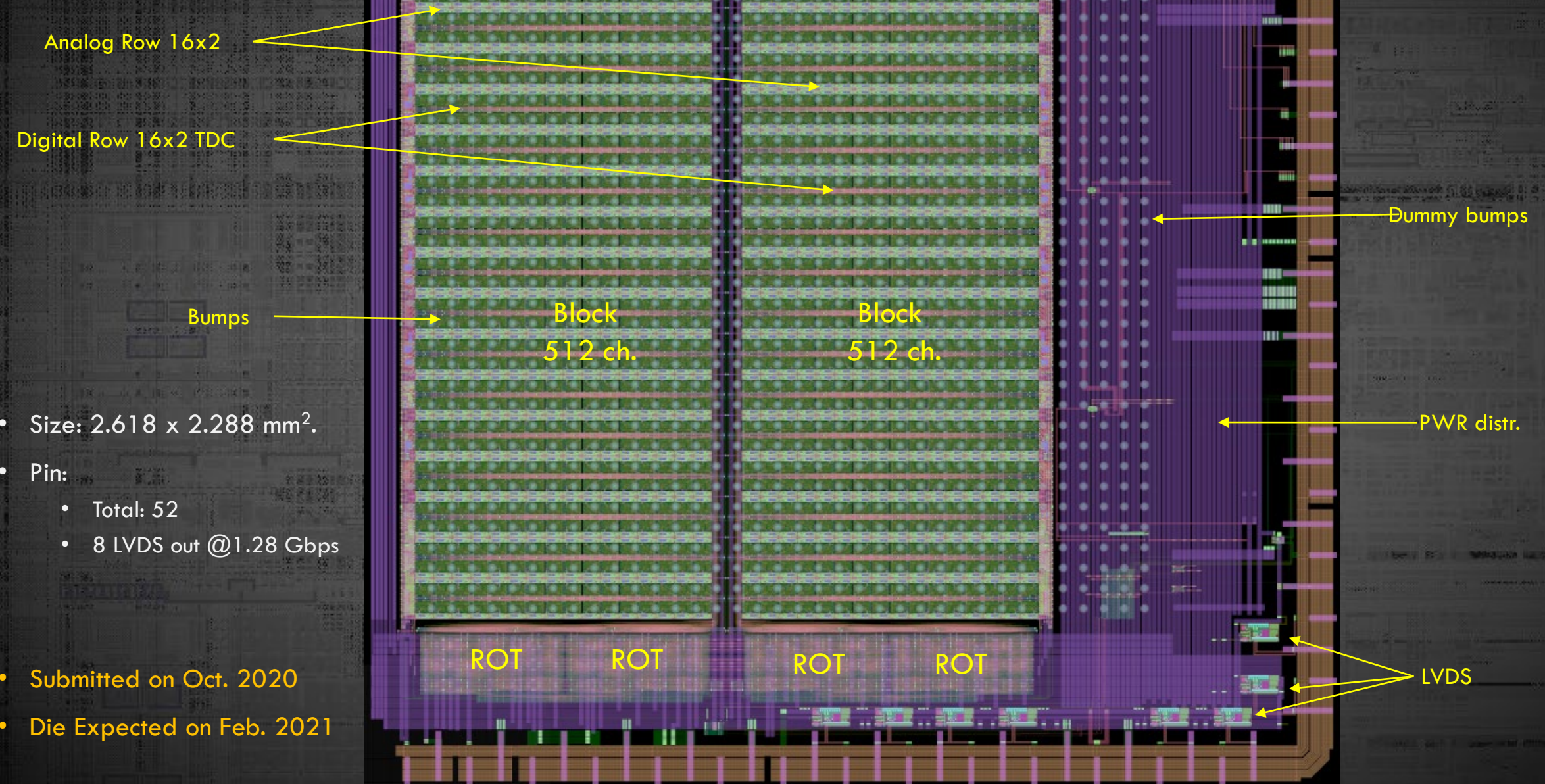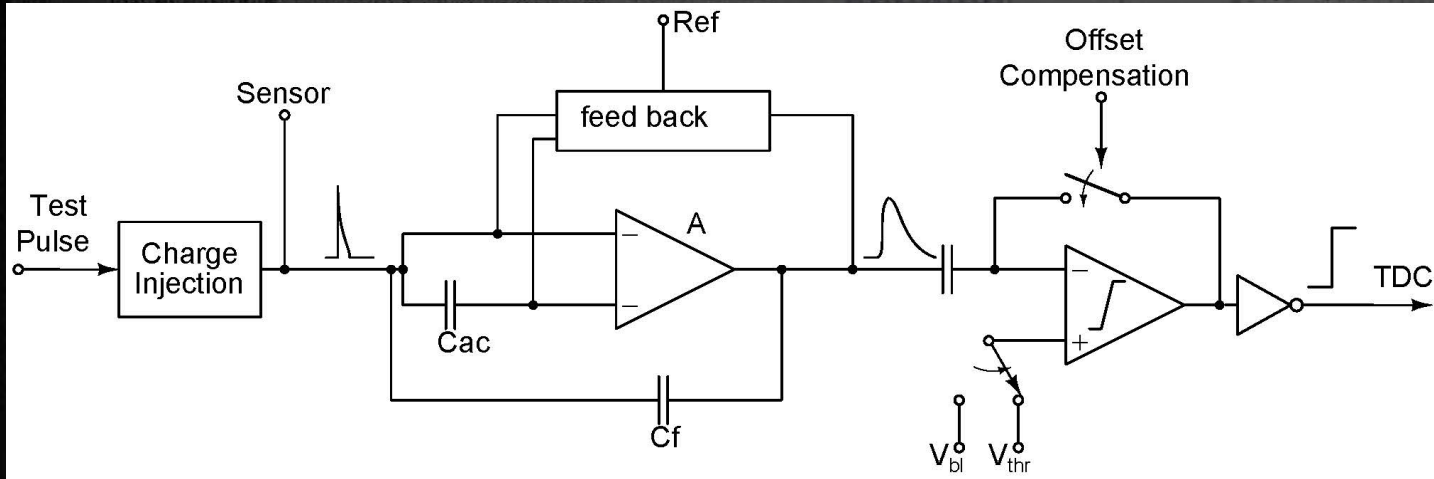| SEM HV: 10.0 kV	WD: 11.59 mm		VEGA3 TESCAN
View field: 176 μm	Det: SE	50 μm	
SEM MAG: 1.57 kx	Date(m/d/y): 10/29/19		FBK Micro-nano Facility

Timespot1 Architecture

- 1024 channels, each equipped with Analog Front End and TDC

- A group of 256 channels is readout by a ROT (Read Out Tree) that addresses incoming data to 2 serializers that drive a LVDS driver each, sending data out @1.28 Gb/s

- There are 10 DACs giving Voltage references to the Front-End cells

- Different clock generator (PLL and DCOs) are implemented to give different clock sources for the circuit, with different jitter performances, to study the jitter influence on the time resolution

- All the chip is controlled/configured through I^2C interfaces
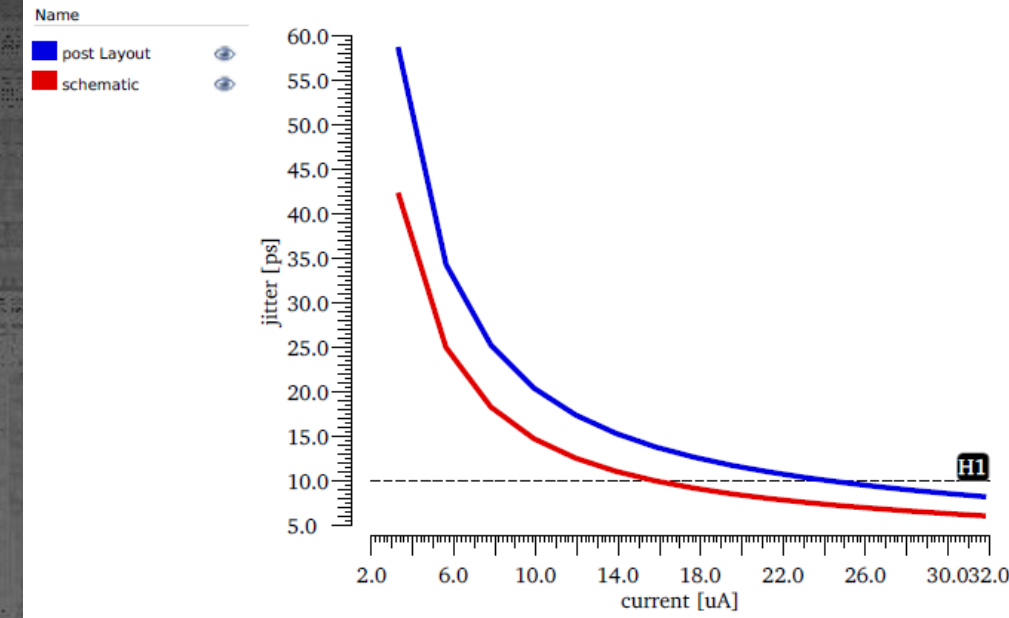
Timespot1 Layout

Analog Row 16x2

Digital Row 16x2 TDC

Bumps

Block 512 ch.

Block 512 ch.

Dummy bumps

PWR distr.

ROT   ROT   ROT   ROT

LVDS

- Size: 2.618 x 2.288 mm^2.
- Pin:
  - Total: 52
  - 8 LVDS out @1.28 Gbps

- Submitted on Oct. 2020
- Die Expected on Feb. 2021

Simulated Jitter vs Bias Current

- CSA architecture consisting in an AC-coupled inverter-like core amplifier with a double feedback path.

- Small size (50 x 15 µm^2) to leave room for the TDC and controls
  - total pixel size: 50 x 55 µm^2.

- 15 ps rms jitter achievable within power constraints.

- Nominal Power Consumption < 20 µW/ch
  - ~17.5 µA CSA bias current, that becomes ~ 30 µA in High-Power regimes.

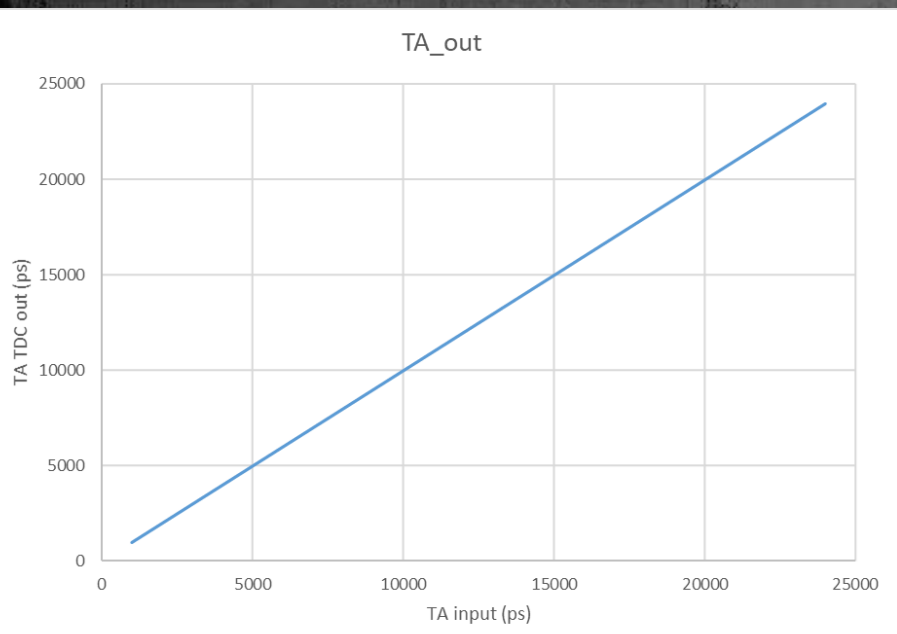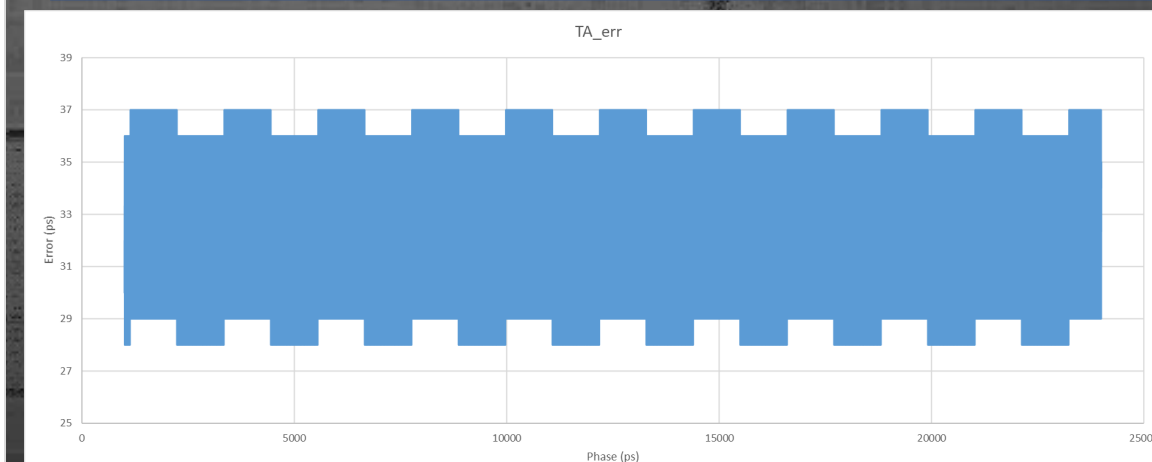| simulation	schematic		layout	
power regime	nominal	High	nominal	High
Slew-Rate [mV/ns]	380	540	250	360
rms noise [mV]	5.0	4.9	3.9	3.8
jitter [ps]	13.2	9.1	15.6	10.5
power/channel [µW]	18.2	31.5	18.6	32.9

Full matrix simulation

TDC

- Vernier Architecture
  - DCOs Frequency: ~ 1GHz
  - DCO's switched off after meas.

- Double measure:
  - Time of Arrival (TA) Res.: ~ **10 ps LSB**
  - Time Over Thresholds (TOT) Res.: ~ **1ns**

- Max event rate: 3 MHz

- Size: 50 x 31.5 μm^2.

- Output: 24 bits (TA + TOT) Serial @ 160MHz

TDC (50 x 31.5 μm^2)

TA_out

Corner	DCO Period	RES High		RES Mid-High		RES Mid-Low		RES Low	
		LSB	RMS	LSB	RMS	LSB	RMS	LSB	RMS
MIN	637 ps	6 ps	1,71 ps	18	5,21	25	7,50	69	20,14
TYP	1105 ps	9 ps	2,87 ps	20	6,05	31	9,23	42	12,37
MAX	1210 ps	12 ps	4,00 ps	30	9,19	30	9,19	50	14,65

TA_err

Power Consumption

|	Tot Pwr (uW)
IDLE	20.7
Calibration	552
DAQ 3MHz	175
DAQ 1MHz	69.3
DAQ 500kHz	45.5
DAQ 100kHz	25.7

Analog Front-End Row

Analog Pixels Double Row 16x2 (800 x 30 μm^2)
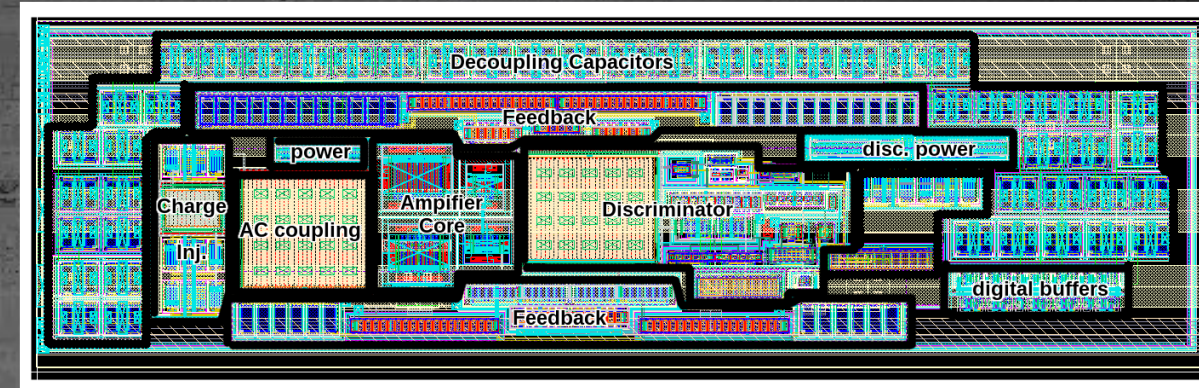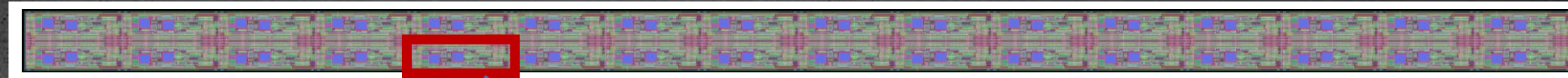
Analog Pixel (50 x 15 μm^2)

- 15 double rows (16x2 pixels) + 2 single rows (16 pixels): 512 pixels.

- Column content
  - 1 BandGap
  - 5 DAC sigma-delta (producing analog levels used by pixels)
  - Programmable bias cell (for power consumption)
  - bias replicas with source followers.

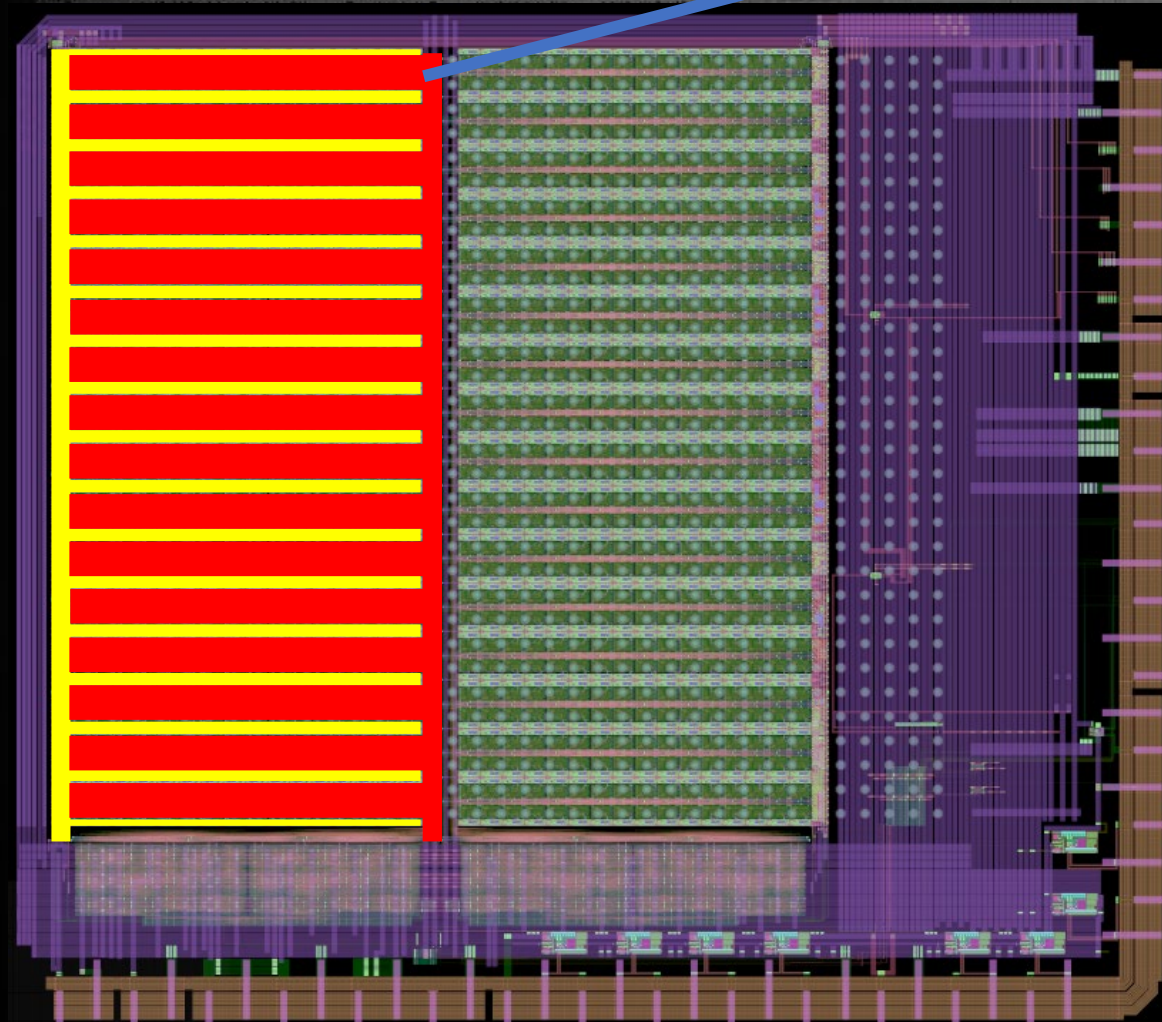- Only power, controls and a reference current coming from outside.
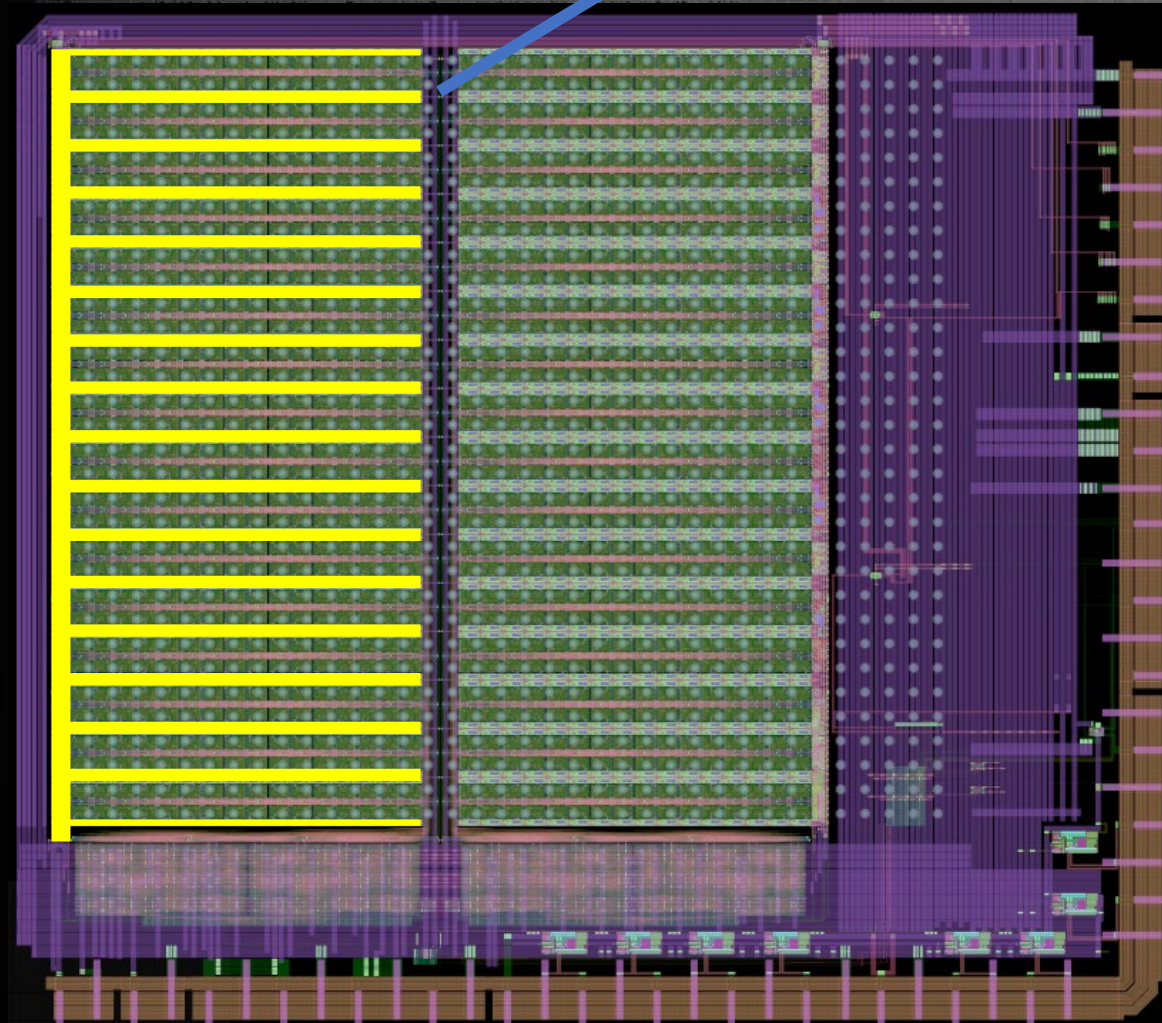
Digital Row
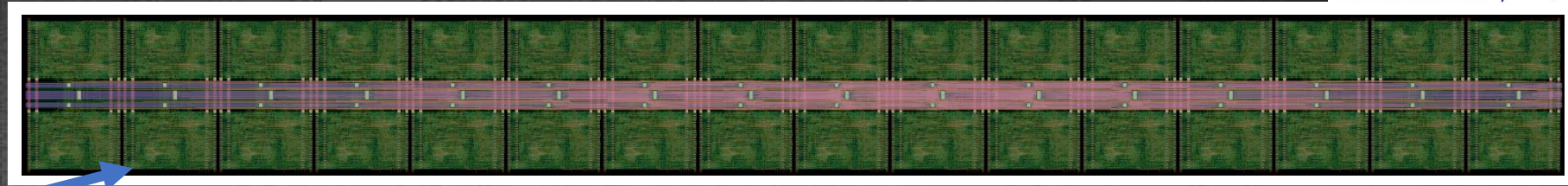
Digital Row 16x2 (800 x 80 μm^2)

- Digital row 16 x 2 TDC

- Center area used for:
  - Controls
  - Conf. registers
  - I^{2}C Interface

- Size: 800 x 80 μm^2.

- TDC serial out on the left

- Right column for power and services

- Serial outs on the bottom where they are got from ROT.

- TDC data are deserialized and memorized inside a cache
  - two caches, data are written in the first free position
  - data are labeled with a 9-bit timestamp
  - an 8-bit address is paired with data at the ROT output

- ROT output is connected with two fifos

- the DDR block generate a 640MHz DDR serial data that is connected with the LVDS link

- Max event rate: 200 kHz
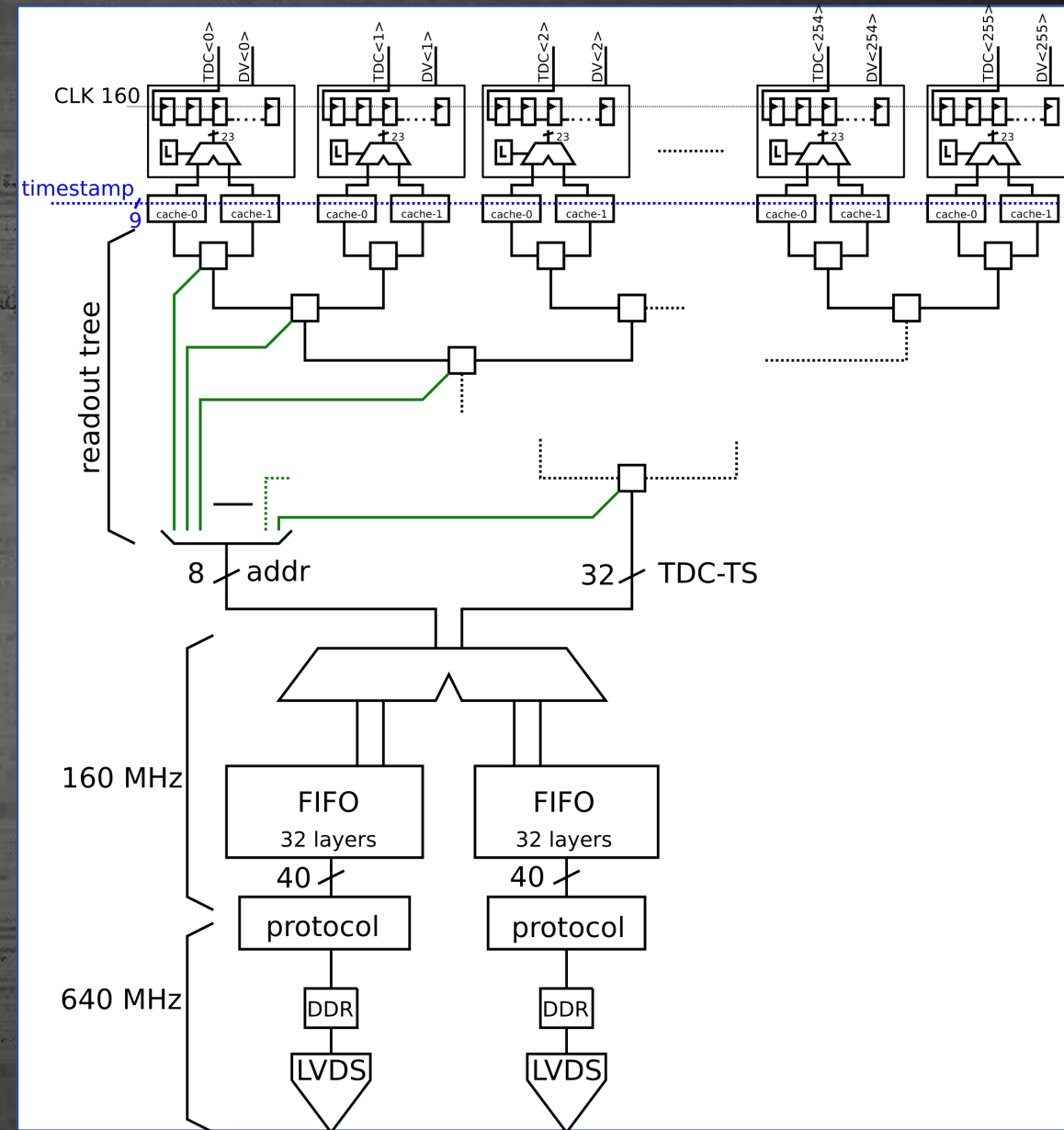
A Board for Test and Demonstrator

- Size: 120 x 80 mm^2.

- Detector supply up to 200V

- PCB area below chip with less material

- Conceived for both ASIC tests and the demonstrator setup with the Detector on top
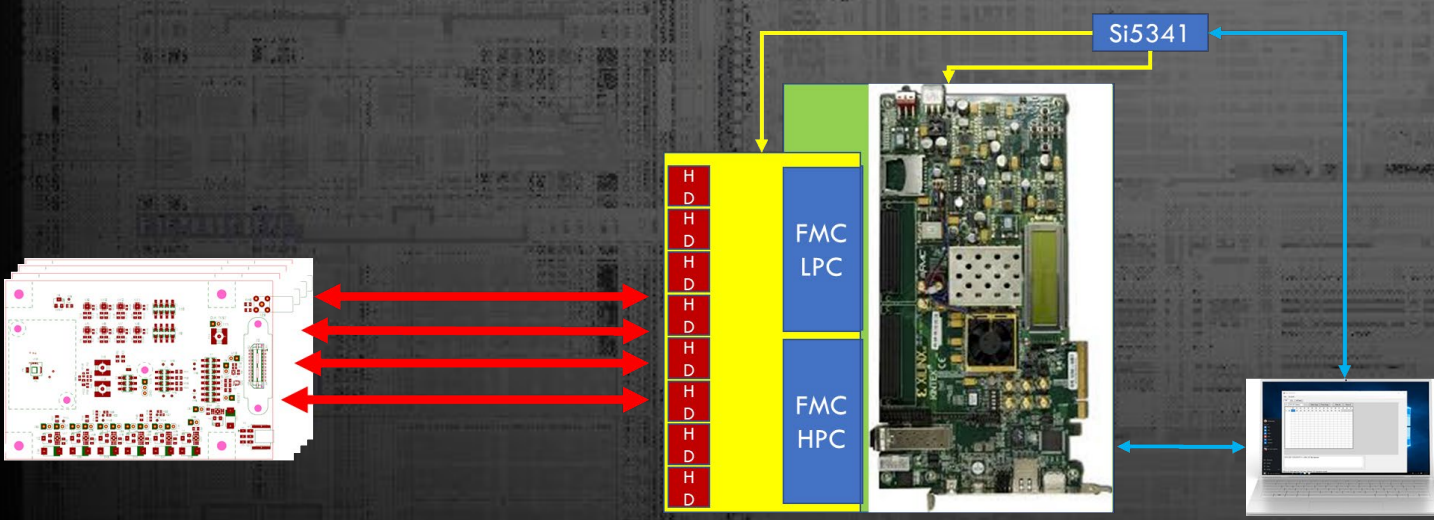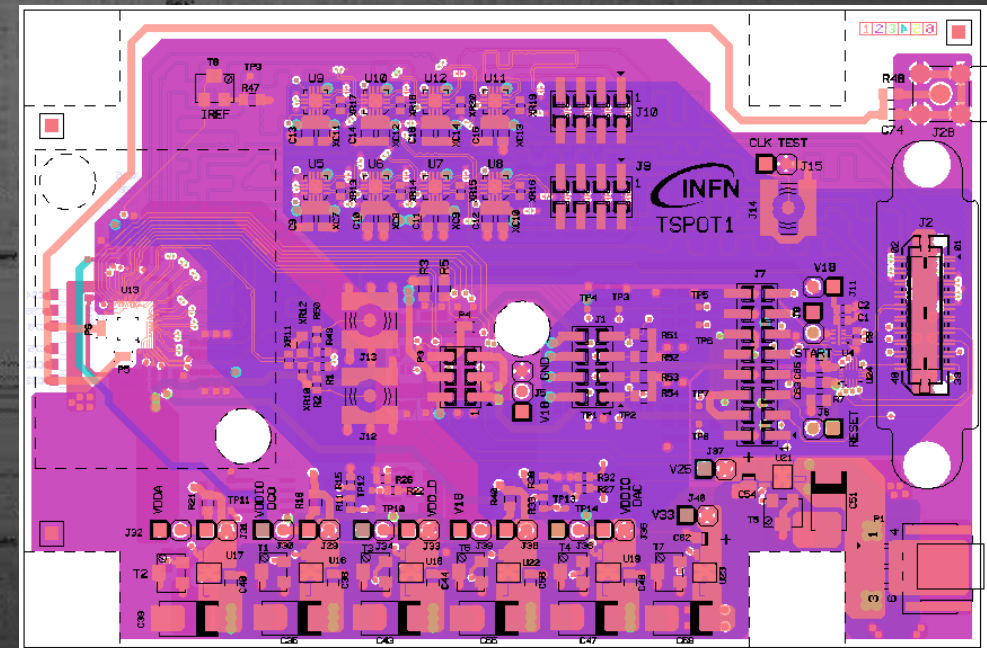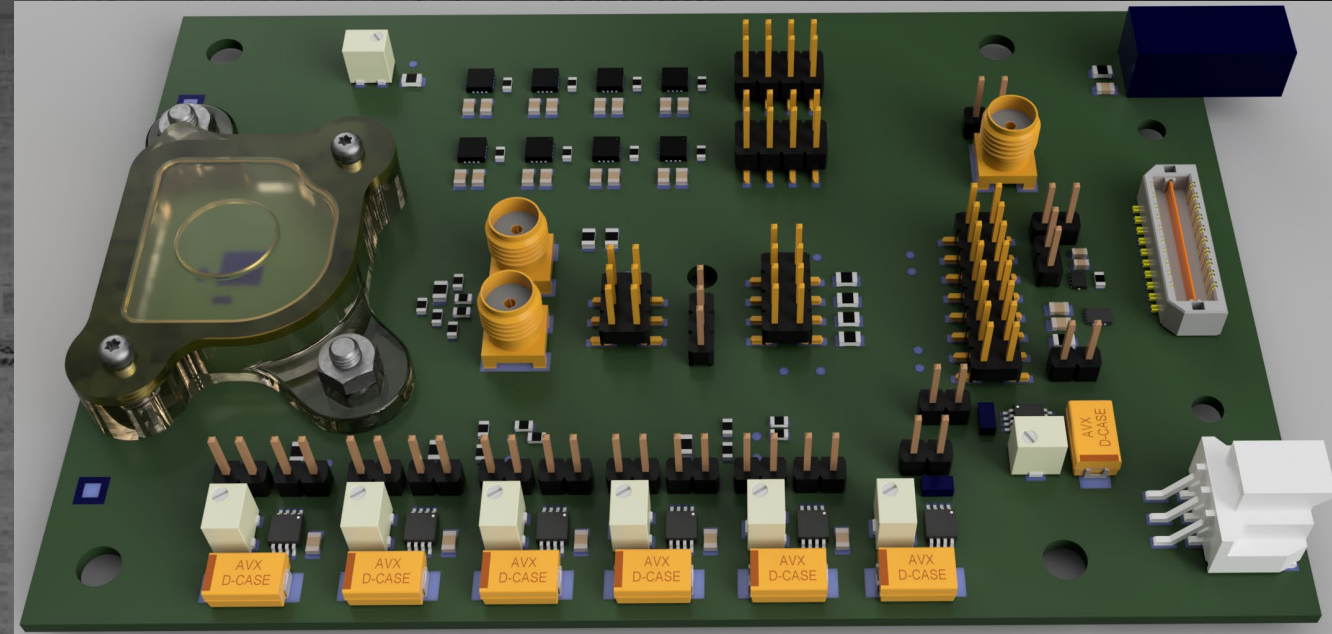
Conclusion

- We develop an ASIC in 28-nm technology for the TimeSPOT project

- We integrate 1024 channels, each one equipped with an AFE and TDC.

- AFE jitter is below 15ps and TDC resolution is 10ps LSB (from post-layout simulation)

- Channel Power Consumption is around 40 μW

- Each channel can sustain a max event rate up to 3 MHz

- Data are output @ 1.28 Gbps

- All the chip can sustain a max event rate up to 200 kHz (all channel fired), limited by data bandwidth

- A Board was developed for both test and demonstrator.

Geometry

Num. Pixels	Pixel Area	Sensible Area
1024	55x55μm².	3,098 mm²

Timing

Detector Resolution	AFE Jitter	TDC Resolution
15 ps	15 ps	10 ps

Power

AFE Consumption	TDC Consumption
<20 μW	<25 μW

Data Rate

Channel Max Rate	Chip Max Rate	Link Data Rate	Tot. Data Rate
3 MHz	200 kHz	1.28 Gbps	10.24 Gbps

TDC

DCO Arch.
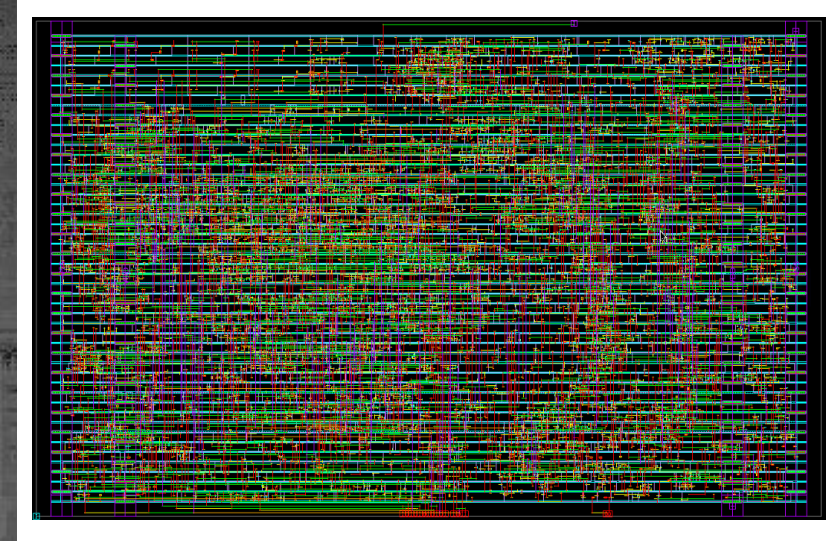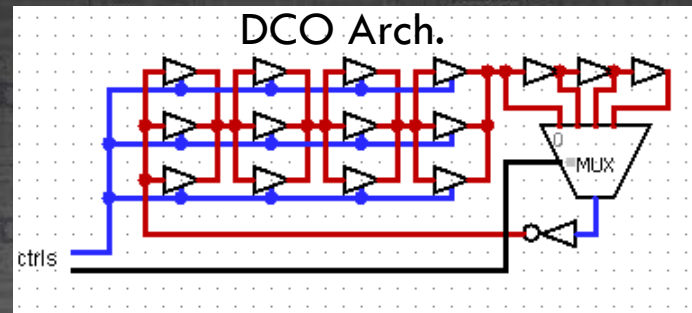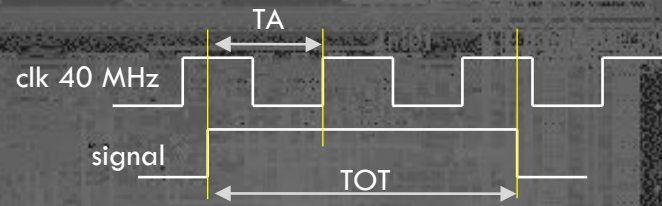
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TDC (50 x 31.5 μm^2)

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