Contribution ID: **152** Type: **Oral**

Timespot1: A 28-nm CMOS ASIC for pixel read-out with time resolution below 20 ps

Wednesday 17 February 2021 14:40 (20 minutes)

We present a prototype ASIC solution for vertex detectors of the next generation of colliders, where high resolution in both space and time measurements will be mandatory requirements in order to cope with the huge number of tracks per event to be detected and processed. The ASIC, named Timespot1, designed in CMOS 28-nm technology and featuring a 32x32 pixel matrix with a 55 μm pitch, is conceived as the first prototype in a series, capable to read-out pixels with timing capabilities in the range of 30 ps and below. Each pixel is endowed with a charge amplifier, a discriminator and a Time-to-Digital-Converter, capable of time resolutions below 20 ps and read-out rates (per pixel) around 3 MHz. The timing performance are obtained respecting a power budget of about 50 μW per pixel, corresponding to a power density of approximately 2 W/cm2. The ASIC has been submitted for production in December 2020 and the dies are expected to arrive soon. Along with the ASIC characteristics and performance, obtained from post-layout simulations, we present an overview of the demonstrator presently under development to test the system in a small real environment.

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Session Classification: Session 7: Electronics

Track Classification: Electronics