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Advanced Silicon Radiation Detectors
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Optimization of the 65 nm CMOS Linear front-end circuit for the CMS pixel readout at the HL-LHC

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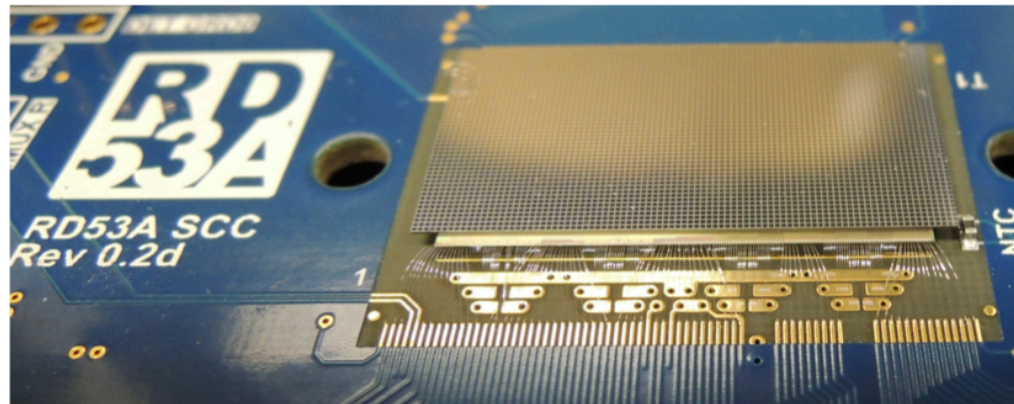
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^dINFN Pavia, ^eINFN Torino



RD53 - An overview

- Collaboration among **ATLAS** & **CMS** communities aiming at the development of large scale pixel chips for LHC phase-2 upgrades
- **65 nm CMOS** is the common technology platform

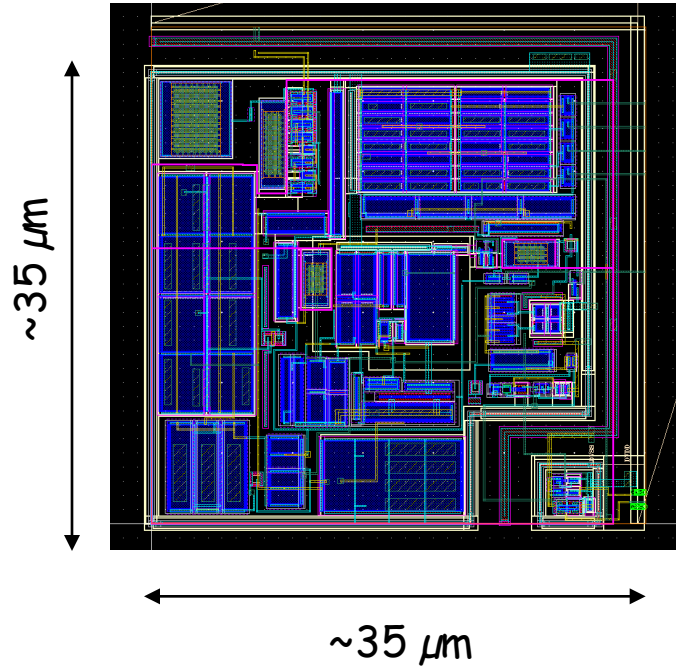
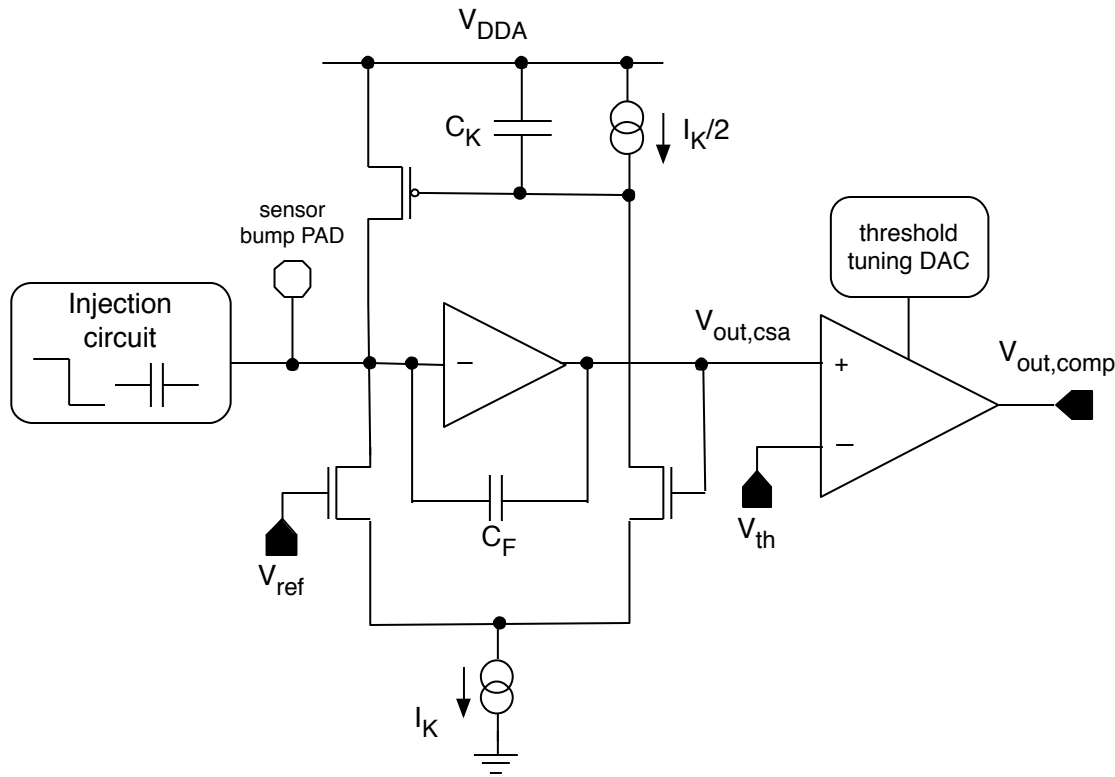


- The efforts of the RD53 collaboration led to the submission (2017) of the **RD53A chip**
- 20x11.5 mm² chip featuring a matrix of **400x192 pixels** (50x50 μm² each)
- It contains design variations for testing purposes: **3 different front-ends** (Synchronous, Linear and Differential)
- **Comprehensive characterization** of the FEs and **FE reviews** in view of the integration of final chips

- The **success of RD53A** is the baseline for the design of the pixel readout chips of *CMS* and *ATLAS* at the HL-LHC
- **RD53B** is the common design framework for the design of the final production pixel chips for *ATLAS* and *CMS*
- After a very detailed review process, a choice was made by the experiments for the analog FEs:
 - *CMS* → **Linear front-end**
 - *ATLAS* → **Differential front-end**
- **Improvements of FEs** according to reviewers' comments and to experiments requirements



RD53A Linear front-end



- **Single stage front-end with Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- Low power asynchronous **current comparator** combined with a **40 MHz Time-over-Threshold (ToT) counter** for digitization of the signal
- **4-bit local DAC for threshold tuning**

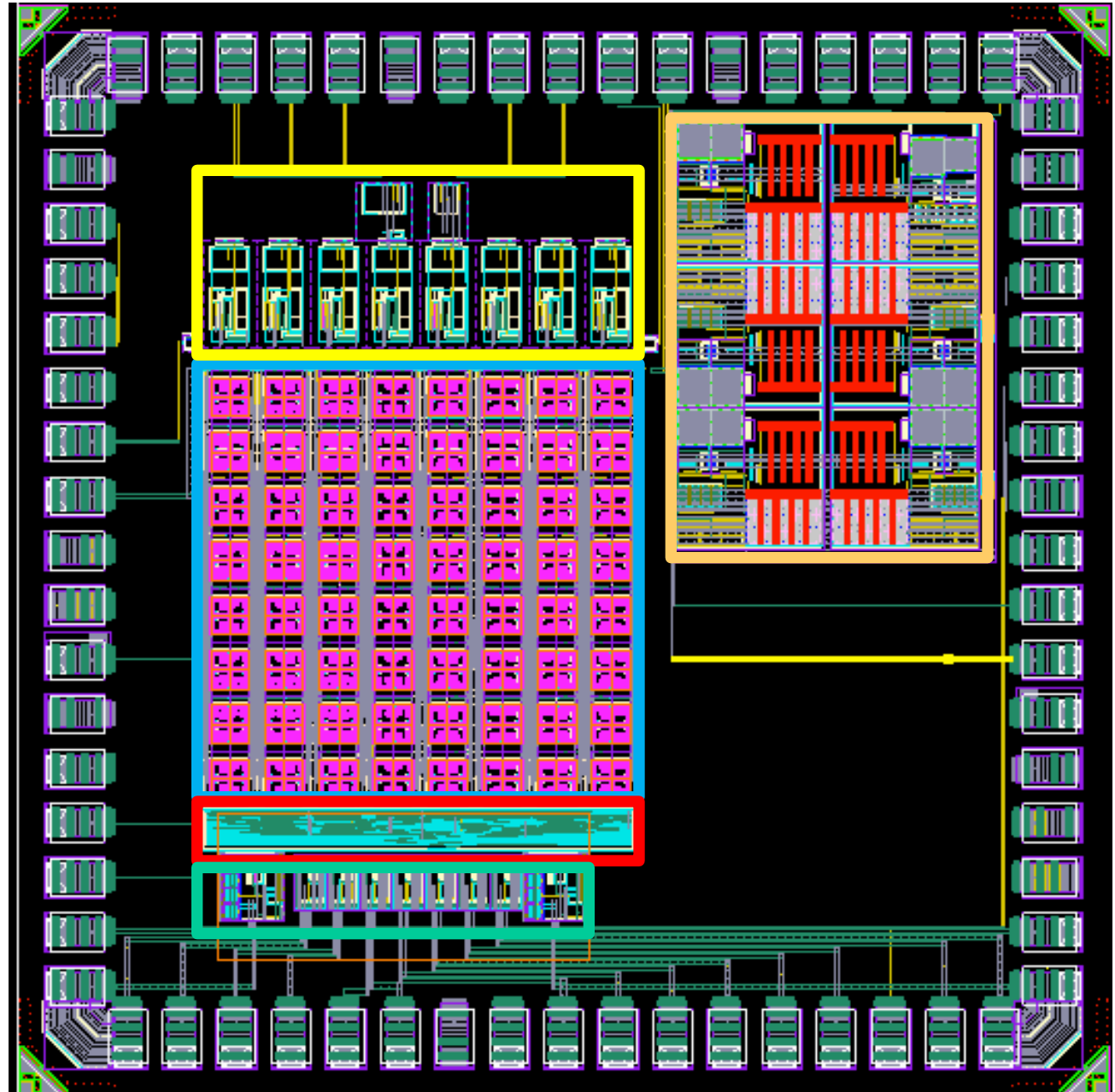
Linear front-end optimization

- ❗ **Two main improvements** implemented in RD53B Linear front-end:
 - Optimization of the threshold tuning DAC
 - Time-walk performance
- **Prototype chip** with RD53A/B versions of the Linear front-end has been submitted and tested

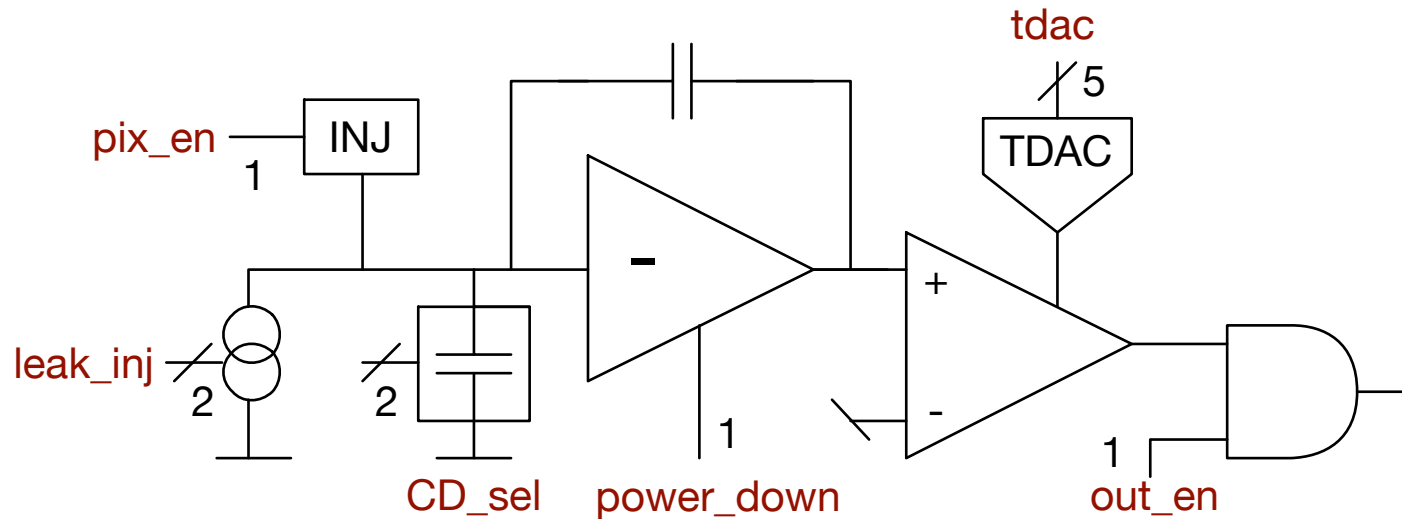
Prototype chip

- 16x16 pixel matrix
 - Two regions: RD53A - RD53B
- Analog bias
- Configuration block
 - SPI-based
- Custom LVDS TX/RX
- Bandgap test structures

Top metal layers not shown

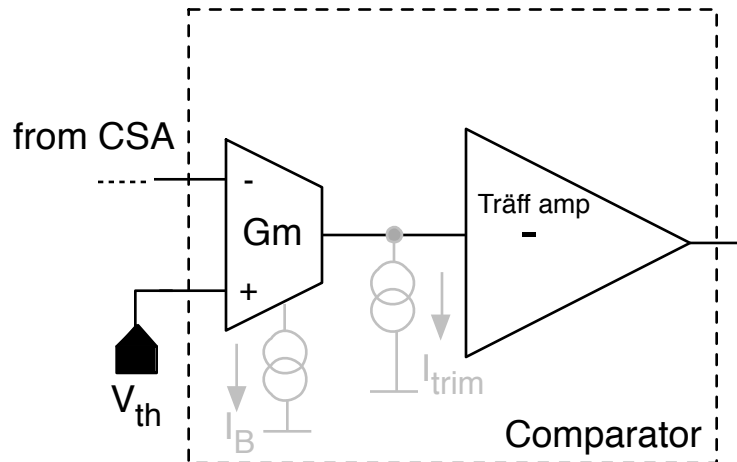
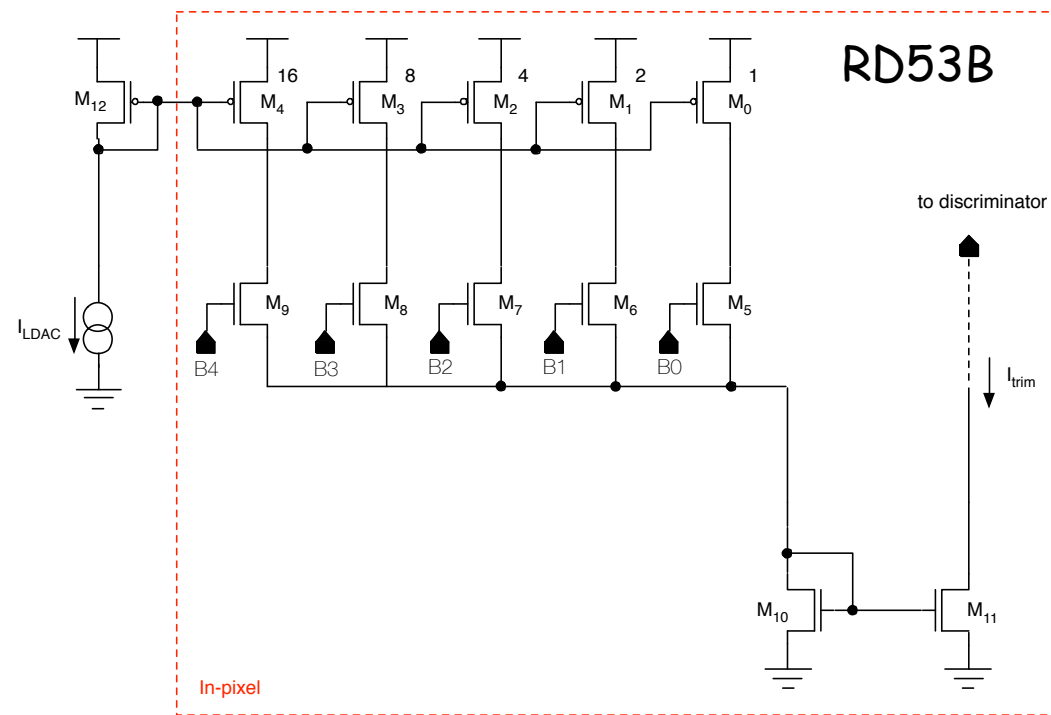
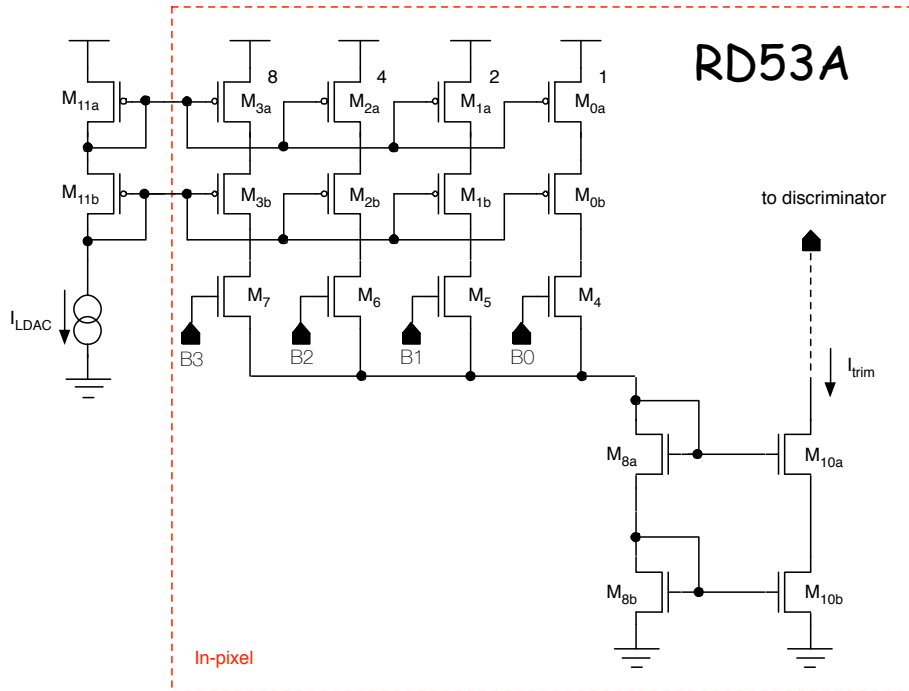


Pixel block diagram



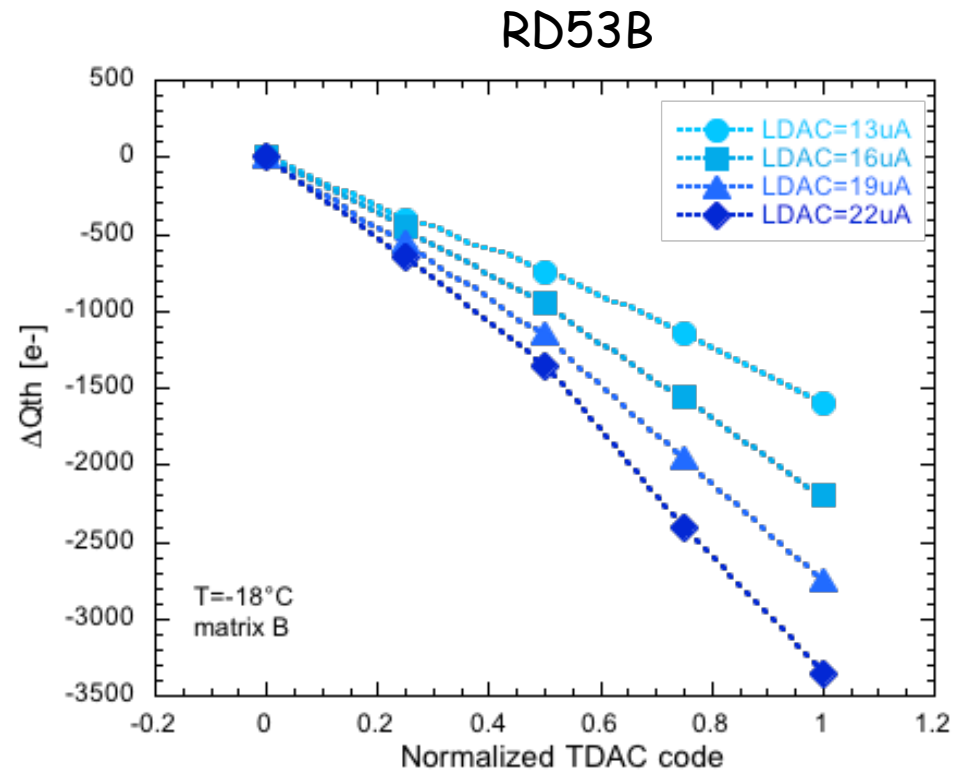
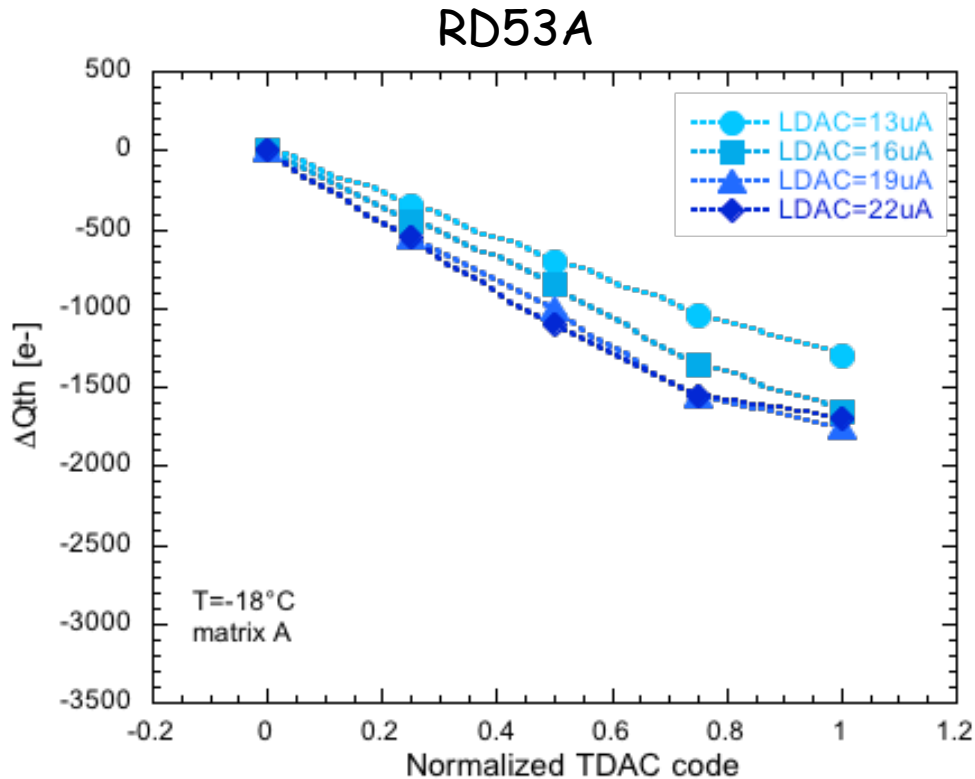
- **2 detector emulating capacitors:** 50 fF and 100 fF
→ $CD = 0, 50 \text{ fF}, 100 \text{ fF}, 150 \text{ fF}$
- **Leakage injection circuit** (possibility to inject "positive" or "negative" currents)

Threshold tuning DACs



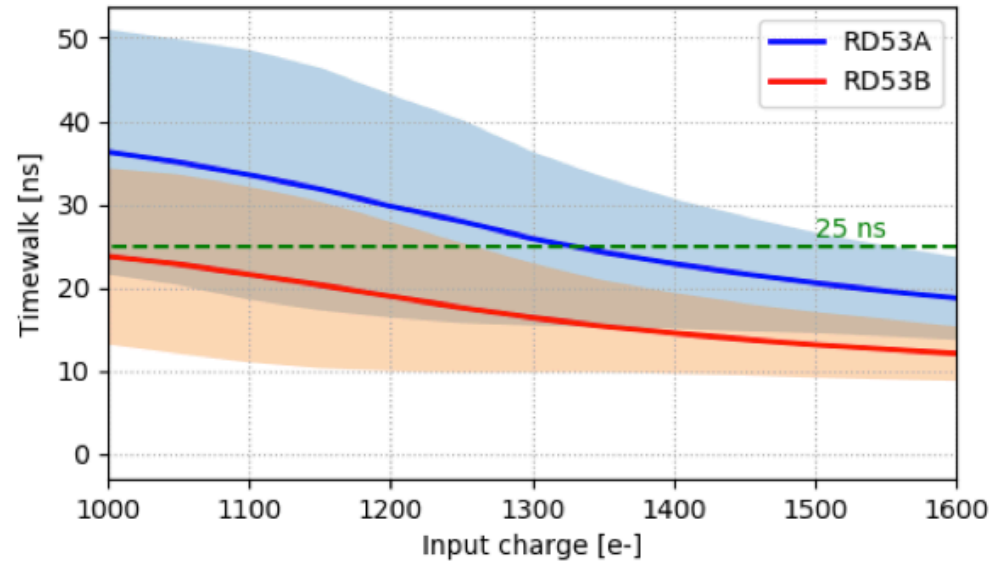
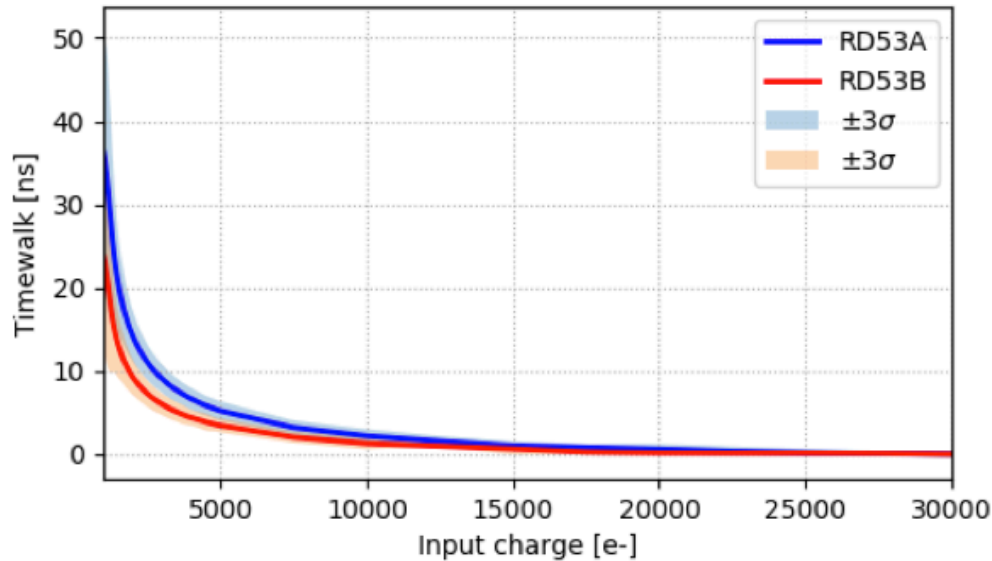
- Current-mode threshold tuning DACs
 - RD53A → 4 bits, **cascoded** current mirrors
 - RD53B → 5 bits, **regular** current mirrors
- **NMOS** switches

TDAC input-output characteristics



- TDAC **dynamic range** controlled by "LDAC" current (matrix periphery)
- **Saturation effect** taking place for RD53A at cold (for large I_{LDAC})
- The effect is **fixed** in the RD53B version

Time-walk test results



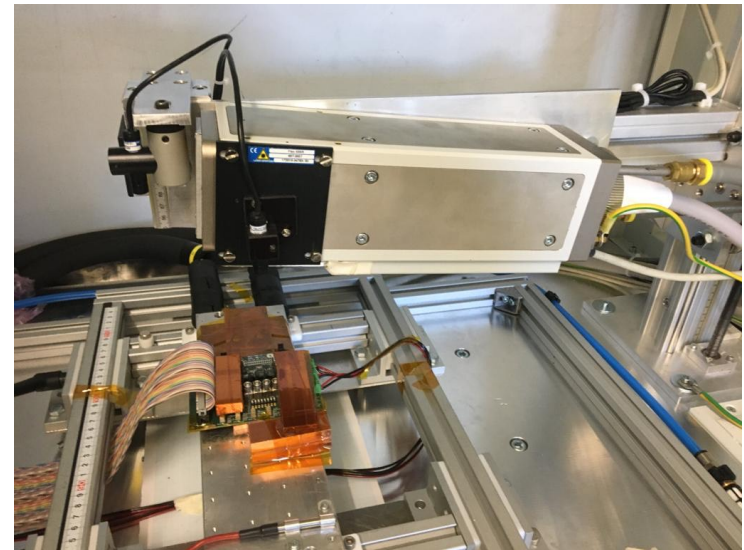
- Results on a sample chip at $T = -20^\circ \text{C}$
- Threshold $\sim 1000 \text{ e-}$, $5 \mu\text{A}$ per-pixel current consumption, 133 ns ToT @ $Q_{\text{in}} = 6 \text{ ke-}$, $C_D = 50 \text{ fF}$

Significant improvement in time-walk at the cost of a marginal increase ($\sim 4\%$) in static current consumption



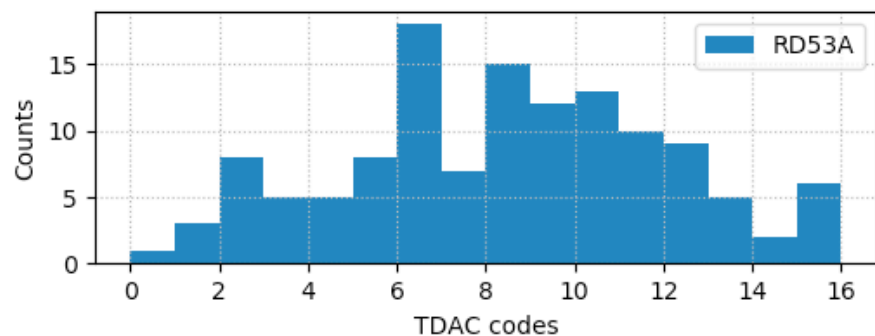
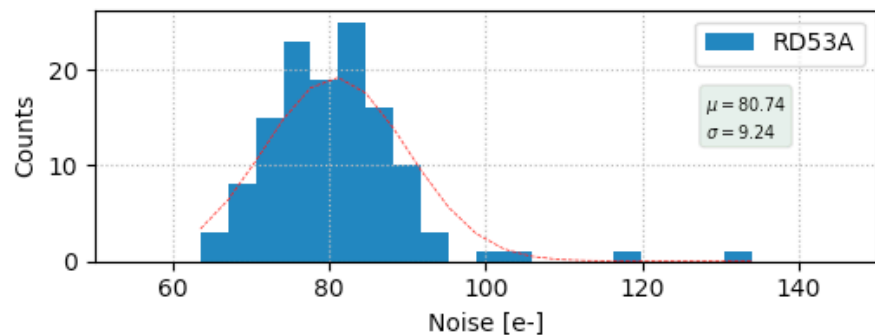
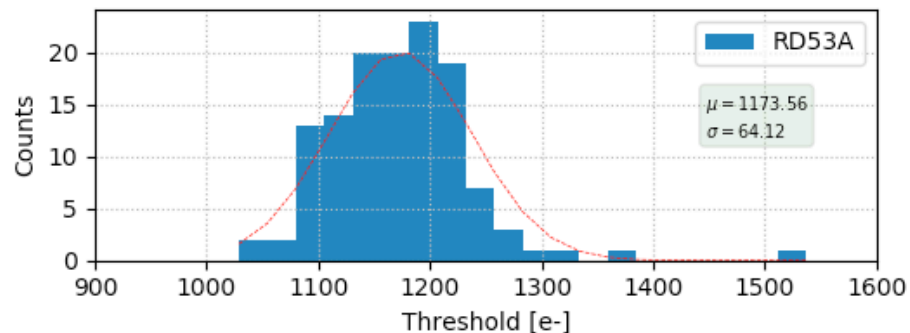
Radiation test

- Two chips have been irradiated at cold with X-rays at CERN
 - One chip with $T_{oT} \sim 133 \text{ ns}$ @ $Q_{in} 6 \text{ ke}$, $I_{LDAC} = 13 \text{ } \mu\text{A}$ (slow ToT)
 - One chip with $T_{oT} \sim 70 \text{ ns}$ @ $Q_{in} 6 \text{ ke}$, $I_{LDAC} = 19 \text{ } \mu\text{A}$ (fast ToT)
- Test conditions:
 - $T = -7^\circ \text{ C}$
 - per-pixel analog consumption $\sim 5 \text{ } \mu\text{A}$
 - $V_{DDA} = V_{DDD} = 1.2 \text{ V}$
 - $C_D = 50 \text{ fF}$
 - pre-rad $Q_{th} = 1100 \text{ e-}$
 - Bias set at room T (no changes after cooling and during irradiation)

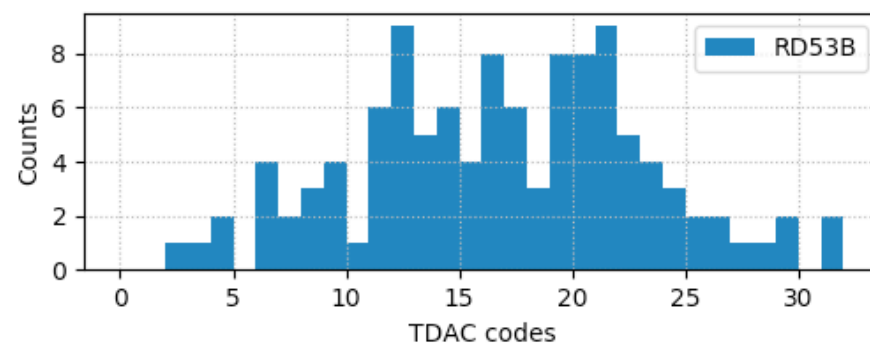
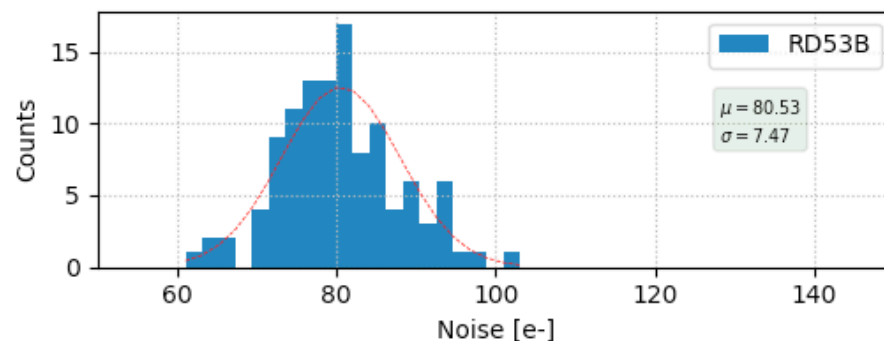
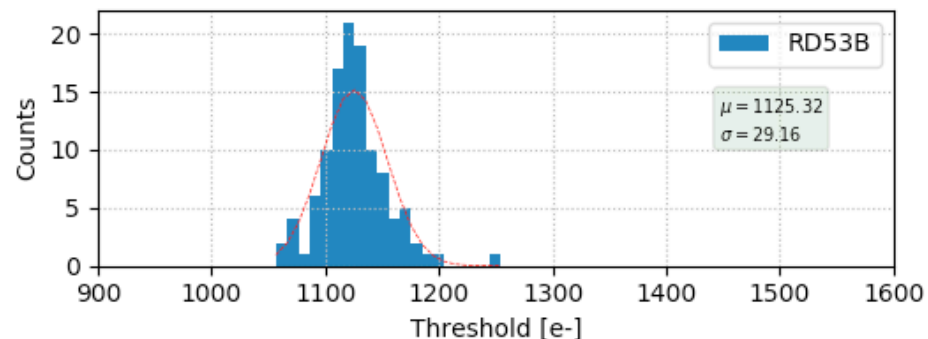


Pre-rad results: Threshold and Noise (slow ToT)

RD53A



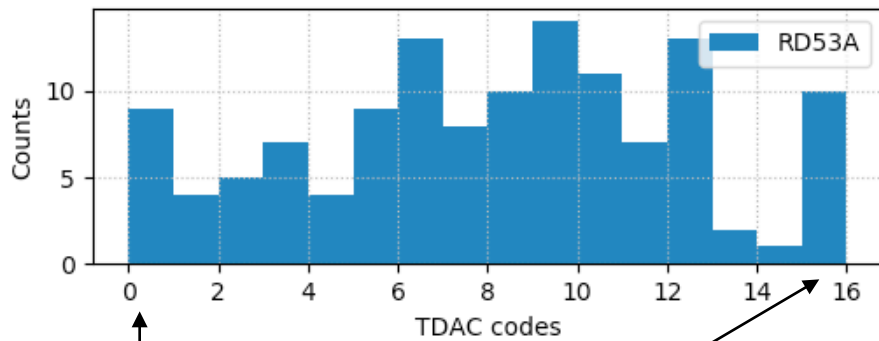
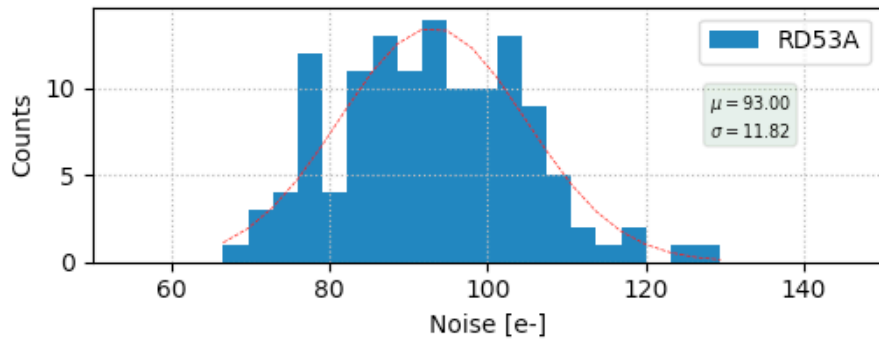
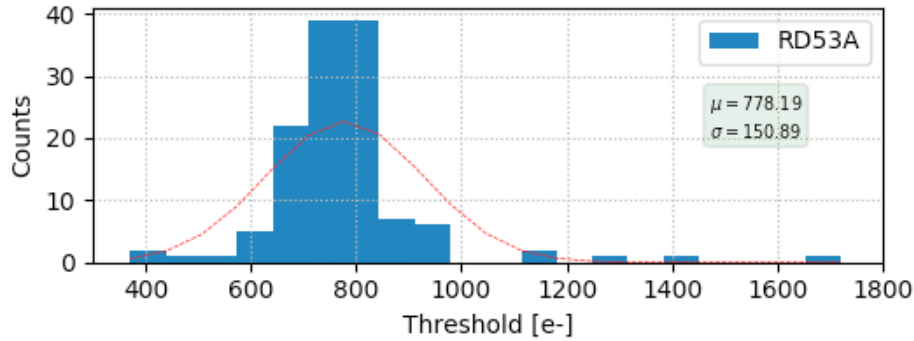
RD53B



- Threshold, Noise and Threshold tuning DAC (TDAC) codes **distributions** for RD53A/B Linear front-end before irradiation

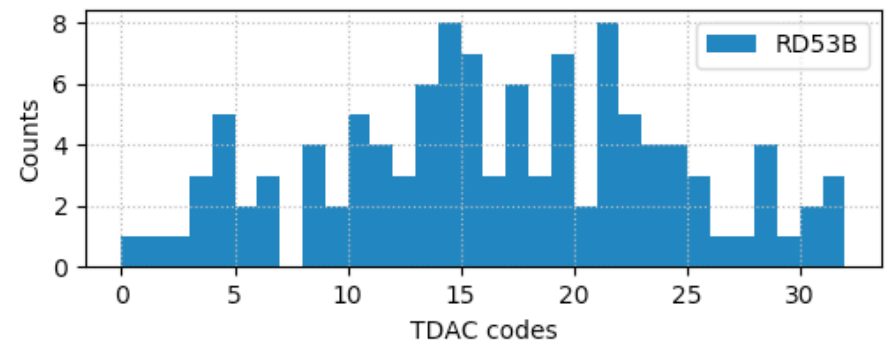
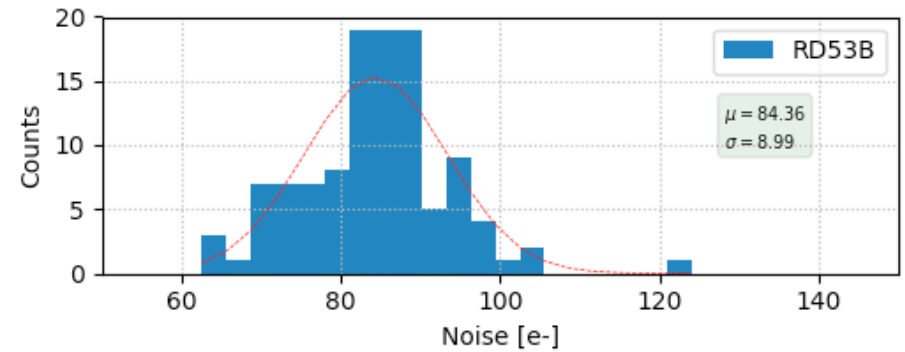
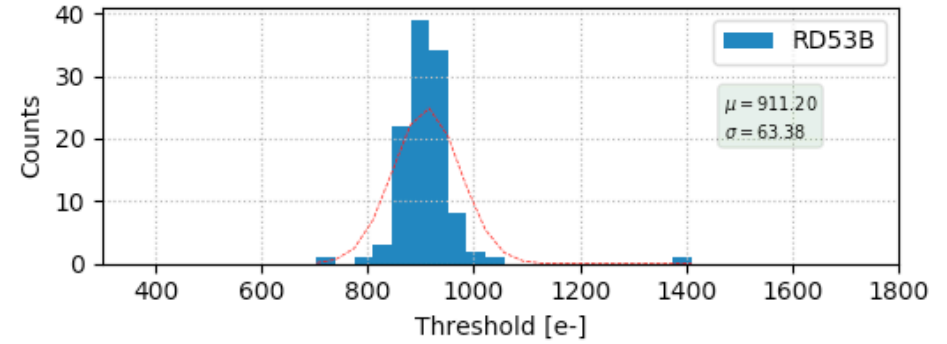
1 Grad results: Threshold and Noise (slow ToT)

RD53A



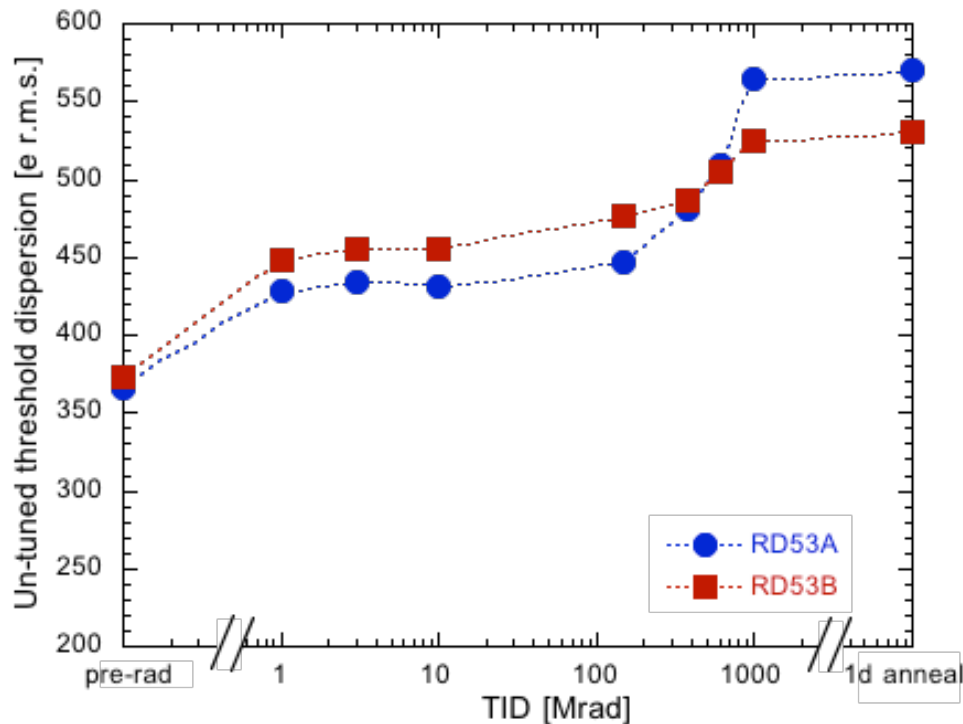
Spikes @ TDAC=0 and TDAC=15

RD53B

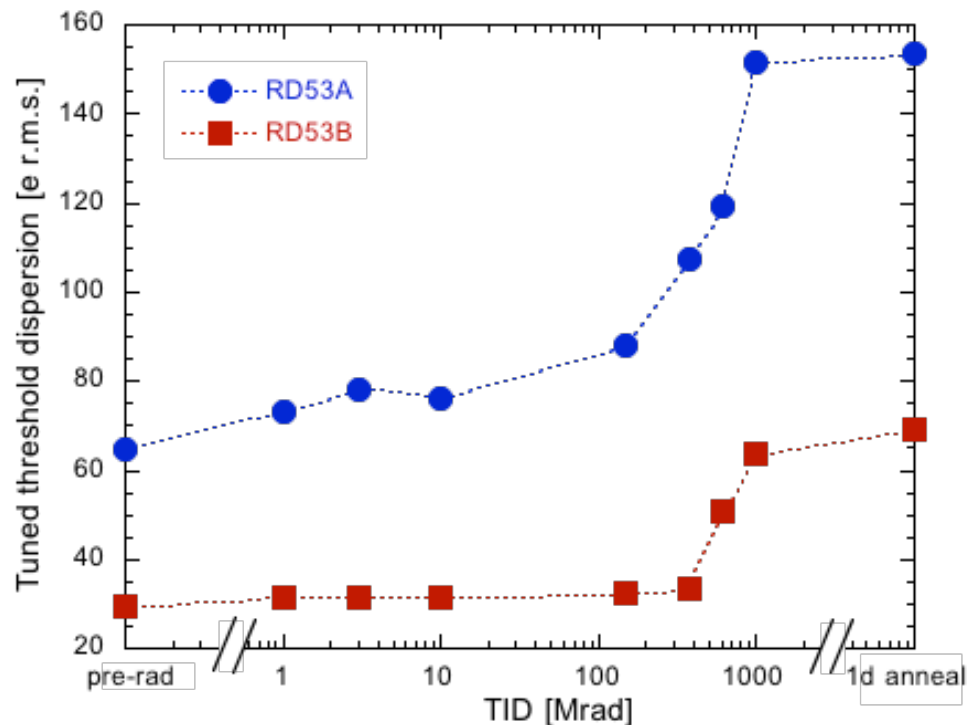


Threshold dispersion vs TID (slow ToT)

Un-tuned threshold dispersion

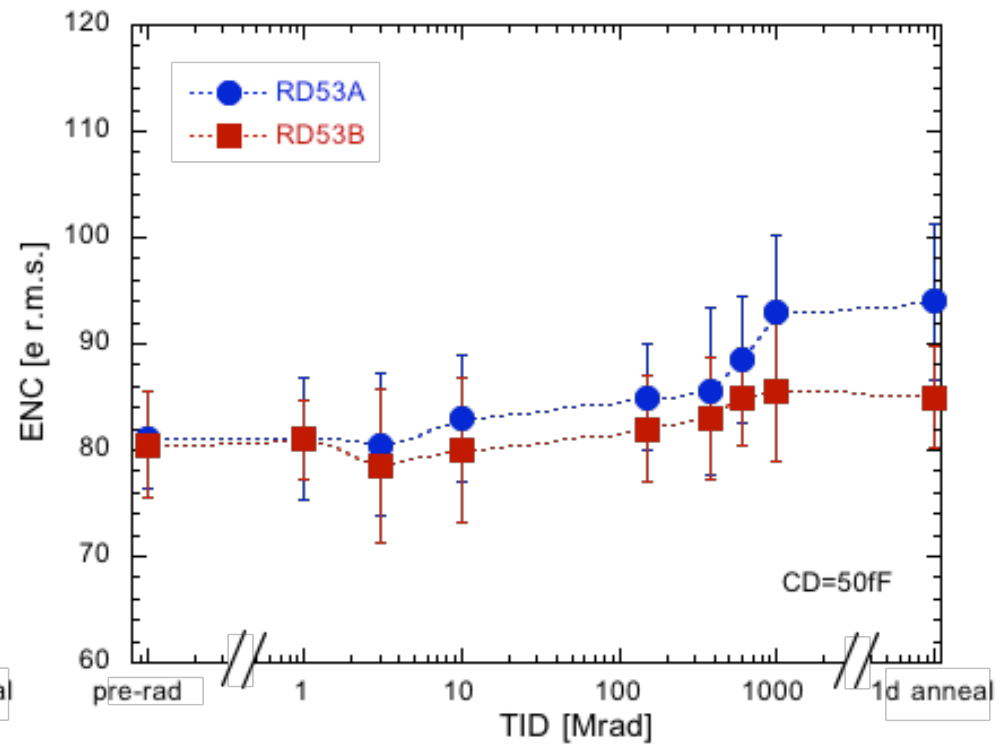
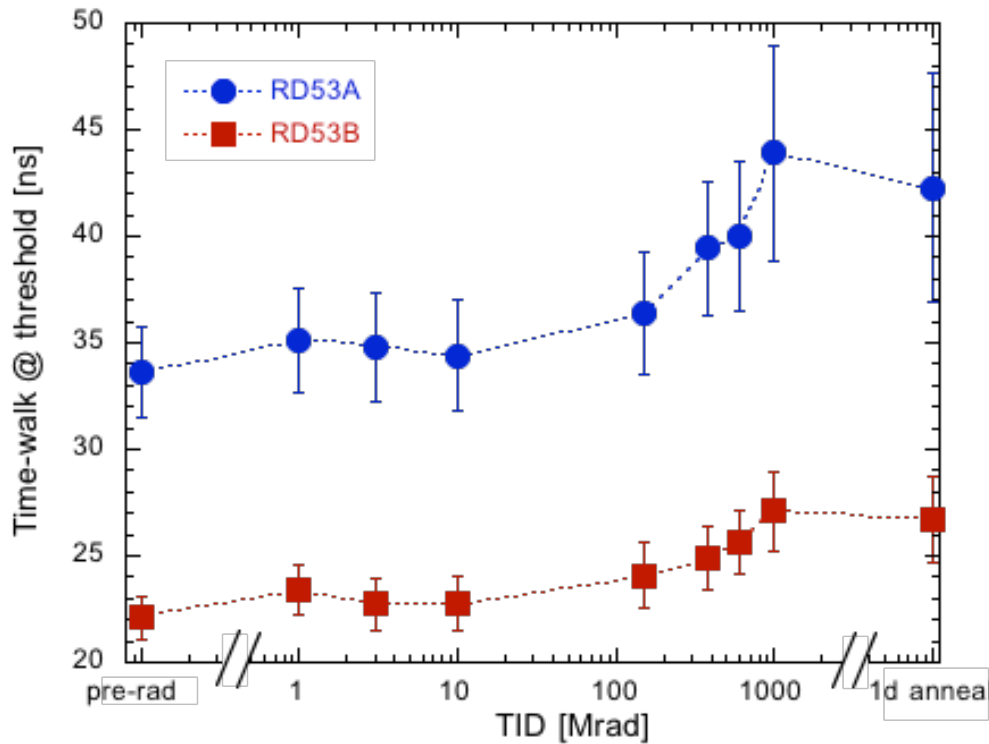


Tuned threshold dispersion



- Significant increase of **un-tuned** threshold dispersion: ~55% (RD53A) and ~40% (RD53B)
- Tuned threshold dispersion ≈ 60 e r.m.s at 1 Grad for RD53B

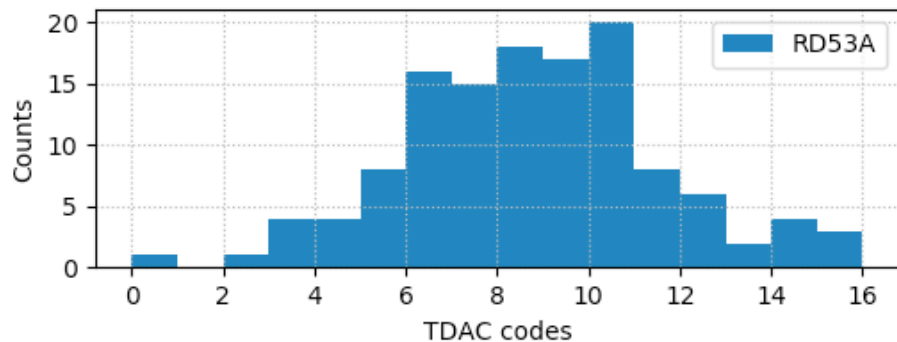
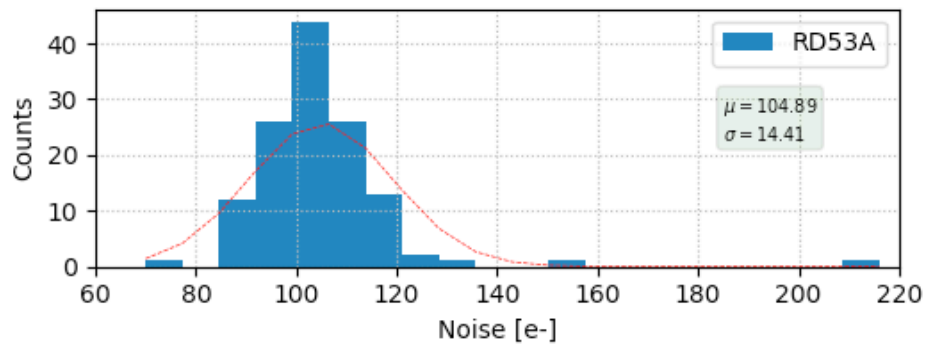
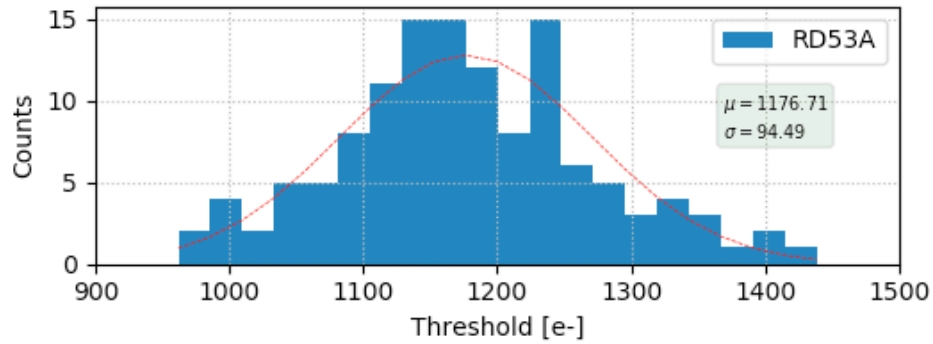
Time-walk and Noise vs TID (slow ToT)



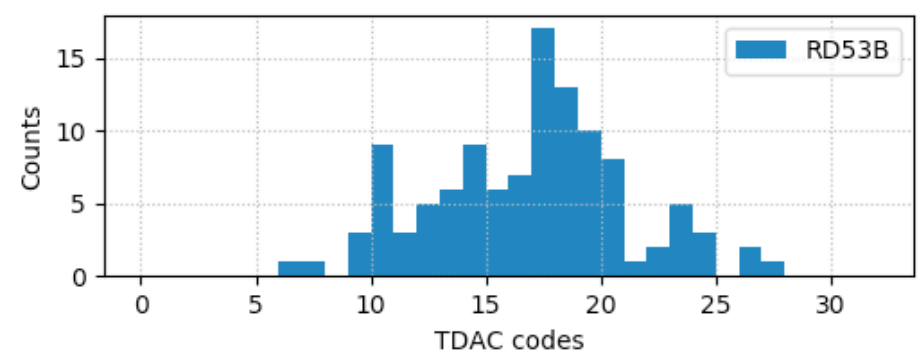
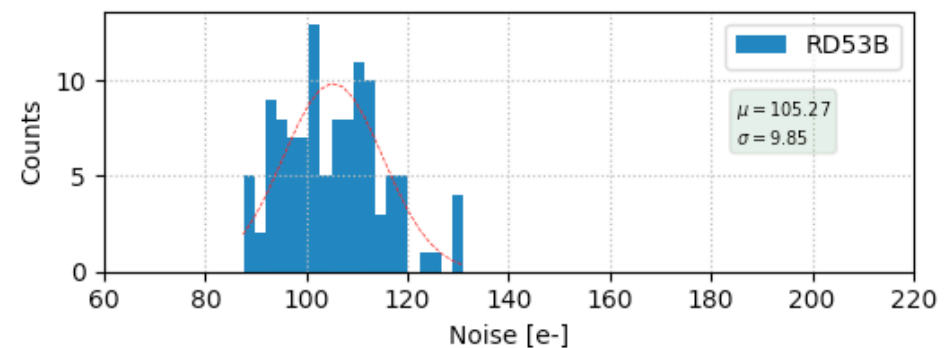
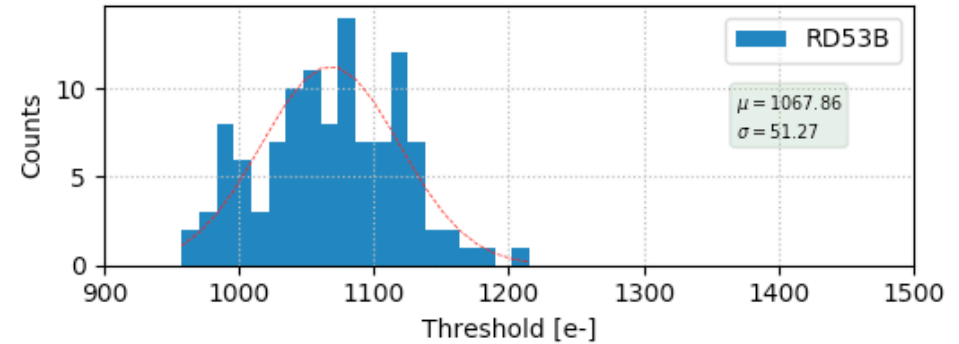
- **Time-walk** for RD53B in general smaller than for RD53A
- Moderate increase of time-walk with TID: 22 ns pre-rad \rightarrow 27 ns @ 1 Grad (RD53B)
- **Noise performance** not significantly affected by radiation
- **Equivalent noise charge (ENC)** slightly smaller for RD53B @ 1 Grad

Pre-rad results: Threshold and Noise (fast ToT)

RD53A

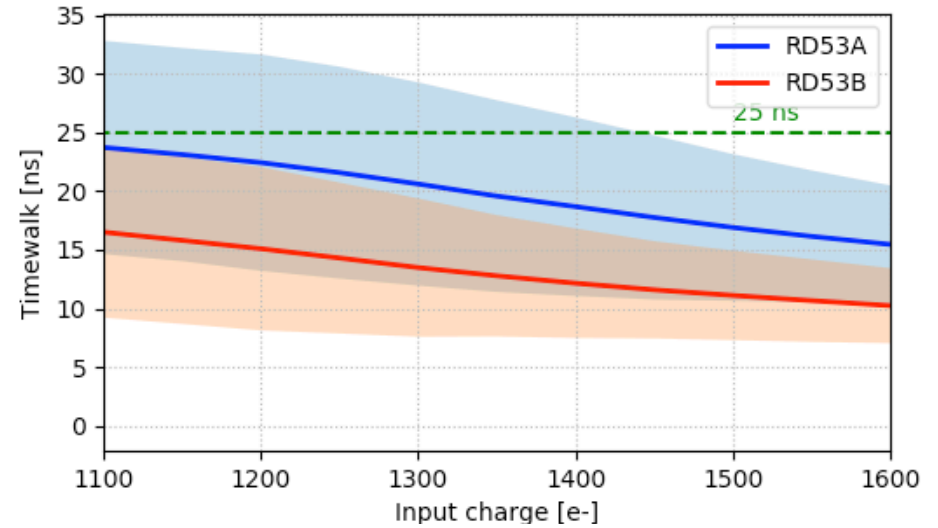
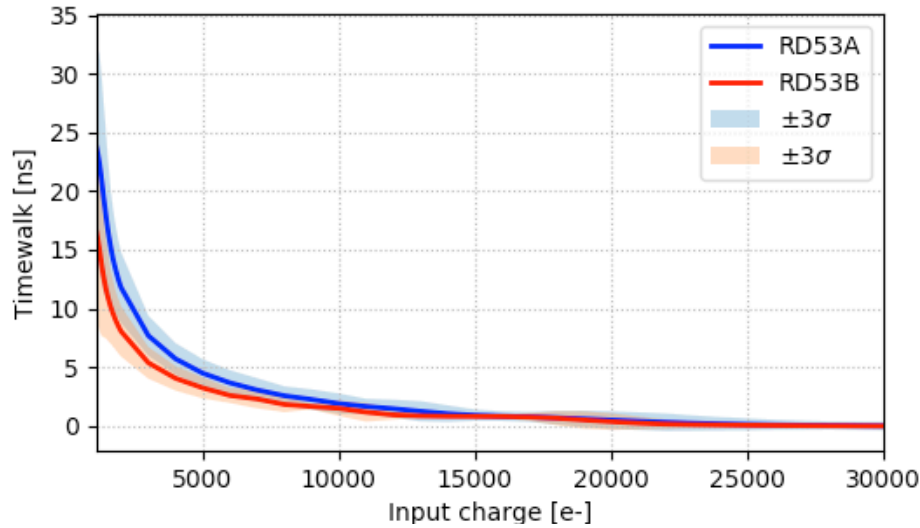


RD53B



- Larger **threshold dispersion** (wrt slow ToT) due to the larger TDAC LSB
- Increased **ENC** with respect to slow ToT (larger noise contribution from Krummnecher feedback network)

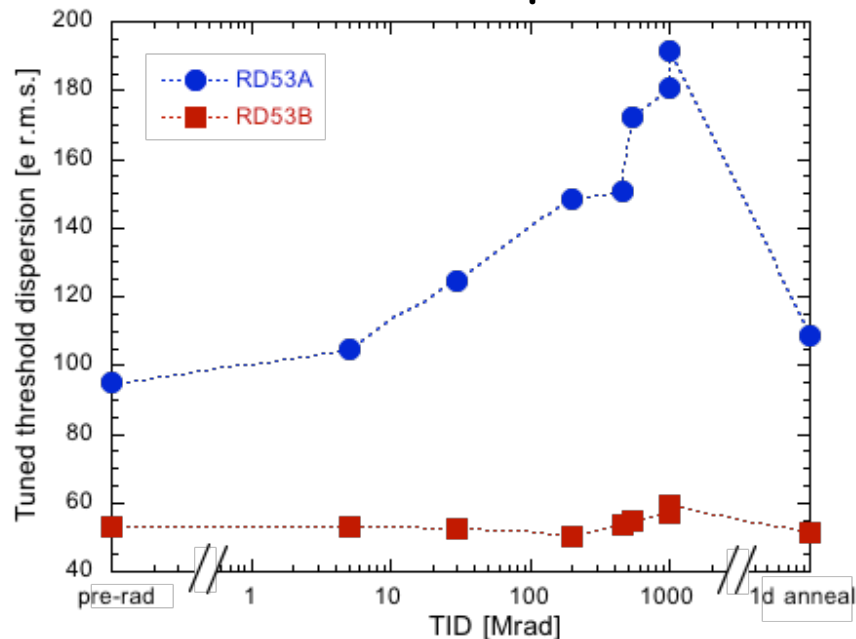
Pre-rad results: time walk (fast ToT)



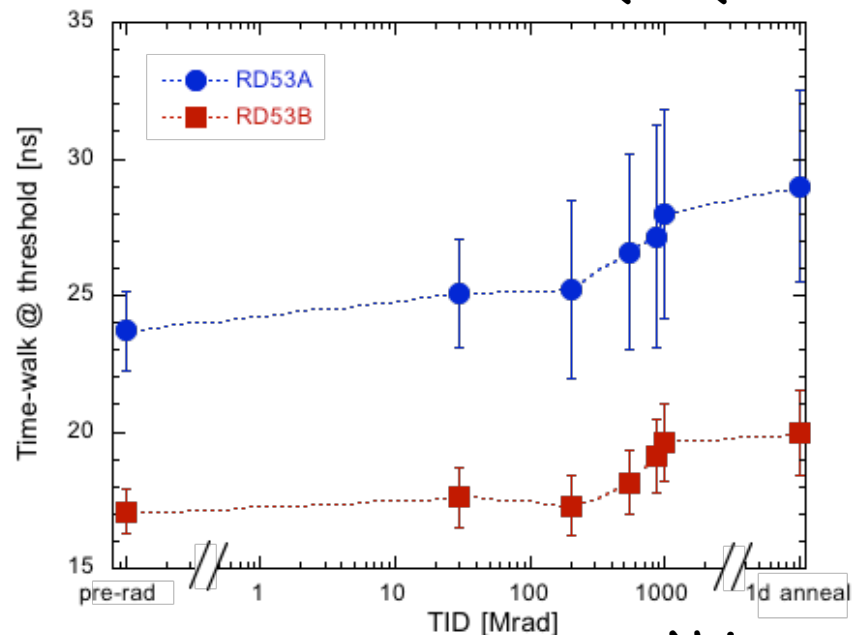
- Smaller **time-walk** wrt slow ToT (faster preamp peaking time)
- Time walk smaller for the RD53B (<25ns in both versions)

Threshold dispersion vs TID (fast ToT)

Tuned threshold dispersion

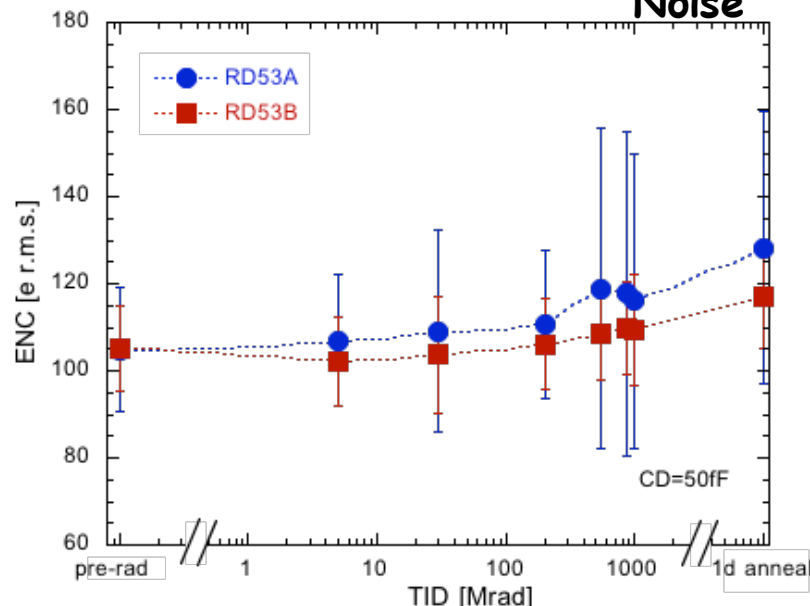


Time-walk evaluated @ $Q_{in}=Q_{th}$



- Significant increase of **tuned** threshold dispersion for RD53A (always < 60 e r.m.s. for RD53B). Recovery after 1d annealing at room T (measurement performed @ room T)
- Increase of **time-walk** with TID (~20% for RD53A, ~10% for RD53B)
- Slight increase of **ENC** with TID

Noise



Conclusions

- The **Linear front-end** has been chosen for the implementation of the pixel readout chips for the HL upgrade of CMS.
- With respect to RD53A, the front-end has been optimized in terms of **time-walk** performance (improved comparator version) and **threshold tuning** capabilities (TDAC saturation effect fixed).
- A **prototype chip** with RD53B Linear front-end was submitted and tested. A radiation campaign has been carried out at CERN on two chips.
- Prototype chips are fully functional at 1 Grad, with results showing little degradation up to 1 Grad for the RD53B version of the Linear front-end.

RD53A floorplan

Top test pad

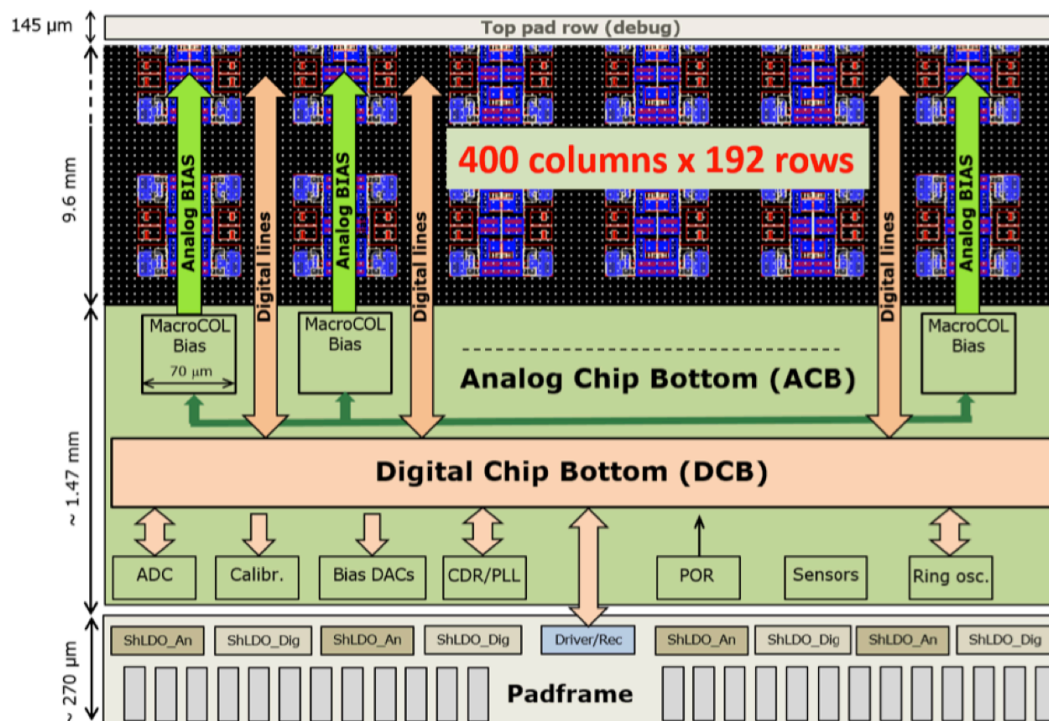
- Row of test pads for debugging purposes
- Will be removed in the production chip

Pixel matrix

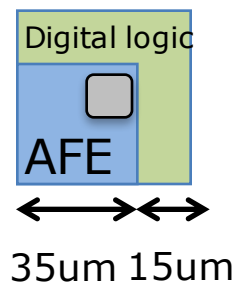
- $192 \times 400 = 76\,800$ pixels

Chip Bottom

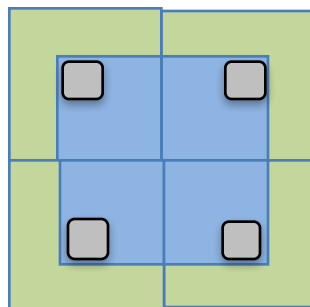
- all global analog and digital circuitry needed to bias, configure, monitor the chip and for signal readout



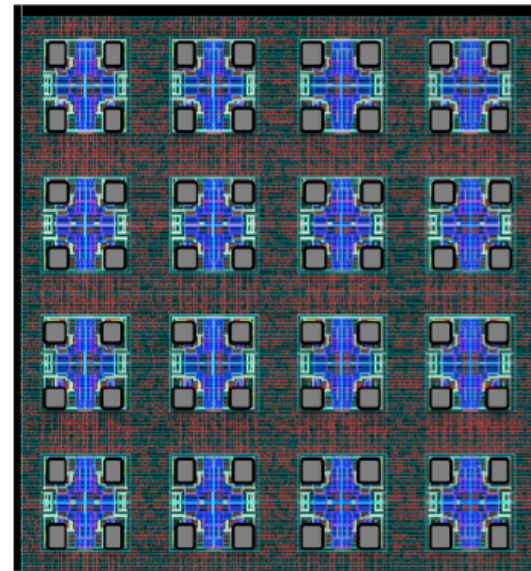
RD53A pixel floorplan



Pixel



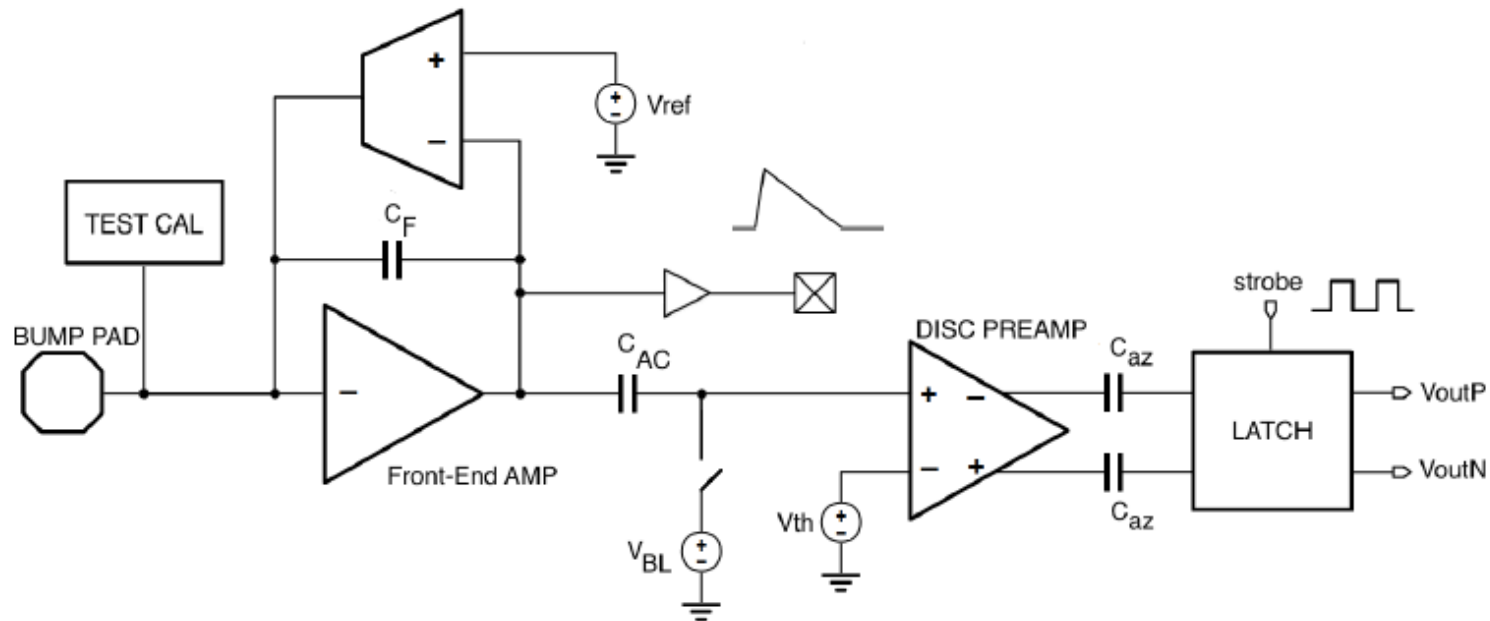
Quad



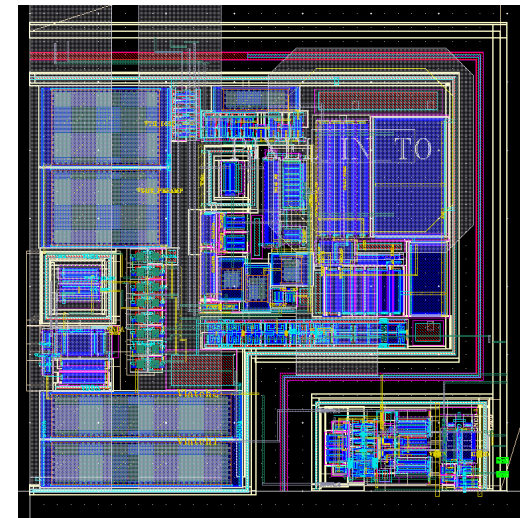
Core

- **Isolation strategy:** two different DNWs for analog and digital
- DNW-isolated analog 'islands':
 - Occasional PFETs using body NW for sub isolation
 - DNW shorted to V_{DDA}
- DNW-isolated digital 'sea':
 - DNW biased at V_{DDD}
- **Global substrate** not used by supply or device bodies

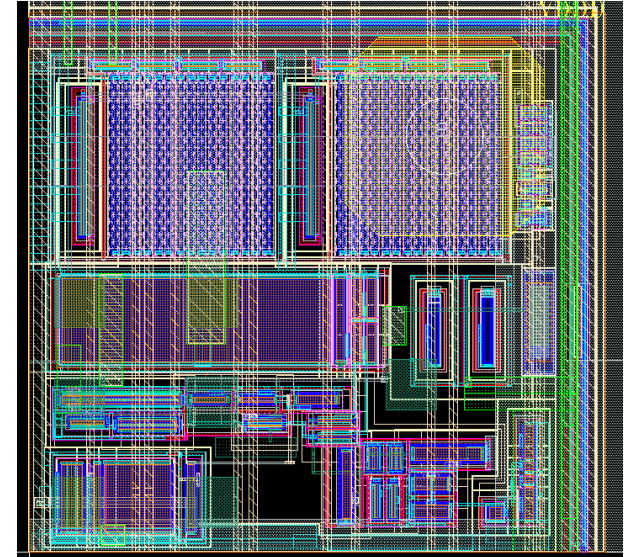
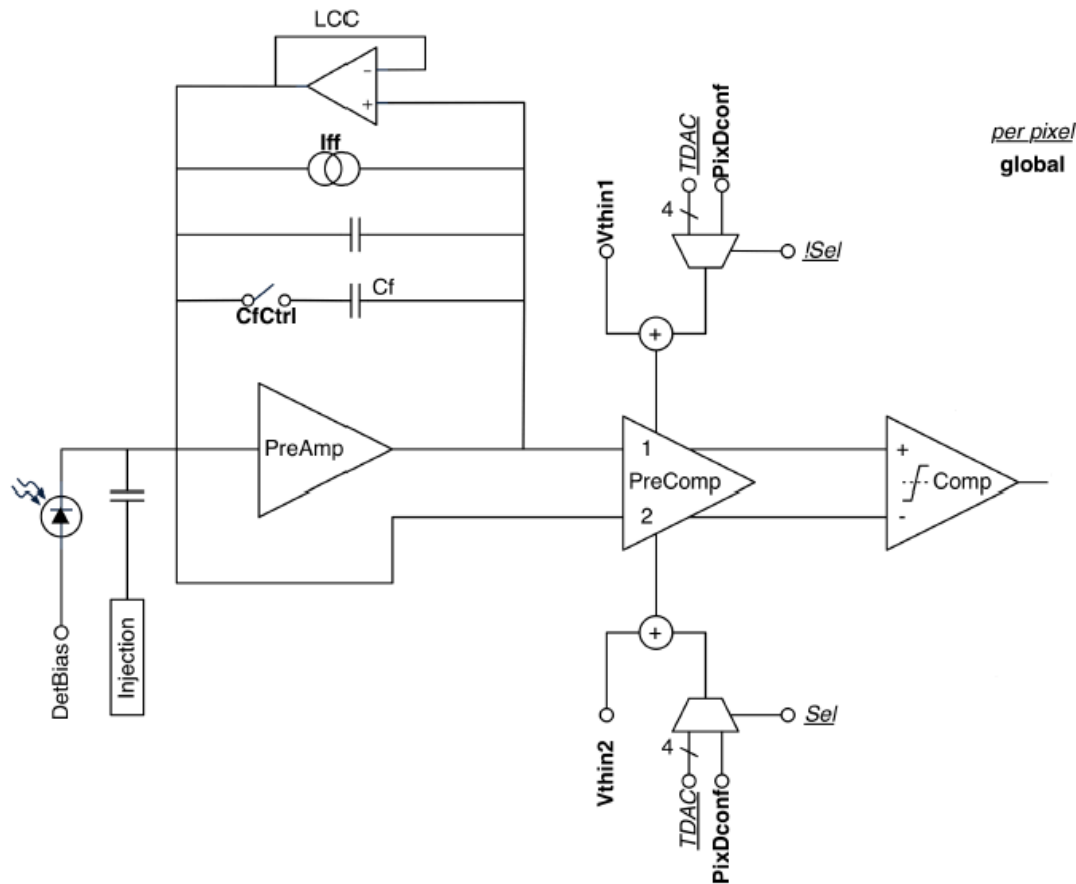
Synchronous Analog Front-end



- **One stage CSA** with **Krummenacher** feedback for linear ToT charge encoding
- **Synchronous discriminator**, AC coupled to CSA, including offset compensated differential amplifier and latch
- Threshold trimming by means of autozeroing (no local trimming DAC)
- **Fast ToT counting** with latch turned into a local oscillator (100-900 MHz)

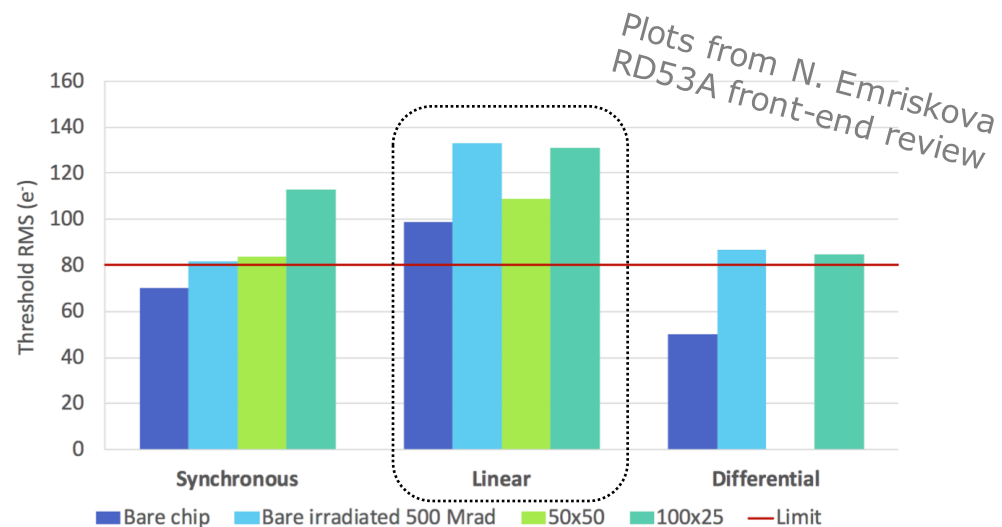
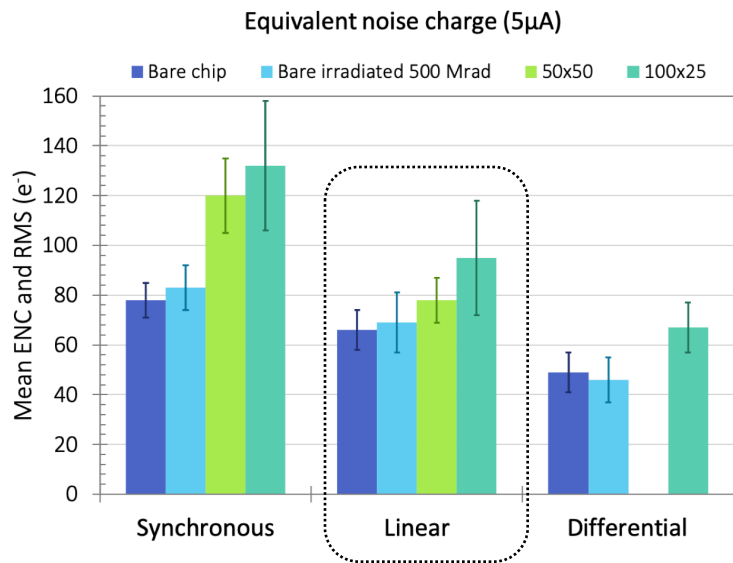


Differential Analog Front-end

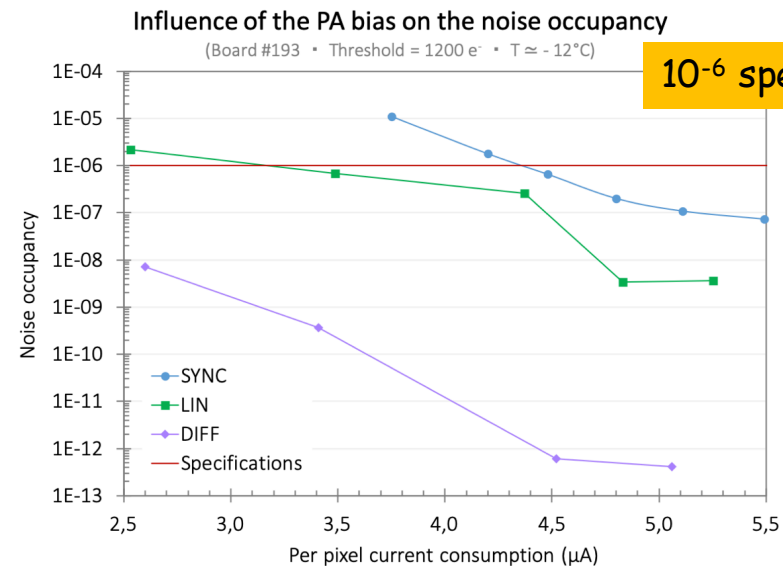


- **Continuous reset integrator** first stage with **DC-coupled pre-comparator** stage
- Two-stage open loop, **fully differential input comparator**
- **Leakage current compensation** a la FEI4
- **Threshold adjusting** with global 8bit DAC and two per pixel 4bit DACs

Noise and threshold dispersion



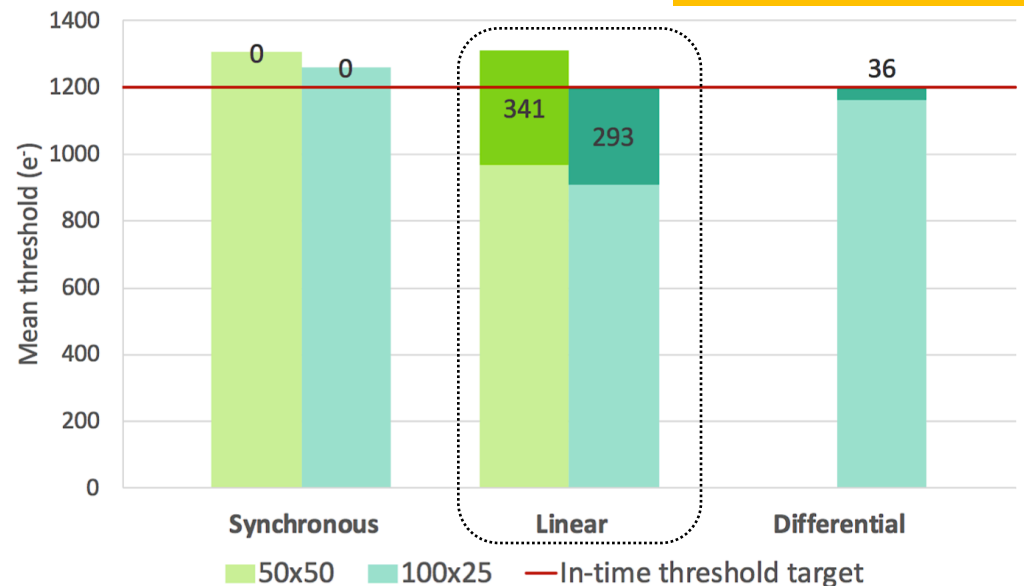
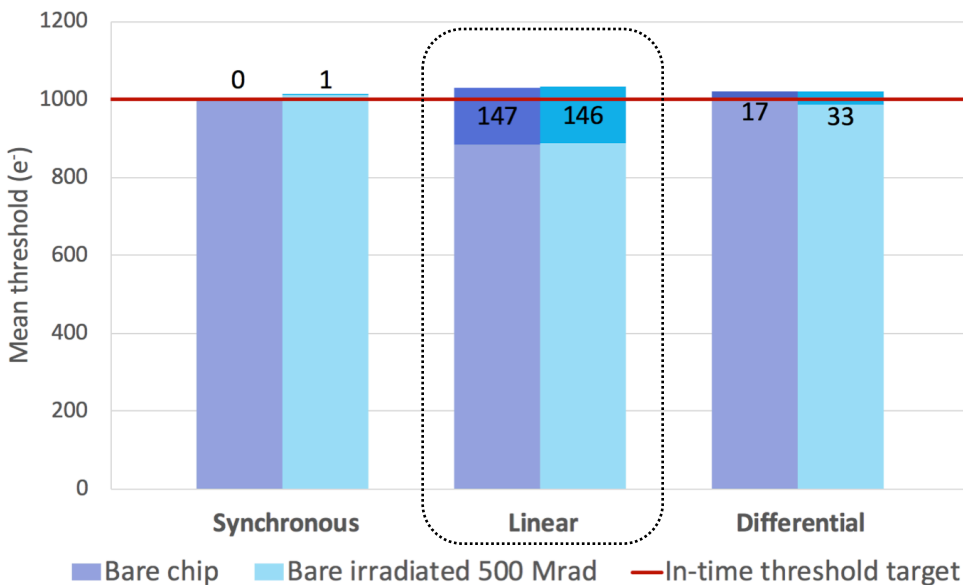
- **Equivalent noise charge and threshold RMS @ 5 μ A for bare chips and assemblies:**
 - 50x50 planar sensor
 - 100x25 planar sensor
- Both parameters have an impact on **noise occupancy** (increasing pixel current consumption also has a beneficial impact thanks to reduced ENC)
- More results on **RD53A: XXXXXXXX**



In-time threshold and overdrive

- **Regular threshold:** the signal charge at which the discriminator has 50% probability to fire
- 25ns BX bunches @ LHC → **in-time threshold:** the minimum signal that is detected in the right BX
- **Overdrive:** in time threshold - regular threshold

Overdrive < 600e⁻
(RD53A spec)

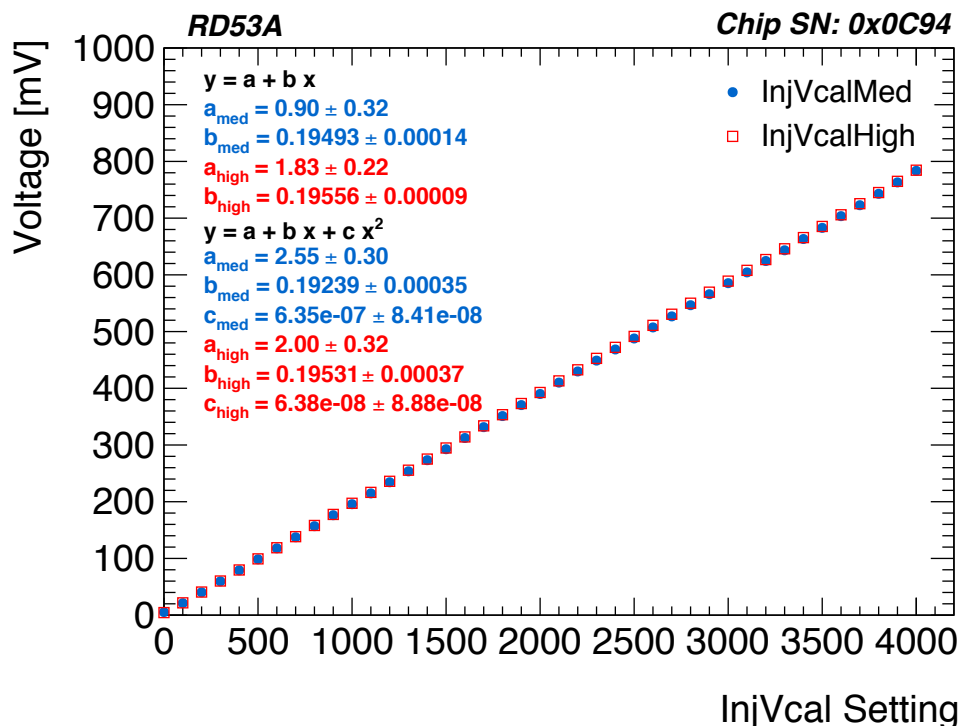
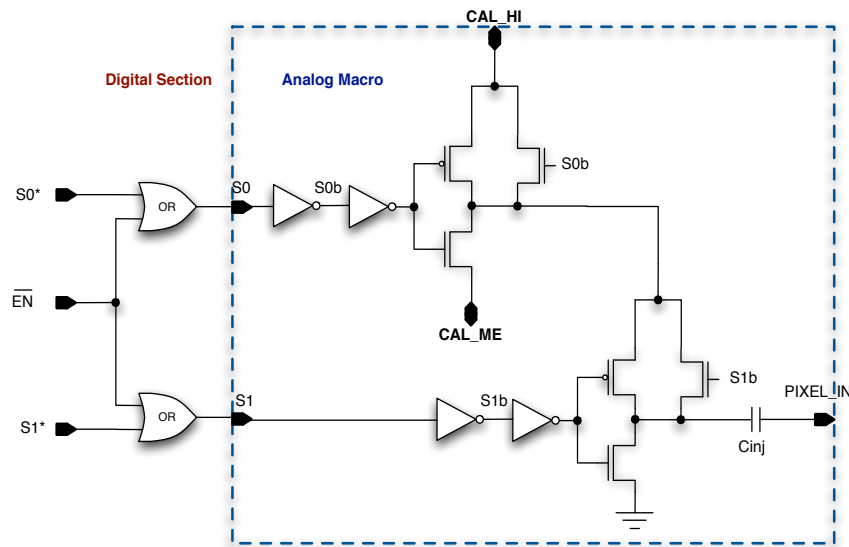


Plots from N. Emriskova
RD53A front-end review

- Bare chips tuned to an in-time threshold of 1000 e⁻ and assemblies to 1200 e⁻

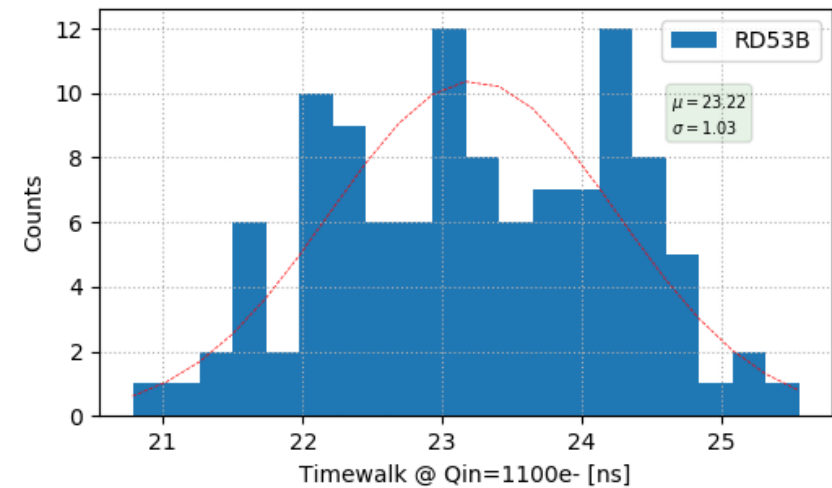
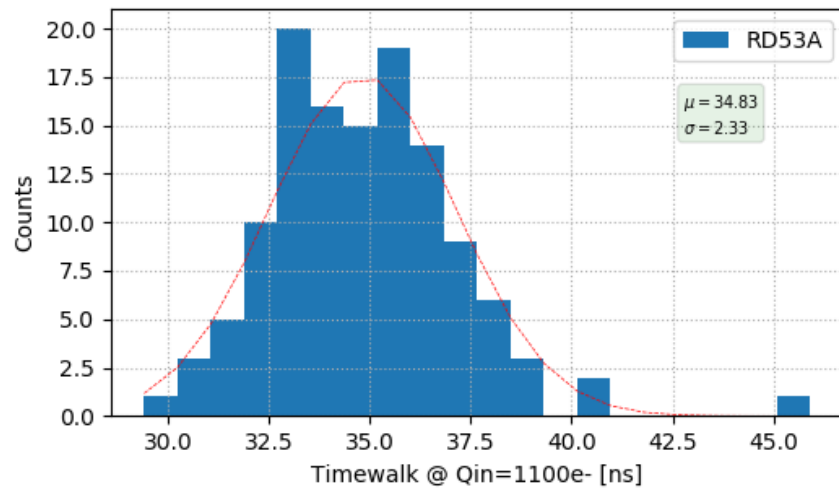
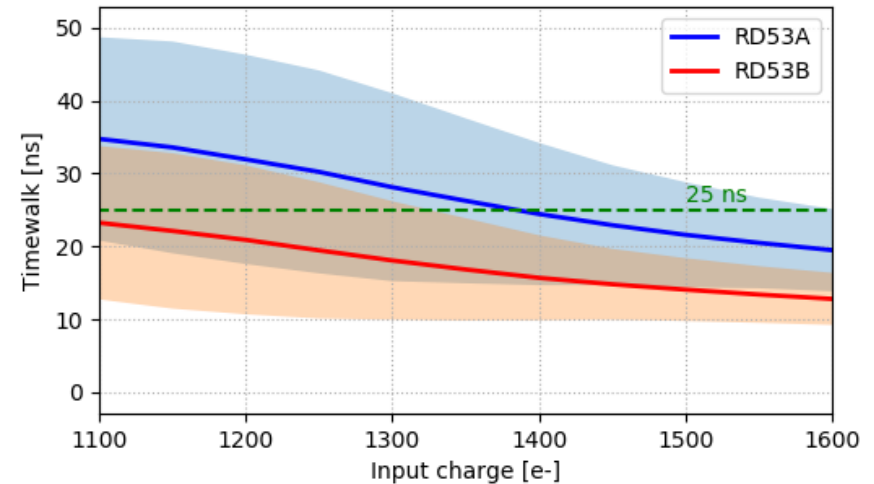
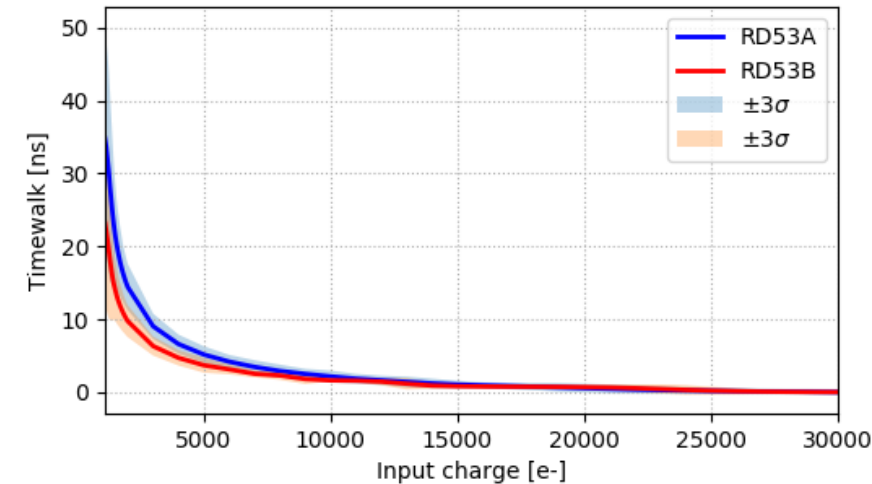
Calibration circuit (in-pixel)

- Local generation of the analog test pulse starting from 2 defined DC voltages CAL_HI and CAL_MI distributed to all pixels and a 3rd level (local GND)
- Two operation modes which allow to generate two consecutive signals of the same polarity or to inject different charges in neighboring pixels at the same time



- Injection DACs fully functional**
- Assuming 8.5fF in-pixel injection cap \rightarrow 10.08 e-/DAC
 - Close to simulation results (\sim 11 e-/DAC)
- All biasing DACs (can be monitored using internal 12-bit ADC and are accessible on a dedicated pad) work fine

Pre-rad results: time walk



- **Time-walk** smaller than 25ns (HL-LHC bunch crossing period) for input charge close to threshold for RD53B