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Optimization of the 65 nm CMOS Linear front-end circuit for the CMS pixel readout at the HL-LHC

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A prototype chip integrating a matrix of 16 × 16 readout channels has been designed and tested in the framework of the RD53 developments for pixel detectors at the High-Luminosity LHC. The matrix is divided in two regions featuring different flavours of the front-end stage, or Linear front-end, that have been tested and compared. The front-end channels include a low-noise charge sensitive amplifier with detector leakage compensation circuit, a free-running comparator, and a current-mode DAC for threshold tuning. The front-end circuits were developed in a 65 nm CMOS technology and feature an overall area of 35 µm × 35 µm with a current consumption close to 5 µA. The prototype has been tested before and after exposure to total ionizing doses up to 1 Grad(SiO_2) of X-rays. A comprehensive discussion of the design and of the characterization of the readout channels will be provided in the conference paper.

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