Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

Sensor development and chip design of innovative low-power, large area FD-MAPS

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16th Trento Workshop
ARCADIA sensor
design based on SEED project

- 110 nm CMOS process with 1.2 V transistors, developed with LFoundry
- fully depleted, charge collection by drift
- backside processing (diode+GR on back)
- low resistivity epi-layer for delayed on-set of punch-through currents

→ realised in SEED in 100 - 300 µm
(< 100 µm n-substrate in epi, bias from front)
ARCADIA sensor – Operation

2D TCAD simulation of 3 'standard' 25µm pitch pixels, 50µm thickness

\[ V_{ntop} = 0.8V, \text{ starts depletion from back side} \]

Absolut values of \( V_{dpl}/V_{pt}/V_{pw} \) determined from I-V curves.
ARCADIA sensor – Operation

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- $V_{\text{ntop}} = 0.8\text{V}$, starts depletion from back side
- $V_{\text{dpl}} = -7\text{V}$, epi-layer not fully-depleted but single collection electrodes electrically isolated

Absolut values of $V_{\text{dpl}}/V_{\text{pt}}/V_{\text{pw}}$ determined from I-V curves.

16/02/2021
coralie.neubueser@tifpa.infn.it: ARCADIA FD-MAPS
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- \( V_{dpl} = -7V \), epi-layer not fully-depleted but single collection electrodes electrically isolated
- \( V_{pt} = -11V \), on-set of punch-through between pwell and p\(^+\) back

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- \( V_{pt} = -11 \text{V} \), on-set of punch-though between pwell and p\text{+} back
- \( V_{pw} = -15.5 \text{V} \), maximum power consumption 0.1 mW/cm\(^2\)

Absolut values of \( V_{dpl}/V_{pt}/V_{pw} \) determined from I-V curves.
SEED results on Pseudo-Matrices

- pixels short-circuited
- tests in micro-beam of 2MeV $p^+$ in Zagreb
  
doi:10.1109/TED.2020.2985639,
  doi:10.1088/1748-0221/14/06/C06016

Latest results on data versus 3D TCAD simulations
**SEED results on MATISSE chip**

**Monolithic AcTIve pixel SenSor Electronics**

doi:10.1109/NSSMIC.2017.8532806

- 24 $\times$ 24 active pixel array
- 50$\mu$m $\times$ 50$\mu$m pixels
- partially integrated electronics
- 4 sectors read out in parallel
- tests of different diode geometries

- scan with $^{55}$Fe, 300$\mu$m thick at $V_{back} = 200$ V ($V_{dpl} = 100$ V), clustering applied with SNR$\sim$6

- tests of 100$\mu$m thick chip after TID
Targeted applications

- medical scanners (proton CT)
- future lepton colliders
- space experiments
- possibly x-ray applications with thick substrates

Requirements:

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>power consumption</td>
<td>5-20 mW/cm²</td>
</tr>
<tr>
<td>hit rate</td>
<td>10-100 MHz/cm²</td>
</tr>
<tr>
<td>timing</td>
<td>1-10 µs</td>
</tr>
<tr>
<td>radiation tolerance</td>
<td>10-50 krad / &lt; 10^{11} neq</td>
</tr>
<tr>
<td>matrix area</td>
<td>24 cm²</td>
</tr>
<tr>
<td>1st prototype</td>
<td>1.3 × 1.3 cm²</td>
</tr>
</tbody>
</table>
• matrix core $512 \times 512$ pxis of 25 $\mu$m pitch
• pixels are $\sim(50/50)$% analog/digital
• sensor diode about 20% of total area
• clock-less matrix (to minimize power dissipation)
• pixel regions propagate the output data to the periphery
two front-end solutions under test:

(a) ALPIDE-like
(b) bulk-driven

- diode area: $9 \times 9 \, \mu \text{m}^2$
- analog circuits area: $223 \, \mu \text{m}^2$

Monte-Carlo simulations on MIP signals:

► jitter negligible against time walk
► bulk driven slightly faster

→ charge vs. time walk/dead times lookup table for full chip simulations
Readout architecture MD1 (1)

- strip-like column drain type

- global shutter with serial readout
- 4 analogue outputs
- low power mode for space applications (one active high-speed output)
- matrix and EoC architecture, data links and payload ID: scalable to $2048 \times 2048$ pxtls
- columns divided in cores (32x2 pxtls) and pixel regions (2x2 pxtls)
Readout architecture MD1 (2)

Pixel clustering within matrix:

- classification of pixel region in 'Masters' and top/bottom 'Slaves', only Masters can send signal

→ reduces column occupancy
→ allows clock running only on periphery
Chip verification and simulation of different particle-types and substrate thicknesses

Monte-Carlo simulation for random cluster generation, combined with look-up tables of time walk and deadtime

example: $p^+$ of Trento Proton Therapy Center

- 100 MHz/cm$^2$, uniform cluster distribution
- 100 $\mu$m thickness

$\rightarrow$ less 1% cluster loss
Conclusions and Plans

- Sensor technology proven functionality in SEED
- First trigger-less binary data readout full-chip demonstrator samples available May 2021
- DAQ in preparation for electrical testing of MD1
- DAQ for telescope with 9 ARCADIA chips in preparation, for beam tests by Fall 2021

Ongoing developments:
- Test of new architecture, SEU protection → 2nd engineering run summer 2021
- Debugging of current baseline + potentially new test-structures → 3rd run beginning 2022
- R&D on new sensor designs (fast timing) → implemented optimised geometry in test-structures..
Optimised sensor geometries
realised in test-structures, electrical testing starts in June 2021

- micro-strips of 1.2 cm length
- $1 \times 1$ and $2 \times 2$ mm$^2$ pseudo-matrices

- extensive TCAD simulation campaign to test different pixel/micro-strip geometries
TCAD simulations of FD-MAPS

- test different geometries in I-V/C-V and transients → selected for minimal capacitance and fastest CCE
- employed a surface/bulk damage model AIDA-2020-D7.4

on-going: tests of new ideas to optimise sensor for sub-ns charge collection..

Many thanks!