TIFPA
Trento Institute for Fundamental Physics and Applications

ARCADIA

Advanced **R**eadout **C**MOS **A**rchitectures with **D**epleted **I**ntegrated sensor **A**rrays

Sensor development and chip design of innovative low-power, large area FD-MAPS

Coralie Neubüser on behalf of the ARCADIA collaboration
Material from: Davide Falchieri, Sara Garbolino, Serena Mattiazzo, Lucio Pancheri, Andrea Paternò, Manuel Rolo

16/02/2021

16th Trento Workshop

ARCADIA sensor

design based on SEED project

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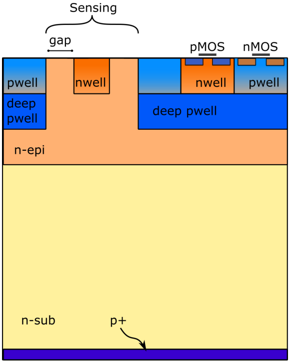

- 110 nm CMOS process with 1.2 V transistors, developed with LFOUNDRY
- fully depleted, charge collection by drift
- backside processing (diode+GR on back)
- low resistivity epi-layer for delayed on-set of punch-through currents

$\rightarrow$ realised in SEED in 100 - 300 μm

($<$ 100 μm n-substrate in epi, bias from front)

ARCADIA sensor – Operation

2D TCAD simulation of 3 'standard' 25μm pitch pixels, 50μm thickness

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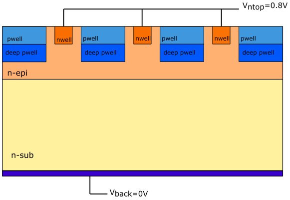
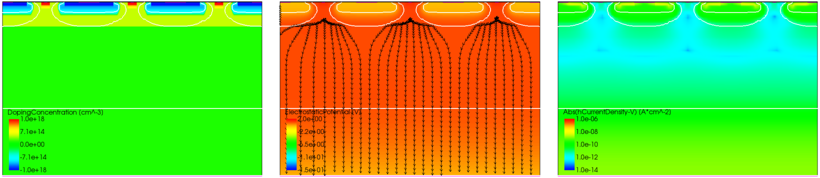


- $V_{ntop} = 0.8$V, starts depletion from back side



Absolut values of $V_{dpl}/V_{pt}/V_{pw}$ determined from I-V curves.

ARCADIA sensor – Operation

2D TCAD simulation of 3 'standard' 25μm pitch pixels, 50μm thickness

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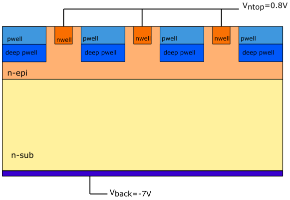
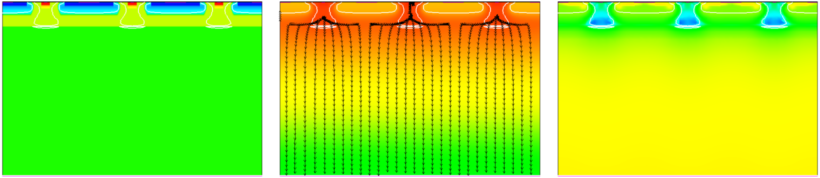


- $V_{ntop} = 0.8$V, starts depletion from back side
- $V_{dpl} = -7$V, epi-layer not fully-depleted but single collection electrodes electrically isolated



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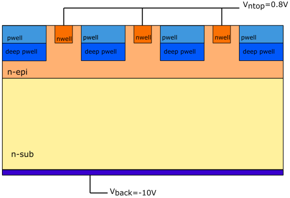
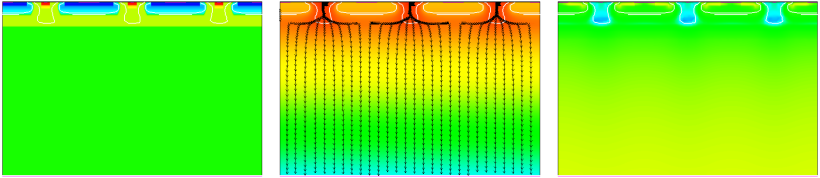


- $V_{ntop} = 0.8$V, starts depletion from back side
- $V_{dpl} = -7$V, epi-layer not fully-depleted but single collection electrodes electrically isolated
- $V_{pt} = -11$V, on-set of punch-though between pwell and p^+ back



Absolut values of $V_{dpl}/V_{pt}/V_{pw}$ determined from I-V curves.

ARCADIA sensor – Operation

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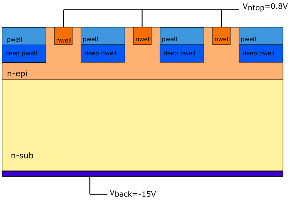

- $V_{ntop} = 0.8$V, starts depletion from back side
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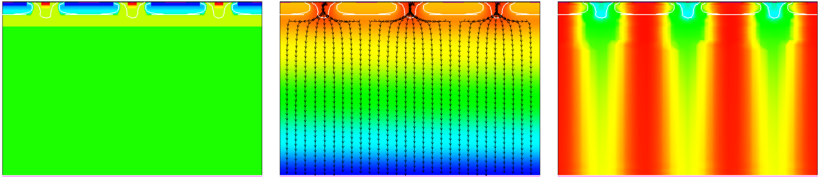
- $V_{pt} = -11$V, on-set of punch-though between pwell and p^+ back
- $V_{pw} = -15.5$V, maximum power consumption 0.1 mW/cm^2



Absolut values of $V_{dpl}/V_{pt}/V_{pw}$ determined from I-V curves.

SEED results on Pseudo-Matrices

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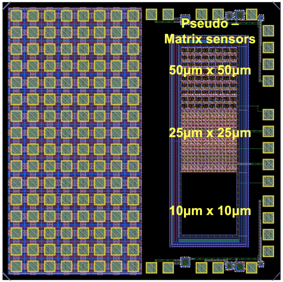
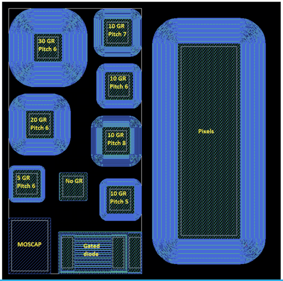
frontside

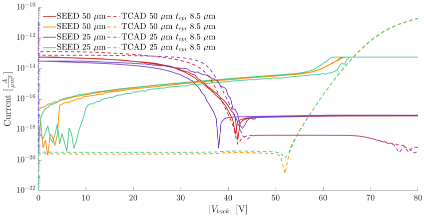


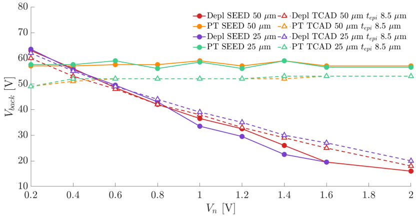
backside



- pixels short-circuited
- tests in micro-beam of 2MeV p^+ in Zagreb
  doi:10.1109/TED.2020.2985639,
  doi:10.1088/1748-0221/14/06/C06016

Latest results on data versus 3D TCAD simulations





Thomas Corradino, doctoral student in Trento

SEED results on MATISSE chip

Monolithic AcTIve pixel SenSor Electronics

doi:10.1109/NSSMIC.2017.8532806

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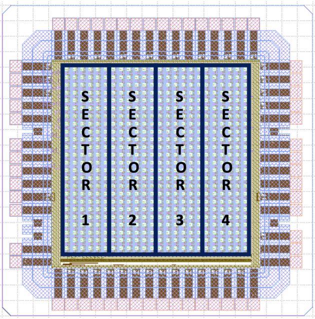
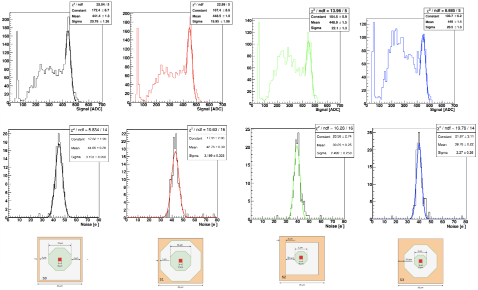
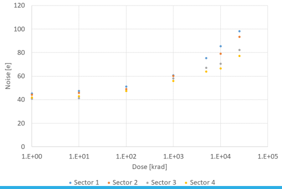


- 24 × 24 active pixel array
- 50μm × 50μm pixels
- partially integrated electronics
- 4 sectors read out in parallel
- tests of different diode geometries

- scan with ^{55}Fe, 300μm thick at $V_{back} = 200$ V ($V_{dpl} = 100$ V), clustering applied with SNR∼6



- tests of 100μm thick chip after TID



Serena Mattiazzo, Padova

Targeted applications

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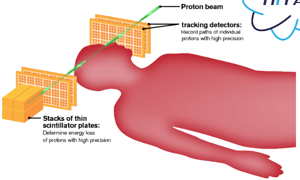
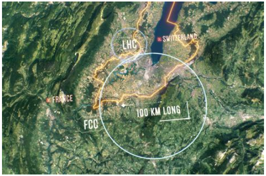
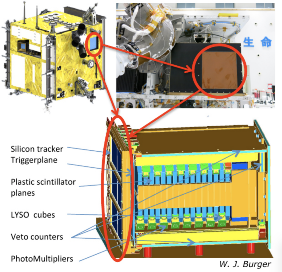


- medical scanners (proton CT)
- future lepton colliders
- space experiments
- possibly x-ray applications with thick substrates



Requirements:

power consumption	5-20 mW/cm^2
hit rate	10-100 MHz/cm^2
timing	1-10 μs
radiation tolerance	10-50 krad / $< 10^{11}$ neq
matrix area	target: 24 cm^2
	1st prototype: 1.3×1.3 cm^2



ARCADIA MD1 – specs

trigger-less, and binary readout

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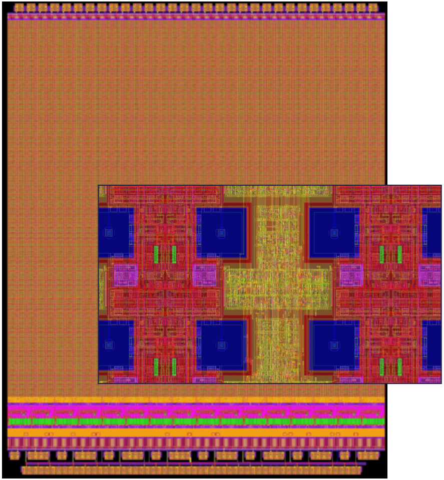
- matrix core 512 $\times$ 512 pxls of 25 μm pitch
- pixels are $\sim$(50/50)% analog/digital
- sensor diode about 20% of total area
- clock-less matrix (to minimize power dissipation)
- pixel regions propagate the output data to the periphery



Manuel Rolo, Torino

ARCADIA MD1a/b – front end

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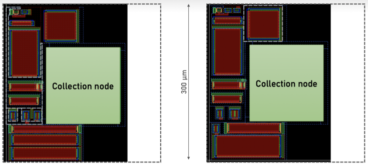
two front-end solutions under test:

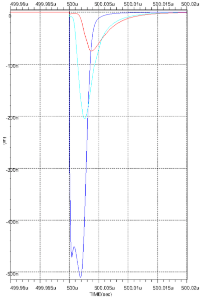
(a) ALPIDE-like

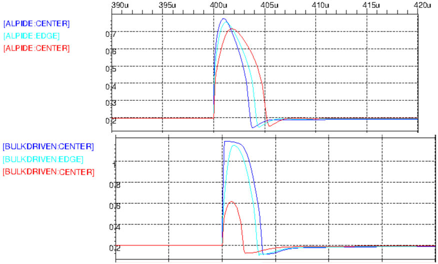
(b) bulk-driven

- diode area: $9 \times 9\ \mu m^2$
- analog circuits area: $223\ \mu m^2$



Monte-Carlo simulations on MIP signals:





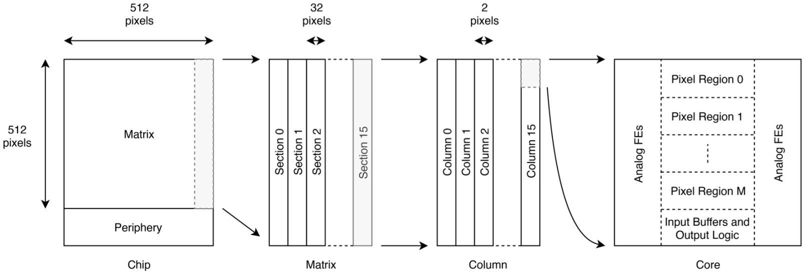
- jitter negligible against time walk
- bulk driven slightly faster

→ charge vs. time walk/dead times lookup table for full chip simulations

Sara Garbolino, Torino

Readout architecture MD1 (1)

strip-like column drain type



- global shutter with serial readout
- 4 analogue outputs
- low power mode for space applications (one active high-speed output)
- matrix and EoC architecture, data links and payload ID: scalable to 2048 $\times$ 2048 pxls
- columns divided in cores (32x2 pxls) and pixel regions (2x2 pxls)

Readout architecture MD1 (2)

Pixel clustering within matrix:

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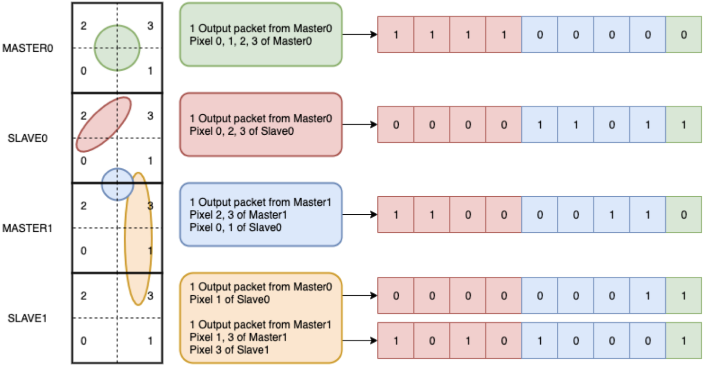
- classification of pixel region in 'Masters' and top/bottom 'Slaves', only Masters can send signal



→ reduces column occupancy
→ allows clock running only on periphery

Andrea Paternò, Torino

Chip verification and simulation

of different particle-types and substrate thicknesses

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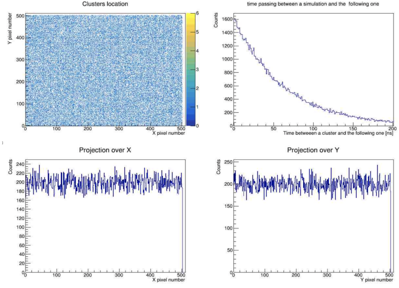
Monte-Carlo simulation for random cluster generation, combined with look-up tables of time walk and deadtime

example: p^+ of Trento Proton Therapy Center

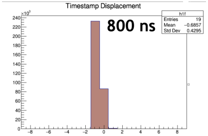
- 100 MHz/cm^2, uniform cluster distribution
- 100 μm thickness



→ less 1% cluster loss

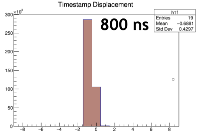
small dE/dx=9.2MeV/cm

```
Final Summary:
   Matched hits:                          319964/    321437 (99.542% of sent)
   Timing displaced hits:                 233403/    321437 (72.612% of sent)
   Deadtime (not injected) hits:            1463/    321437 ( 0.455% of sent)
   Ghost hits:                                 0/    319966 ( 0.000% of recv)
   Duplicate hits:                             1/    319966 ( 0.000% of recv)

   Missing hits:                               8
```



large dE/dx=23MeV/cm

```
Final Summary:
   Matched hits:                          393007/    395245 (99.434% of sent)
   Timing displaced hits:                 287460/    395245 (72.730% of sent)
   Deadtime (not injected) hits:            2229/    395245 ( 0.564% of sent)
   Ghost hits:                                 0/    393008 ( 0.000% of recv)
   Duplicate hits:                             0/    393008 ( 0.000% of recv)

   Missing hits:                               8
```



Davide Falchieri, Bologna

Conclusions and Plans

- sensor technology proven functionality in SEED
- first trigger-less binary data readout full-chip demonstrator samples available May 2021
- DAQ in preparation for electrical testing of MD1
- DAQ for telescope with 9 ARCADIA chips in preparation, for beam tests by Fall 2021

Ongoing developments:

- test of new architecture, SEU protection
  $\rightarrow$ 2nd engineering run summer 2021
- debugging of current baseline + potentially new test-structures
  $\rightarrow$ 3rd run beginning 2022
- R&D on new sensor designs (fast timing)
  $\rightarrow$ implemented optimised geometry in test-structures..

Optimised sensor geometries

realised in test-structures, electrical testing starts in June 2021

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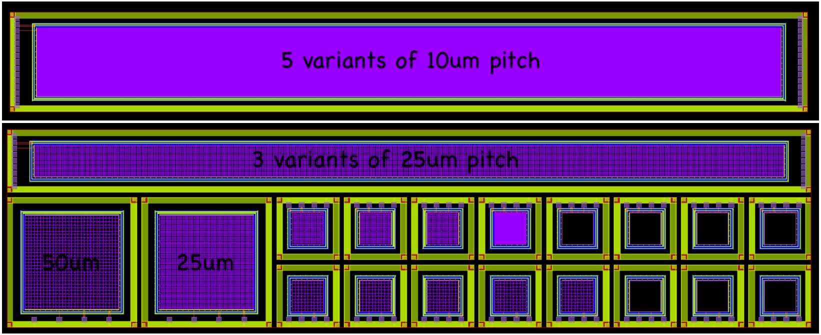
- micro-strips of 1.2 cm length
- 1 × 1 and 2 × 2 mm^2 pseudo-matrices



- extensive TCAD simulation campaign to test different pixel/micro-strip geometries

TCAD simulations of FD-MAPS

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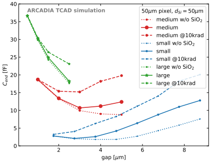
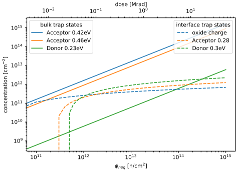
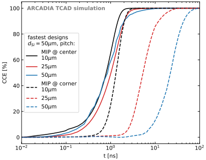
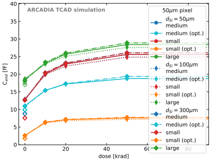
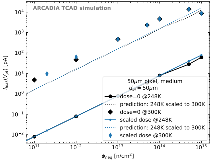
- test different geometries in I-V/C-V and transients
  → selected for minimal capacitance and fastest CCE
- employed a surface/bulk damage model *AIDA-2020-D7.4*











on-going: tests of new ideas to optimise sensor for sub-ns charge collection..

→ details on simulations of FD-MAPS can be found: *arXiv:2011.09723*, **talk** by Lorenzo on FD-MAMS (*arXiv:2101.09088*)

ARCADIA collaboration

INFN - Bologna, Milano, Padova, Perugia, Pavia, TIFPA, Torino

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